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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx350f256h-v-mr

PIC32MX330/350/370/430/450/470

TABLE 7: PIN NAMES FOR 124-PIN DEVICES

124-PIN VTLA (BOTTOM VIEW) ^(1,2,3,4)			
PIC32MX430F064L PIC32MX450F128L PIC32MX450F256L PIC32MX470F512L			
Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
A1	No Connect	A38	D-
A2	RG15	A39	SCL2/RA2
A3	Vss	A40	TDI/CTED9/RA4
A4	AN23/PMD6/RE6	A41	VDD
A5	RPC1/RC1	A42	OSC2/CLKO/RC15
A6	RPC3/RC3	A43	Vss
A7	AN16/C1IND/RPG6/SCK2/PMA5/RG6	A44	SDA1/RPA15/RA15
A8	AN18/C2IND/RPG8/PMA3/RG8	A45	RPD9/RD9
A9	AN19/C2INC/RPG9/PMA2/RG9	A46	RPD11/PMCS1/RD11
A10	VDD	A47	SOSCI/IPC13/RC13
A11	RPE8/RE8	A48	VDD
A12	AN5/C1INA/RPB5/VBUSON/RB5	A49	No Connect
A13	PGED3/AN3/C2INA/RPB3/RB3	A50	No Connect
A14	VDD	A51	No Connect
A15	PGEC1/AN1/RPB1/CTED12/RB1	A52	AN24/RPD1/RD1
A16	No Connect	A53	AN26/RPD3/RD3
A17	No Connect	A54	PMD13/RD13
A18	No Connect	A55	RPD5/PMRD/RD5
A19	No Connect	A56	PMD15/RD7
A20	PGEC2/AN6/RPB6/RB6	A57	No Connect
A21	VREF-/CVREF-/PMA7/RA9	A58	No Connect
A22	AVDD	A59	VDD
A23	AN8/RPB8/CTED10/RB8	A60	RPF1/PMD10/RF1
A24	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	A61	RPG0/PMD8/RG0
A25	Vss	A62	TRD3/CTED8/RA7
A26	TCK/CTED2/RA1	A63	Vss
A27	RPF12/RF12	A64	PMD1/RE1
A28	AN13/PMA10/RB13	A65	TRD1/RG12
A29	AN15/RPB15/OCFB/CTED6/PMA0/RB15	A66	AN20/PMD2/RE2
A30	VDD	A67	AN21/PMD4/RE4
A31	RPD15/RD15	A68	No Connect
A32	RPF5/PMA8/RF5	B1	VDD
A33	No Connect	B2	AN22/RPE5/PMD5/RE5
A34	No Connect	B3	AN27/PMD7/RE7
A35	USBID/RF3	B4	RPC2/RC2
A36	RPF2/RF2	B5	RPC4/CTED7/RC4
A37	VBus	B6	AN17/C1INC/RPG7/PMA4/RG7

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select"** for restrictions.
 - 2: Every I/O port pin (RAX-RGx) can be used as a change notification pin (CNAX-CNGx). See **Section 12.0 "I/O Ports"** for more information.
 - 3: Shaded package bumps are 5V tolerant.
 - 4: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
CTED4	22	33	B19	I	ST	CTMU External Edge Input 4
CTED5	29	43	B24	I	ST	CTMU External Edge Input 5
CTED6	30	44	A29	I	ST	CTMU External Edge Input 6
CTED7	—	9	B5	I	ST	CTMU External Edge Input 7
CTED8	—	92	A62	I	ST	CTMU External Edge Input 8
CTED9	—	60	A40	I	ST	CTMU External Edge Input 9
CTED10	21	32	A23	I	ST	CTMU External Edge Input 10
CTED11	23	34	A24	I	ST	CTMU External Edge Input 11
CTED12	15	24	A15	I	ST	CTMU External Edge Input 12
CTED13	14	23	B13	I	ST	CTMU External Edge Input 13
MCLR	7	13	B7	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	19	30	A22	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	B18	P	P	Ground reference for analog modules
VDD	10, 26, 38, 57	2, 16, 37, 46, 62, 86	B1, A10, A14, B21, A30, A41, A48, A59, B53	P	—	Positive supply for peripheral logic and I/O pins
VCAP	56	85	B48	P	—	Capacitor for Internal Voltage Regulator
VSS	9, 25, 41	15, 36, 45, 65, 75	A3, B8, B12, A25, B25, A43, B41, A63	P	—	Ground reference for logic and I/O pins
VREF+	16	29	B17	I	Analog	Analog Voltage Reference (High) Input
VREF-	15	28	A21	I	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = TTL input buffer

Note 1: This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices.

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2.8.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- C_{IN} = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- C_{OUT} = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e., 12 mm length) = 2.5 pF

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION

Crystal manufacturer recommended: $C1 = C2 = 15 \text{ pF}$

Therefore:

$$\begin{aligned} C_{LOAD} &= \{ ([C_{IN} + C1] * [C_{OUT} + C2]) / [C_{IN} + C1 + C2 + C_{OUT}] \} \\ &\quad + \text{estimated oscillator PCB stray capacitance} \\ &= \{ ([5 + 15][5 + 15]) / [5 + 15 + 15 + 5] \} + 2.5 \text{ pF} \\ &= \{ ([20][20]) / [40] \} + 2.5 \\ &= 10 + 2.5 = 12.5 \text{ pF} \end{aligned}$$

Rounded to the nearest standard value or 13 pF in this example for Primary Oscillator crystals "C1" and "C2".

The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

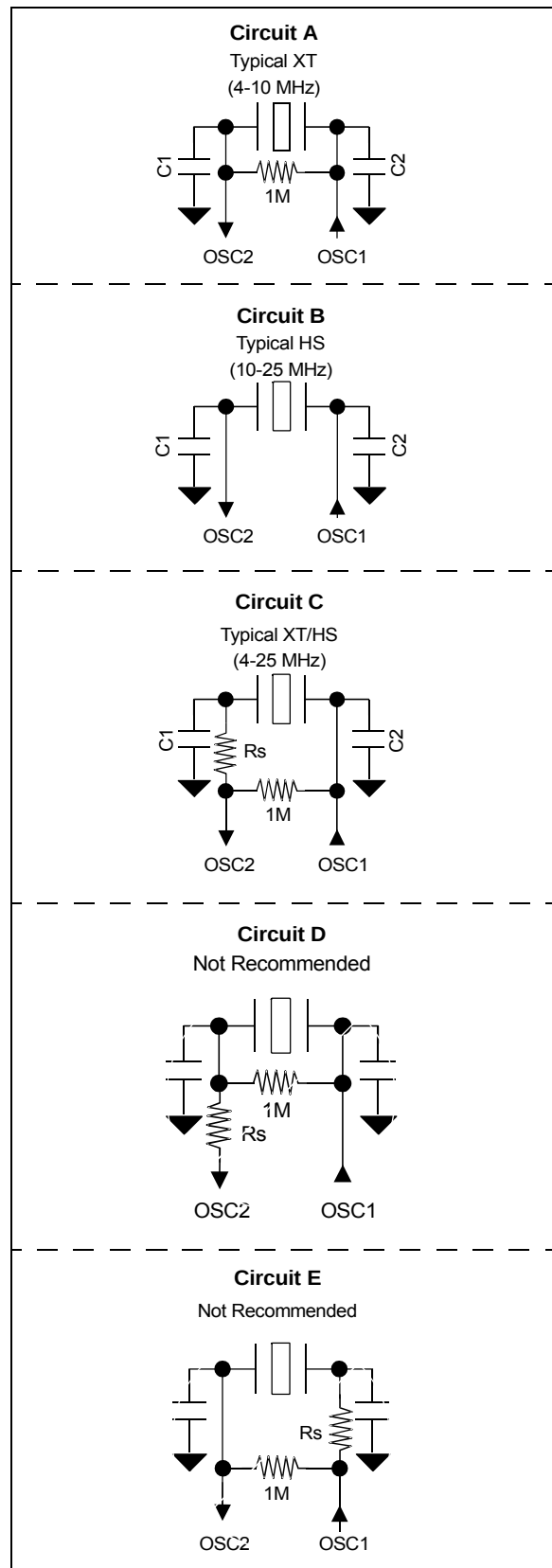
- Select a crystal with a lower "minimum" power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing "ESR" rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.

Note: Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, R_S , as shown in circuit "C" in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to $\sim V_{DD} - 0.6V$. When measuring the oscillator signal you must use a FET scope probe or a probe with $\leq 1.5 \text{ pF}$ or the scope probe itself will unduly change the gain and peak-to-peak levels.

2.8.1.1 Additional Microchip References

- AN588 "PICmicro® Microcontroller Oscillator Design Guide"
- AN826 "Crystal Oscillator Basics and Crystal Selection for rPIC™ and PICmicro® Devices"
- AN849 "Basic PICmicro® Oscillator Design"

FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS



PIC32MX330/350/370/430/450/470

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)

- bit 9-8 **IS1<1:0>**: Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0
- bit 7-5 **Unimplemented**: Read as '0'
- bit 4-2 **IP0<2:0>**: Interrupt Priority bits
111 = Interrupt priority is 7
.
.
.
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled
- bit 1-0 **IS0<1:0>**: Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.
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TABLE 11-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.
- 2: This register does not have associated SET and INV registers.
- 3: This register does not have associated CLR, SET and INV registers.
- 4: Reset value for this bit is undefined.

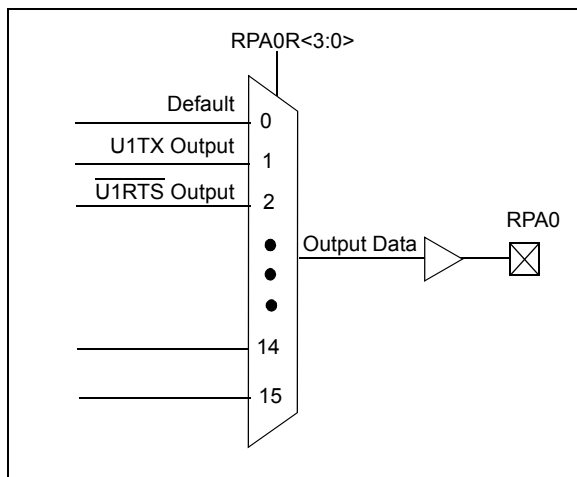
PIC32MX330/350/370/430/450/470

12.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPNR registers (Register 12-2) are used to control output mapping. Like the *[pin name]R* registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 12-2 and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPA0



12.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

12.3.6.1 Control Register Lock

Under normal operation, writes to the RPNR and *[pin name]R* registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

12.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPNR and *[pin name]R* registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

12.4 Control Registers

TABLE 12-3: PORTA REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, PIC32MX370F512L, PIC32MX430F064L, PIC32MX450F128L, PIC32MX450F256L, AND PIC32MX470F512L DEVICES ONLY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	ANSELA10	ANSELA9	—	—	—	—	—	—	—	—	—	0060
6010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	xxxx
6020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	—	—	RA10	RA9	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
6030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	—	—	ODCA10	ODCA9	—	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	xxxx
6050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUA15	CNPUA14	—	—	—	CNPUA10	CNPUA9	—	CNPUA7	CNPUA6	CNPUA5	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	xxxx
6060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDA15	CNPDA14	—	—	—	CNPDA10	CNPDA9	—	CNPDA7	CNPDA6	CNPDA5	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	xxxx
6070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEA15	CNIEA14	—	—	—	CNIEA10	CNIEA9	—	CNIEA7	CNIEA6	CNIEA5	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	xxxx
6090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATA15	CN STATA14	—	—	—	CN STATA10	CN STATA9	—	CN STATA7	CN STATA6	CN STATA5	CN STATA4	CN STATA3	CN STATA2	CN STATA1	CN STATA0	xxxx

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 12-8: PORTD REGISTER MAP FOR PIC32MX330F064H, PIC32MX350F128H, PIC32MX350F256H, PIC32MX370F512H, PIC32MX430F064H, PIC32MX450F128H, PIC32MX450F256H, PIC32MX470F512H DEVICES ONLY

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	ANSELD3	ANSELD2	ANSELD1	—	000E
6310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	xxxx
5320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
6330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
6340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	xxxx
6350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	xxxx
6360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	xxxx
6370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	xxxx
6390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CN STATD11	CN STATD10	CN STATD9	CN STATD8	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	xxxx

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 12-10: PORTE REGISTER MAP FOR PIC32MX330F064H, PIC32MX350F128H, PIC32MX350F256H, PIC32MX370F512H, PIC32MX430F064H, PIC32MX450F128H, PIC32MX450F256H, AND PIC32MX470F512H DEVICES ONLY

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ANSELE7	ANSELE6	ANSELE5	ANSELE4	—	ANSELE2	—	—	00F4
6410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	xxxx
6420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6440	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	xxxx
6450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPDE3	CNPUE2	CNPUE1	CNPUE0	xxxx
6460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	xxxx
6470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNIEE7	CNIEE6	CNIEE5	CNIEE4	CNIEE3	CNIEE2	CNIEE1	CNIEE0	xxxx
6490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	xxxx

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

15.0 WATCHDOG TIMER (WDT)

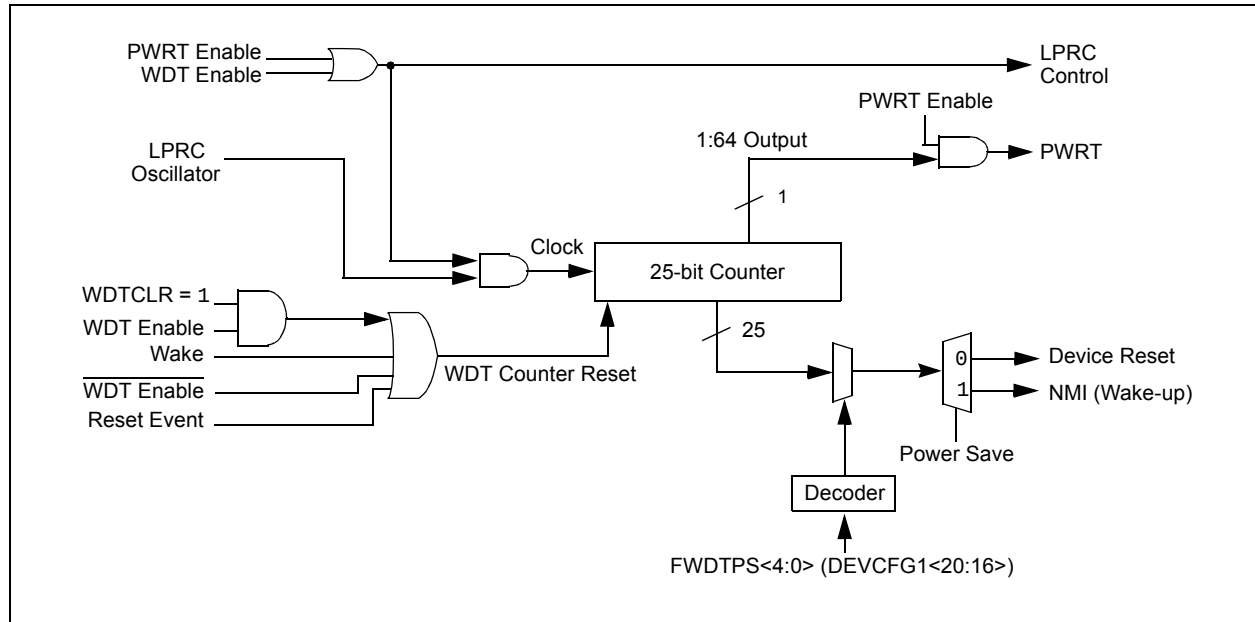
Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog, Deadman, and Power-up Timers”** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 15-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM



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REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON ^(1,2)	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	—	SWDTPS<4:0>					WDTWINEN	WDTCLR

Legend:	y = Values set from Configuration bits on POR
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit^(1,2)

1 = Enables the WDT if it is not enabled by the device configuration

0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits

On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit

1 = Enable windowed Watchdog Timer

0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit

1 = Writing a '1' will clear the WDT

0 = Software cannot force this bit to a '0'

Note 1: A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.

Note 2: When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

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NOTES:

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REGISTER 18-3: SPIxSTAT: SPI STATUS REGISTER (CONTINUED)

- bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit
1 = Transmit not yet started, SPITXB is full
0 = Transmit buffer is not full
Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPIxSR.
Enhanced Buffer Mode:
Set when CWPTR + 1 = SRPTR; cleared otherwise
- bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB is full
0 = Receive buffer, SPIxRXB is not full
Standard Buffer Mode:
Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer Mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise

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REGISTER 21-4: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<15:14> ⁽¹⁾		PTEN<13:8>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<7:2>						PTEN<1:0> ⁽²⁾	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Write '0'; ignore read

bit 15-14 **PTEN<15:14>:** PMCSx Address Port Enable bits

1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1⁽¹⁾

0 = PMA15 and PMA14 function as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits

1 = PMA<13:2> function as PMP address lines

0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits

1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL⁽²⁾

0 = PMA1 and PMA0 pads function as port I/O

Note 1: The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

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REGISTER 22-4: RTCDATE: RTC DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<3:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **YEAR10<3:0>**: Binary-Coded Decimal Value of Years bits, 10s place digits

bit 27-24 **YEAR01<3:0>**: Binary-Coded Decimal Value of Years bits, 1s place digit

bit 23-20 **MONTH10<3:0>**: Binary-Coded Decimal Value of Months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>**: Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>**: Binary-Coded Decimal Value of Days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>**: Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **WDAY01<3:0>**: Binary-Coded Decimal Value of Weekdays bits, 1s place digit; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

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REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 2-0 **FPLLIDIV<2:0>**: PLL Input Divider bits

111 = 12x divider

110 = 10x divider

101 = 6x divider

100 = 5x divider

011 = 4x divider

010 = 3x divider

001 = 2x divider

000 = 1x divider

Note 1: This bit is available on PIC32MX4XX devices only.

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FIGURE 31-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS

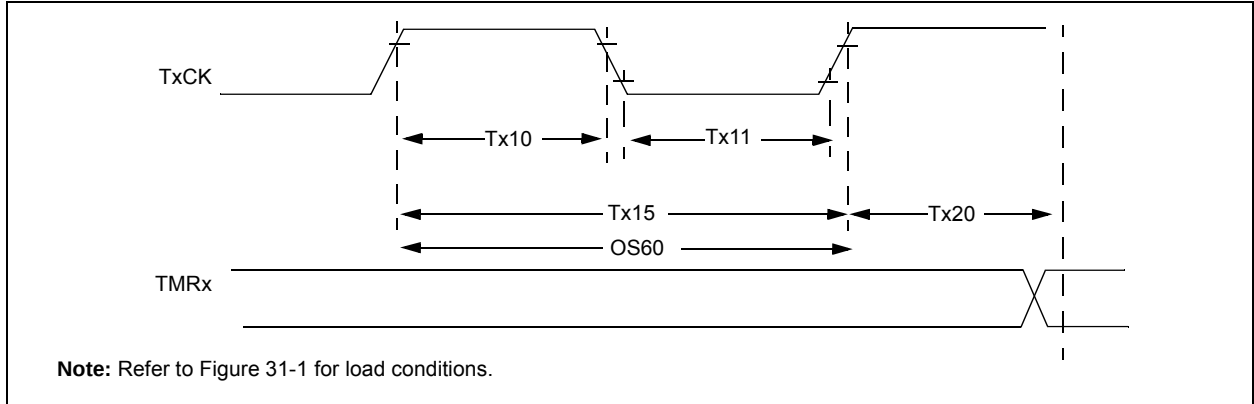


TABLE 31-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics ⁽²⁾		Min.	Typical	Max.	Units	Conditions
TA10	TtxH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TtxL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TtxP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 ns or 2 TPB)/N] + 30 ns	—	—	ns	VDD > 2.7V
				[(Greater of 25 ns or 2 TPB)/N] + 50 ns	—	—	ns	VDD < 2.7V
		Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V (Note 3)	
			50	—	—	ns	VDD < 2.7V (Note 3)	
OS60	Ft1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	100	kHz	—
TA20	TckEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPB	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

FIGURE 31-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

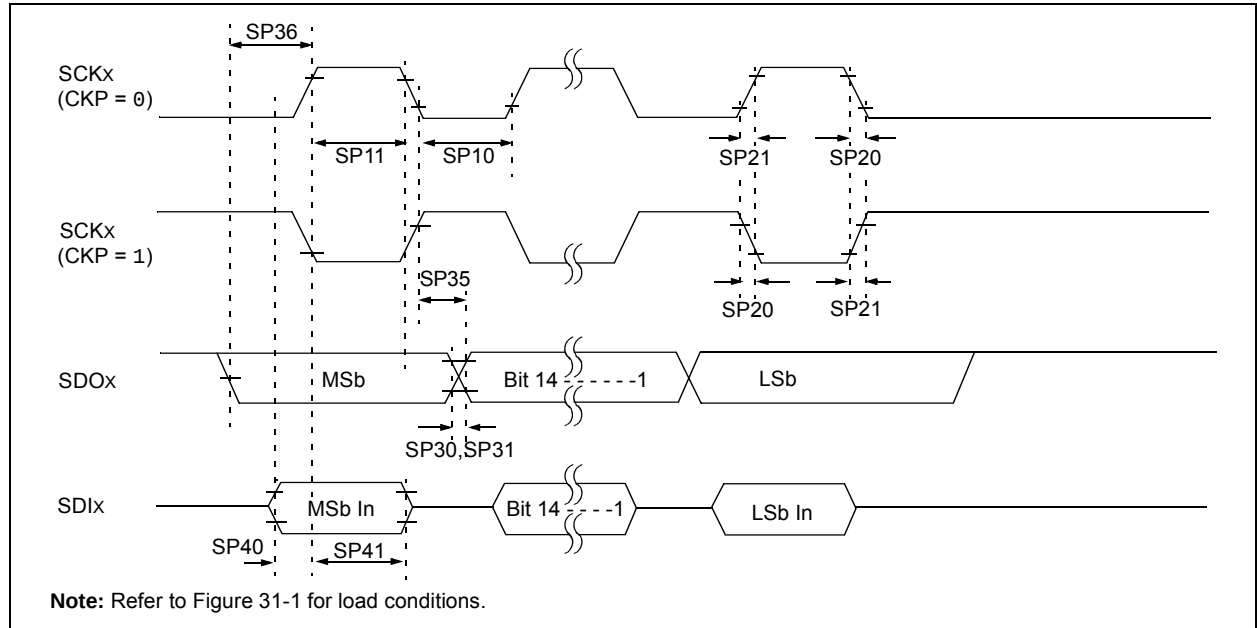


TABLE 31-30: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TsCL	SCKx Output Low Time (Note 3)	TsCK/2	—	—	ns	—
SP11	TsCH	SCKx Output High Time (Note 3)	TsCK/2	—	—	ns	—
SP20	TsCF	SCKx Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP21	TsCR	SCKx Output Rise Time (Note 4)	—	—	—	ns	See parameter DO32
SP30	TDoF	SDOx Data Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP31	TDoR	SDOx Data Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP35	TsCH2DoV, TsCL2DoV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP36	TDoV2sc, TDoV2scL	SDOx Data Output Setup to First SCKx Edge	15	—	—	ns	—
SP40	TDiV2sch, TDiV2scL	Setup Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V
SP41	TsCH2DiL, TsCL2DiL	Hold Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

Note 2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Note 3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

Note 4: Assumes 50 pF load on all SPIx pins.

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TABLE 31-37: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

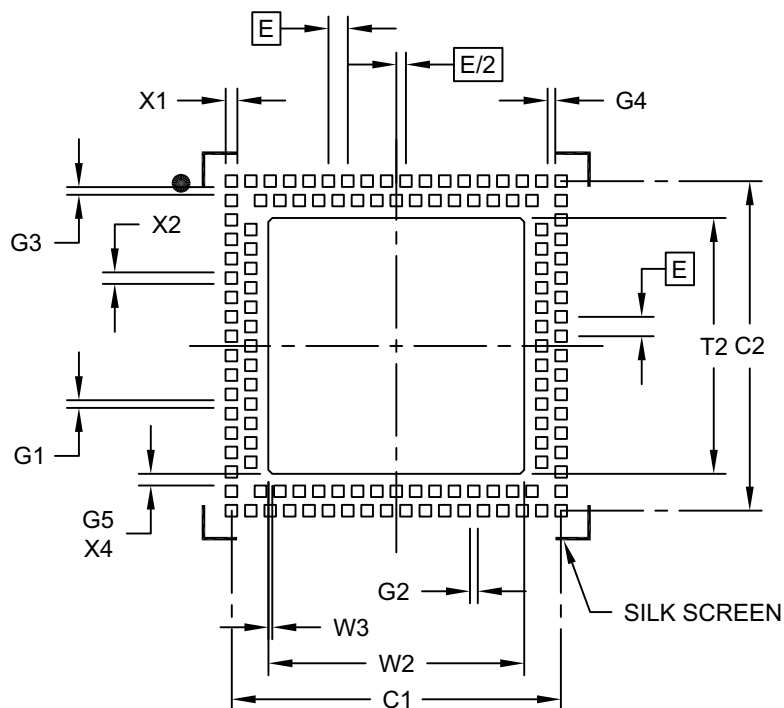
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period ⁽²⁾	65	—	—	ns	See Table 31-36
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed) ⁽⁴⁾	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	2 TAD	—	—	—	—
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽³⁾	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽³⁾	—	—	2	μs	—

- Note 1:** These parameters are characterized, but not tested in manufacturing.
2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.
3: Characterized by design but not tested.
4: Refer to Table 31-36 for detailed conditions.

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124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
		MIN	NOM	MAX
Dimension Limits				
Contact Pitch	E	0.50 BSC		
Pad Clearance	G1	0.20		
Pad Clearance	G2	0.20		
Pad Clearance	G3	0.20		
Pad Clearance	G4	0.20		
Contact to Center Pad Clearance (X4)	G5	0.30		
Optional Center Pad Width	T2			6.60
Optional Center Pad Length	W2			6.60
Optional Center Pad Chamfer (X4)	W3		0.10	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X124)	X1			0.30
Contact Pad Length (X124)	X2			0.30

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A