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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx370f512h-v-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 4: PIN NAMES FOR 100-PIN DEVICES (CONTINUED)

			· · · · · · · · · · · · · · · · · · ·
10	0-PIN TQFP (TOP VIEW) ^(1,2,3)		
	PIC32MX330F064L PIC32MX350F128L PIC32MX350F256L PIC32MX370F512L		
			100 1
Pin #	Full Pin Name	Pin #	Full Pin Name
71	RPD11/PMCS1/RD11	86	Vdd
72	RPD0/RD0	87	RPF0/PMD11/RF0
73	SOSCI/RPC13/RC13	88	RPF1/PMD10/RF1
74	SOSCO/RPC14/T1CK/RC14	89	RPG1/PMD9/RG1
75	Vss	90	RPG0/PMD8/RG0
76	AN24/RPD1/RD1	91	TRCLK/RA6
77	AN25/RPD2/RD2	92	TRD3/CTED8/RA7
78	AN26/RPD3/RD3	93	PMD0/RE0
79	RPD12/PMD12/RD12	94	PMD1/RE1
80	PMD13/RD13	95	TRD2/RG14
81	RPD4/PMWR/RD4	96	TRD1/RG12
82	RPD5/PMRD/RD5	97	TRD0/RG13
83	PMD14/RD6	98	AN20/PMD2/RE2
84	PMD15/RD7	99	RPE3/CTPLS/PMD3/RE3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 12.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RGx), with the exception of RF6, can be used as a change notification pin (CNAx-CNGx). See Section 12.0 "I/O Ports" for more information.

3: RPF6 (pin 55) and RPF7 (pin 54) are only remappable for input functions.

TABLE 6: PIN NAMES FOR 124-PIN DEVICES

		-				
124	-PIN VTLA (BOTTOM VIEW) ^(1,2,3,4,5)				A3	4
	`		D 40	B29		
			B13	220		Conductive
						Thermal Pad
			B1		B41	
			E	856		A51
	FIG3ZWIAS/UF31ZL	A1				
			,	69		
	Polarity I	ndicator		100		
Package Bump #	Full Pin Name	Package Bump #			Full Pin	Name
A1	No Connect	A38	SDA1	/RG3		
A2	RG15	A39	SCL2/	'RA2		
A3	Vss	A40	TDI/C	TED9/RA4		
A4	AN23/PMD6/RE6	A41	Vdd			
A5	RPC1/RC1	A42	OSC2	/CLKO/RC1	5	
A6	RPC3/RC3	A43	Vss			
A7	AN16/C1IND/RPG6/SCK2/PMA5/RG6	A44	RPA1	5/RA15		
A8	AN18/C2IND/RPG8/PMA3/RG8	A45	RPD9	/RD9		
A9	AN19/C2INC/RPG9/PMA2/RG9	A46	RPD1	1/PMCS1/R	D11	
A10	VDD	A47	SOSC	I/RPC13/RC	C13	
A11	RPE8/RE8	A48	Vdd			
A12	AN5/C1INA/RPB5/RB5	A49	No Co	nnect		
A13	PGED3/AN3/C2INA/RPB3/RB3	A50	No Co	nnect		
A14	VDD	A51	No Co	nnect		
A15	PGEC1/AN1/RPB1/CTED12/RB1	A52	AN24/	RPD1/RD1		
A16	No Connect	A53	AN26/	RPD3/RD3		
A17	No Connect	A54	PMD1	3/RD13		
A18	No Connect	A55	RPD5	PMRD/RD5	5	
A19	No Connect	A56	PMD1	5/RD7		
A20	PGEC2/AN6/RPB6/RB6	A57	No Co	nnect		
A21	VREF-/CVREF-/PMA7/RA9	A58	No Co	nnect		
A22	AVDD	A59	VDD			
A23	AN8/RPB8/CTED10/RB8	A60	RPF1/	PMD10/RF	1	
A24	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	A61	RPG0	/PMD8/RG0)	
A25	Vss	A62	TRD3	CTED8/RA	7	
A26	TCK/CTED2/RA1	A63	Vss			
A27	RPF12/RF12	A64	PMD1	/RE1		
A28	AN13/PMA10/RB13	A65	TRD1	/RG12		
A29	AN15/RPB15/OCFB/CTED6/PMA0/RB15	A66	AN20/	PMD2/RE2		
A30	VDD	A67	AN21/	PMD4/RE4		
A31	RPD15/RD15	A68	No Co	nnect		
A32	RPF5/PMA8/RF5	B1	Vdd			
A33	No Connect	B2	AN22/	RPE5/PMD	5/RE5	
A34	No Connect	B3	AN27/	PMD7/RE7		
A35	RPF3/RF3	B4	RPC2	/RC2		
A36	RPF2/RF2	B5	RPC4	/CTED7/RC	4	
A37	RPF7/RF7	B6	AN17/	C1INC/RPG	7/PMA4/RG	7

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 12.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RGx), with the exception of RF6, can be used as a change notification pin (CNAx-CNGx). See Section 12.0 "I/O Ports" for more information.

3: RPF6 (bump B30) and RPF7 (bump A37) are only remappable for input functions.

4: Shaded package bumps are 5V tolerant.

5: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial ProgrammingTM (ICSPTM) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB[®] ICD 3 or MPLAB REAL ICE[™].

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- "Using MPLAB[®] ICD 3" (poster) DS50001765
- "MPLAB[®] ICD 3 Design Advisory" DS50001764
- "MPLAB[®] REAL ICE™ In-Circuit Debugger User's Guide" DS50001616
- *"Using MPLAB[®] REAL ICE™ Emulator"* (poster) DS50001749

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

2.7 Trace

The trace pins can be connected to a hardware trace-enabled programmer to provide a compressed real-time instruction trace. When used for trace, the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 31. "Direct Memory Access (DMA) Controller" (DS60001117), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, etc.) or memory itself.

Following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
 - Auto-increment source and destination address registers
 - Source and destination pointers
 - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
 - Transfer granularity, down to byte level
 - Bytes need not be word-aligned at source and destination

- Fixed priority channel arbitration
- · Flexible DMA channel operating modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- · Flexible DMA requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA debug support features:
 - Most recent address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- · CRC Generation module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable



FIGURE 10-1: DMA BLOCK DIAGRAM

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	_	—	—	—	_	_	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
					RDWR	DMACH<2:0>		

REGISTER 10-2: DMASTAT: DMA STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 Unimplemented: Read as '0'

- bit 3 RDWR: Read/Write Status bit
 - 1 = Last DMA bus access was a read
 - 0 = Last DMA bus access was a write
- bit 2-0 **DMACH<2:0>:** DMA Channel bits These bits contain the value of the most recent active DMA channel.

REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
01.04	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
31:24				DMAADDF	<31:24>				
00.40	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
23:10	DMAADDR<23:16>								
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
15:8	DMAADDR<15:8>								
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
7:0				DMAADD	R<7:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 DMAADDR<31:0>: DMA Module Address bits

These bits contain the address of the most recent DMA access.

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 6 **CRCAPP:** CRC Append Mode bit⁽¹⁾

- 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
- 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5 **CRCTYP:** CRC Type Selection bit
 - 1 = The CRC module will calculate an IP header checksum
 - 0 = The CRC module will calculate a LFSR CRC
- bit 4-3 Unimplemented: Read as '0'
- bit 2-0 CRCCH<2:0>: CRC Channel Select bits
 - 111 = CRC is assigned to Channel 7
 - 110 = CRC is assigned to Channel 6
 - 101 = CRC is assigned to Channel 5
 - 100 = CRC is assigned to Channel 4
 - 011 = CRC is assigned to Channel 3
 - 010 = CRC is assigned to Channel 2
 - 001 = CRC is assigned to Channel 1
 - 000 = CRC is assigned to Channel 0
- **Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		—	_	_	—	_	_	_
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	_	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24	Unimplemented: Read as '0'
bit 23	CHSDIE: Channel Source Done Interrupt Enable bit
	1 = Interrupt is enabled
1.11.00	
bit 22	CHSHIE: Channel Source Half Empty Interrupt Enable bit
	1 = Interrupt is enabled 0 = Interrupt is disabled
bit 21	CHDDIE: Channel Destination Done Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 20	CHDHIE: Channel Destination Half Full Interrupt Enable bit
	1 = Interrupt is enabled
h:+ 40	0 = Interrupt is disabled
DIT 19	
	0 = Interrupt is disabled
bit 18	CHCCIE: Channel Cell Transfer Complete Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 17	CHTAIE: Channel Transfer Abort Interrupt Enable bit
	1 = Interrupt is enabled
bit 16	0 – Interrupt is disabled
DIL TO	
	0 = Interrupt is disabled
bit 15-8	Unimplemented: Read as '0'
bit 7	CHSDIF: Channel Source Done Interrupt Flag bit
	1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
	0 = No interrupt is pending
bit 6	CHSHIF: Channel Source Half Empty Interrupt Flag bit
	 1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2) 0 = No interrupt is pending
bit 5	CHDDIF: Channel Destination Done Interrupt Flag bit
	1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ
	0 = No interrupt is pending
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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
	UTEYE	UOEMON		USBSIDL			_	UASUSPND

REGISTER 11-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 UTEYE: USB Eye-Pattern Test Enable bit

- 1 = Eye-Pattern Test is enabled
- 0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB OE Monitor Enable bit

1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving
 0 = OE signal is inactive

bit 5 Unimplemented: Read as '0'

- bit 4 USBSIDL: Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode

bit 3-1 Unimplemented: Read as '0'

bit 0 UASUSPND: Automatic Suspend Enable bit

- 1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 11-5.
- 0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

TABLE 12-6: PORTC REGISTER MAP FOR PIC32MX330F064H, PIC32MX350F128H, PIC32MX350F256H, PIC32MX370F512H, PIC32MX430F064H, PIC32MX450F128H, PIC32MX450F256H, AND PIC32MX470F512H DEVICES ONLY

ess		6								Bits									
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6210	TRISC	31:16	_	_	—	_		—	_		_			_	_		_		0000
0210	TRISC	15:0	TRISC15	TRISC14	TRISC13	TRISC12	_	—	—	—	—	_	_	_	_	_	_	_	xxxx
6220	PORTO	31:16	_	_	_	_	_	—	_	—	_	_	_	_	_	—	_	_	0000
0220	TORIC	15:0	RC15	RC14	RC13	RC12	_	—	_	—	—		_	_	_	—			xxxx
6230	LATC	31:16	—	_	_	_	_	—	_	—	—		_	_	_	—			0000
0200	LATO	15:0	LATC15	LATC14	LATC13	LATC12	_	—	—	—	—	—	—	—	—		_	_	xxxx
6240	ODCC	31:16	—	—	—	—	—	—	—	—	—	_	—	—	—	—	—	_	0000
02.0	0200	15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	_	—	—	_	—	—	—	_		_	xxxx
6250	CNPUC	31:16	_	_	—	_		—	_		_							_	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	_		—	—	—	—			XXXX
6260	CNPDC	31:16	_	_		_	—	—	—	—	_	—	—	—	—	—	—	_	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	_	—	_	_	_	—	—	—	—	_	XXXX
6270	CNCONC	31:16	_			—	—	—	_		—	_	—	—	—	_	—	—	0000
		15:0	ON		SIDL	—	—	—	_		—	_	—	—	—	_	—	—	0000
6280	CNENC	31:16					—	—	_		—	_	—	—	—	_	—	—	0000
		15:0	CNIEC15	CNIEC14	CNIEC13	CNIEC12	—	—	_		_	_	—	—	—		_	_	xxxx
6290	CNSTATC	31:16	_	—		_	—	—	_		_	_	—	—	—		_	_	0000
	-	15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

		U																	
ess										Bi	ts								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6510	TRISE	31:16	_	_	—	—			-										0000
00.0		15:0	—	_	TRISF13	TRISF12	_	_	_	TRISF8	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	xxxx
6520	PORTE	31:16	—	_	—	—	—	_	_	—	—	—	—	—	—	—	—	—	0000
0020	1 OIGH	15:0	—	_	RF13	RF12	_	_		RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6530		31:16	—			—		_			_	—			—	—			0000
0000	D.(II	15:0	—	_	LATF13	LATF12	—	—	—	LATF8	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6540	ODCE	31:16	—	_	—	—	_	-	-	—	-	—	—	-	—	—	—	—	0000
0040	ODOI	15:0	_	_	ODCF13	ODCF12	-	_	_	ODCF8	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	xxxx
6550		31:16	_		_	_				_		_	_		_	_	_	_	0000
0550	CINFUI	15:0	_		CNPUF13	CNPUF12				CNPUF8	CNPUF7	CNPUF6	CNPUF5	CNPUF4	CNPDF3	CNPUF2	CNPUF1	CNPUF0	xxxx
6560		31:16	_	_	—	—	-	_	_	—	_	—	—	_	—	—	_	—	0000
0000		15:0	_	_	CNPDF13	CNPDF12	-	_	_	CNPDF8	CNPDF7	CNPDF6	CNPDF5	CNPDF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	xxxx
6570		31:16	_		_	—				_		_	_		_	_	_	_	0000
0370	CINCOIN	15:0	ON		SIDL	_				_		_	_		_	_	_	_	0000
6500	CNENE	31:16		-	—	—		-	_	—		—	—	_	—	—	—	_	0000
0500	CINEINF	15:0	—	—	CNIEF13	CNIEF12	—	_	_	CNIEF8	CNIEF7	_	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	xxxx
		31:16	_	—	_	_	_	_	_	—	_	_	—	—	_	_	_	_	0000
6590	CNSTATF	15:0	_	_	CN STATF13	CN STATF12	_	_	_	CN STATF8	CN STATF7	—	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	xxxx

TABLE 12-11: PORTF REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, AND PIC32MX370F512L DEVICES

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

TABLE 12-16:PORTG REGISTER MAP FOR PIC32MX330F064H, PIC32MX350F128H, PIC32MX350F256H, PIC32MX370F512H,
PIC32MX430F064H, PIC32MX450F128H, PIC32MX450F256H, AND PIC32MX470F512H DEVICES ONLY

ess		a a								Bi	its								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6600	ANSELG	31:16		—	—	—	—	_	—	_	-	—	—	_	_	—	—	_	0000
	/	15:0	—	—	—	-	—	—	ANSELG9	ANSELG8	ANSELG7	ANSELG6	—	_	—	—	—	-	01C0
6610	TRISG	31:16	_	_	—	_	_		—	_	_	—	_	_		—	_		0000
		15:0		_	—	_	—	_	TRISG9	TRISG8	TRISG7	TRISG6	_	_	TRISG3	TRISG2	—		xxxx
6620	PORTG	31:16		_	—	_	—	_	—	-	—	—	_	_	—	—	—		0000
		15:0	_	—	—	_	—	—	RG9	RG8	RG7	RG6	—	_	RG3 ⁽²⁾	RG2 ⁽²⁾	—		xxxx
6630	LATG	31:16	_	—	—	_	—	—	—		—	—	—	_	—	—	—		0000
	EATO	15:0	_	—	—	_	—	—	LATG9	LATG8	LATG7	LATG6	—	_	LATG3	LATG2	—		xxxx
6640	ODCG	31:16	—	—	—	-	—	—	—	-	—	—	—	_	—	—	—	-	0000
00.0	0200	15:0	—	—	—	-	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	_	ODCG3	ODCG2	—	-	xxxx
6650	CNPUG	31:16	—	—	—	-	—	—	—	-	—	—	—	_	—	—	—	-	0000
	0.1.00	15:0	—	—	—	-	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	_	CNPUG3	CNPUG2	—	-	xxxx
6660	CNPDG	31:16	—	—	—	-	—	—	—	-	—	—	—	_	—	—	—	-	0000
	0.1. 20	15:0	—	—	—	-	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	_	CNPDG3	CNPDG2	—	-	xxxx
6670	CNCONG	31:16	—	—	—	-	—	—	—	-	_	—	—	_	—	—	—	-	0000
0070	onconc	15:0	ON	—	SIDL	—	—	—	—	—	_	—	—	_	—	—	—	—	0000
6680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	—	0000
0000	GILLING	15:0	—		—	_	—		CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	_	CNIEG3	CNIEG2	—	—	xxxx
		31:16	_	—	—	_	—		—	—	—	—	_	_		—	—	—	0000
6690	CNSTATG	15:0	_	_	—	_	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	_	_	CN STATG3	CN STATG2	_	—	xxxx

Legend: x = Unknown value on Reset; - = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

2: This bit is only available on devices without a USB module.

PIC32MX330/350/370/430/450/470

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
15:0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
10.0	ON ^(1,3)	—	SIDL ⁽⁴⁾	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
7:0	TGATE ⁽³⁾	Т	CKPS<2:0>(3)	T32 ⁽²⁾	—	TCS ⁽³⁾	—

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

- bit 15 **ON:** Timer On bit^(1,3)
 - 1 = Module is enabled
 - 0 = Module is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 SIDL: Stop in Idle Mode bit⁽⁴⁾
 - 1 = Discontinue operation when device enters Idle mode0 = Continue operation even in Idle mode

bit 12-8 Unimplemented: Read as '0'

- bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽³⁾
 - When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6-4 TCKPS<2:0>: Timer Input Clock Prescale Select bits⁽³⁾

- 111 = 1:256 prescale value
- 110 = 1:64 prescale value
- 101 = 1:32 prescale value
- 100 = 1:16 prescale value
- 011 = 1:8 prescale value
- 010 = 1:4 prescale value
- 001 = 1:2 prescale value
- 000 = 1:1 prescale value
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.
 - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

NOTES:

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0						
31.24	—	—	—	—	—	—	—	
22:16	U-0	U-0						
23:10	—	—	—	—	—	—	—	-
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	F	ORM<2:0>	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
7:0		SSRC<2:0>		CLRASAM		ASAM	SAMP ⁽²⁾	DONE ⁽³⁾

REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1

Legend:

bit 14

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** ADC Operating Mode bit⁽¹⁾
 - 1 = ADC module is operating
 - 0 = ADC module is not operating
 - Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode
- bit 12-11 Unimplemented: Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits

- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd ddd0 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INTO pin ends sampling and starts conversion
- 000 = Clearing SAMP bit ends sampling and starts conversion
- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ 0, this bit is automatically cleared by hardware to end sampling and start conversion.
 - 3: This bit is automatically set by hardware when ADC is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

	ER 20-1. CTMOCON. CTMO CONTROL REGISTER (CONTINUE
bit 24	EDG1STAT: Edge 1 Status bit
	Indicates the status of Edge 1 and can be written to control edge source
	1 = Edge 1 has occurred
	0 = Edge 1 has not occurred
bit 23	EDG2MOD: Edge 2 Edge Sampling Select bit
	1 = Input is edge-sensitive
h:+ 00	0 = Input is level-sensitive
DIT 22	EDG2POL: Edge 2 Polarity Select bit
	1 = Edge 2 programmed for a positive edge response
h:+ 04 40	0 = Euge z programmed for a negative euge response
DIL 21-18	
	1111 = Reserved
	1110 = C2OOT pin is selected 1101 = C1OUT pin is selected
	1100 = PBCLK clock is selected
	1011 = IC3 Capture Event is selected
	1010 = IC2 Capture Event is selected
	1001 = IC1 Capture Event is selected
	1000 = CTED13 pin is selected
	0111 = CTED12 pin is selected
	0101 = CTED10 pin is selected
	0100 = CTED9 pin is selected
	0011 = CTED1 pin is selected
	0010 = CTED2 pin is selected
	0001 = OC1 Compare Event is selected
	0000 = Timer1 Event is selected
bit 17-16	Unimplemented: Read as '0'
bit 15	ON: ON Enable bit
	1 = Module is enabled
	0 = Module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	CIMUSIDL: Stop in Idle Mode bit
	1 = Discontinue module operation when device enters Idle mode
h:+ 40	0 = Continue module operation in Idle mode
DICIZ	
	1 = Enables edge delay generation
hit 11	EDGEN: Edge Enable bit
	1 - Edges are not blocked
	r = Euges are hound blocked $0 = Edges are blocked$
	bit 24 bit 23 bit 22 bit 21-18 bit 17-16 bit 15 bit 14 bit 13 bit 12 bit 12 bit 11

- **Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 31-42) in Section 31.0 "Electrical Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

30.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers (MCU) and dsPIC[®] digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB[®] X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICkit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

30.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows[®], Linux and Mac OS[®] X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- · Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- · Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window
- Project-Based Workspaces:
- Multiple projects
- Multiple tools
- · Multiple configurations
- · Simultaneous debugging sessions

File History and Bug Tracking:

- · Local file history feature
- Built-in support for Bugzilla issue tracker

30.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- · MPLAB X IDE compatibility

30.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

30.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

30.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

PIC32MX330/350/370/430/450/470



AC CHA	RACTER	ISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$								
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions				
SY00	Τρυ	Power-up Period Internal Voltage Regulator Enabled		400	600	μS					
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	_	1 μs + 8 SYSCLK cycles		_	_				
SY20	TMCLR	MCLR Pulse Width (low)	2			μS	—				
SY30	TBOR	BOR Pulse Width (low)		1		μS	—				

TABLE 31-23: RESETS TIMING

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	Ν	/ILLIMETER	S
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.50 BSC	
Pad Clearance	G1	0.20		
Pad Clearance	G2	0.20		
Pad Clearance	G3	0.20		
Pad Clearance	G4	0.20		
Contact to Center Pad Clearance (X4)	G5	0.30		
Optional Center Pad Width	T2			6.60
Optional Center Pad Length	W2			6.60
Optional Center Pad Chamfer (X4)	W3		0.10	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X124)	X1			0.30
Contact Pad Length (X124)	X2			0.30

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A