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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx370f512l-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 μ F to 47 μ F. This capacitor should be located as close to the device as possible.

2.3 Capacitor on Internal Voltage Regulator (VCAP)

2.3.1 INTERNAL REGULATOR MODE

A low-ESR (3 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 31.0 "Electrical Characteristics"** for additional information on CEFC specifications.

2.4 Master Clear (MCLR) Pin

The $\overline{\text{MCLR}}$ pin provides two specific device functions:

- Device Reset
- Device programming and debugging

Pulling The $\overline{\text{MCLR}}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{\text{MCLR}}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.



EXAMPLE OF MCLR PIN CONNECTIONS



No pull-ups or bypass capacitors are allowed on

active debug/program PGECx/PGEDx pins.

Reset period during POR.

3:

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2.** "CPU" (DS60001113), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). Resources for the MIPS32[®] M4K[®] Processor Core are available at http://www.imgtec.com.

The the MIPS32[®] M4K[®] Processor Core is the heart of the PIC32MX330/350/370/430/450/470 device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

3.1 Features

- 5-stage pipeline
- · 32-bit address and data paths
- MIPS32[®] Enhanced Architecture (Release 2):
 - Multiply-accumulate and multiply-subtract instructions
 - Targeted multiply instruction
 - Zero/One detect instructions
 - WAIT instruction
 - Conditional move instructions (MOVN, MOVZ)
 - Vectored interrupts
 - Programmable exception vector base
 - Atomic interrupt enable/disable
 - GPR shadow registers to minimize latency for interrupt handlers
 - Bit field manipulation instructions

- MIPS16e[®] Code Compression:
 - 16-bit encoding of 32-bit instructions to improve code density
 - Special PC-relative instructions for efficient loading of addresses and constants
 - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
 - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) Mechanism:
- Simple Dual Bus Interface:
 - Independent 32-bit address and data buses
 - Transactions can be aborted to improve interrupt latency
- Autonomous Multiply/Divide Unit (MDU):
 - Maximum issue rate of one 32x16 multiply per clock
 - Maximum issue rate of one 32x32 multiply every other clock
 - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (*rs*) sign extension-dependent)
- · Power Control:
 - Minimum frequency: 0 MHz
 - Low-Power mode (triggered by WAIT instruction)
 - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace:
 - Support for single stepping
 - Virtual instruction and data address/value
 - Breakpoints



Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

Exception	Description
Reset	Assertion MCLR or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Вр	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

TABLE 3-3: MIPS32[®] M4K[®] PROCESSOR CORE EXCEPTION TYPES

3.3 Power Management

The MIPS[®] M4K[®] processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see Section 27.0 "Power-Saving Features".

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX330/350/370/430/450/470 family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The MIPS[®] M4K[®] processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K[®] core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	HVDR	—	—	—	—	—
22.16	U-0	U-0						
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
10.0	—	—	—	—	—	—	CMR	VREGS
7.0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
7.0	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR ⁽¹⁾	POR ⁽¹⁾

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Legend:	HS = Set by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

- bit 29 HVDR: High Voltage Detect Reset Flag bit 1 = High Voltage Detect (HVD) Reset has occurred 0 = HVD Reset has not occurred bit 28-10 Unimplemented: Read as '0' bit 9 **CMR:** Configuration Mismatch Reset Flag bit 1 = Configuration mismatch Reset has occurred 0 = Configuration mismatch Reset has not occurred bit 8 VREGS: Voltage Regulator Standby Enable bit 1 = Regulator is enabled and is on during Sleep mode 0 = Regulator is set to Stand-by Tracking mode EXTR: External Reset (MCLR) Pin Flag bit bit 7 1 = Master Clear (pin) Reset has occurred 0 = Master Clear (pin) Reset has not occurred bit 6 SWR: Software Reset Flag bit 1 = Software Reset was executed 0 = Software Reset as not executed bit 5 Unimplemented: Read as '0' bit 4 WDTO: Watchdog Timer Time-out Flag bit 1 = WDT Time-out has occurred 0 = WDT Time-out has not occurred bit 3 **SLEEP:** Wake From Sleep Flag bit 1 = Device was in Sleep mode 0 = Device was not in Sleep mode bit 2 **IDLE:** Wake From Idle Flag bit 1 = Device was in Idle mode 0 = Device was not in Idle mode **BOR:** Brown-out Reset Flag bit⁽¹⁾ bit 1 1 = Brown-out Reset has occurred 0 = Brown-out Reset has not occurred bit 0 **POR:** Power-on Reset Flag bit⁽¹⁾ 1 = Power-on Reset has occurred
 - 0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view next detection.

REGISTER 11-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.9	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	STALLIE	ATTACHIE	RESUMEIE		TDNIE	SOFIE		URSTIE ⁽²⁾
						CONE		DETACHIE ⁽³⁾

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

	-
bit 7	STALLIE: STALL Handshake Interrupt Enable bit
	1 = STALL interrupt is enabled
	0 = STALL interrupt is disabled
bit 6	ATTACHIE: ATTACH Interrupt Enable bit
	1 = ATTACH interrupt is enabled
	0 = ATTACH interrupt is disabled
bit 5	RESUMEIE: RESUME Interrupt Enable bit
	1 = RESUME interrupt is enabled
	0 = RESUME interrupt is disabled
bit 4	IDLEIE: Idle Detect Interrupt Enable bit
	1 = Idle interrupt is enabled
	0 = Idle interrupt is disabled
bit 3	TRNIE: Token Processing Complete Interrupt Enable bit
	1 = TRNIF interrupt is enabled
	0 = TRNIF interrupt is disabled
bit 2	SOFIE: SOF Token Interrupt Enable bit
	1 = SOFIF interrupt is enabled
	0 = SOFIF interrupt is disabled
bit 1	UERRIE: USB Error Interrupt Enable bit ⁽¹⁾
	1 = LISB Error interrunt is enabled

- 1 = USB Error interrupt is enabled 0 = USB Error interrupt is disabled
- bit 0 URSTIE: USB Reset Interrupt Enable bit⁽²⁾
 - 1 = URSTIF interrupt is enabled
 - 0 = URSTIF interrupt is disabled
 - DETACHIE: USB Detach Interrupt Enable bit⁽³⁾
 - 1 = DATTCHIF interrupt is enabled
 - 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

- 2: Device mode.
- 3: Host mode.

TABLE 12-8: PORTD REGISTER MAP FOR PIC32MX330F064H, PIC32MX350F128H, PIC32MX350F256H, PIC32MX370F512H, PIC32MX430F064H, PIC32MX450F128H, PIC32MX450F256H, PIC32MX470F512H DEVICES ONLY

ess		6								B	lits								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6300		31:16	_	—	—	—	—	—	—	—	—	—	_	_	—	—	_	—	0000
0000	ANOLLD	15:0	_	—	—	—	—	—	—	—	—	—	—	—	ANSELD3	ANSELD2	ANSELD1	—	000E
6310	TRISD	31:16	_	_	—	—	—		—	—	—		—	—	—		—		0000
0010	TRIOD	15:0	_	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	xxxx
5320	PORTD	31:16	_	—	—	—	-	_	—	—	—	—	—	—	—	—	—	—	0000
0020		15:0	_	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
6330	LATD	31:16	_	—	—	—	-	_	—	—	—	—	—	—	—	—	—	—	0000
	0.0	15:0	_	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
6340	ODCD	31:16	_	—	—	—	-	_	—	—	—	—	—	—	—	—	—	—	0000
00.0	0000	15:0	_	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	xxxx
6350	CNPUD	31:16	_	—	—	—	-	_	—	—	—	—	—	—	—	—	—	—	0000
	0.11 00	15:0	_	—	—	—	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	xxxx
6360	CNPDD	31:16	_	—	—	—	-	_	—	—	—	—	—	—	—	—	—	—	0000
	0.11 00	15:0	_	—	—	—	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	xxxx
6370	CNCOND	31:16	_	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
	0.100.15	15:0	ON		SIDL	—	—	_	—	_		—	—	_	—	—	—	—	0000
6380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0000	ONLIND	15:0	—	—	—	—	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	xxxx
		31:16	_		—	—	—		—	—		—	—	—	—	—	—	—	0000
6390	CNSTATD	15:0	_	—	—	—	CN STATD11	CN STATD10	CN STATD9	CN STATD8	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	xxxx

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for Note 1: more information.

REGISTER 12-3:	CNCONX: CHANGE NOTICE CONTROL FOR PORTX REGISTER ($x = A - G$)
----------------	--

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	ON	—	SIDL	—	—	—	—	—
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	—	—		_	_	_	-	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Change Notice (CN) Control ON bit
 - 1 = CN is enabled
 - 0 = CN is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Control bit
 - 1 = CPU Idle Mode halts CN operation
 - 0 = CPU Idle does not affect CN operation
- bit 12-0 Unimplemented: Read as '0'

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
15:8	ON ⁽¹⁾	—	SIDL	TWDIS	TWIP	—	—	—
	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
7:0	TGATE		TCKP	S<1:0>		TSYNC	TCS	_

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15	ON: Timer On bit ⁽¹⁾
	1 = Timer is enabled
	0 = Timer is disabled
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Stop in Idle Mode bit
	1 = Discontinue operation when device enters Idle mode0 = Continue operation even in Idle mode
bit 12	TWDIS: Asynchronous Timer Write Disable bit
	1 = Writes to TMR1 are ignored until pending write operation completes0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)
bit 11	TWIP: Asynchronous Timer Write in Progress bit
	In Asynchronous Timer mode:
	1 = Asynchronous write to TMR1 register in progress
	0 = Asynchronous while to TMRT register complete
	This bit is read as '0'.
bit 10-8	Unimplemented: Read as '0'
bit 7	TGATE: Timer Gated Time Accumulation Enable bit
	When TCS = 1:
	This bit is ignored.
	When ICS = 0:
	0 = Gated time accumulation is enabled
bit 6	Unimplemented: Read as '0'
bit 5-4	TCKPS<1:0>: Timer Input Clock Prescale Select bits
	11 = 1:256 prescale value
	10 = 1:64 prescale value
	01 = 1.8 prescale value
hit 2	Unimplemented: Deed es '0'
DIC 3	Unimplemented: Read as 0

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

14.2 Control Register

TABLE 14-1: TIMER2 THROUGH TIMER5 REGISTER MAP

ess										В	its								
Virtual Addre (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0800	TOCON	31:16	—	—	_	—	—			-	—		—	—	—		—		0000
0800	12001	15:0	ON	—	SIDL	_	_	_	_	_	TGATE	-	TCKPS<2:0	>	T32	_	TCS	_	0000
0810	TMD2	31:16	_	—	_	_	_	_	_	_	_	_	—	_	_	_	_	_	0000
0010	TIVITZ	15:0								TMR2	<15:0>								0000
0820	002	31:16	_	—	_	_	_	_	_	_	_	_	—	_	_	_	_	_	0000
0020	FNZ	15:0								PR2<	:15:0>								FFFF
0.000		31:16	_	—	_	_	_	_	_	_	_	_	—	_	_	_	_	_	0000
0400	13001	15:0	ON	—	SIDL	_	_	_	_	_	TGATE	-	TCKPS<2:0	>	_	_	TCS	_	0000
0410	TMD3	31:16	_	—	_	_	_	_	_	_	_	_	—	_	_	_	_	_	0000
UAIU	TIMING	15:0								TMR3	<15:0>								0000
0420	DD3	31:16	_	—	—	_	—	—	—	—	—	_	—	—	—	—	—	_	0000
0720	110	15:0				-				PR3<	:15:0>				-		-		FFFF
0000		31:16	_	—	_	_	_	-	-	-	—	—	—	_	—	_	—	_	0000
0000	14001	15:0	ON	—	SIDL		_	_	_	_	TGATE	-	TCKPS<2:0	>	T32	_	TCS		0000
0010	TMP4	31:16	_	—	_	_	_	-	-	-	—	—	—	_	—	_	—	_	0000
0010	11011.54	15:0				-				TMR4	<15:0>				-		-		0000
0020		31:16	_	—	_	_	_	-	-	-	—	—	—	_	—	_	—	_	0000
0020	1114	15:0				-				PR4<	:15:0>				-		-		FFFF
0500		31:16	_	—	_	_	_	-	-	-	—	—	—	_	—	_	—	_	0000
0200	10001	15:0	ON	—	SIDL		_	_	_	_	TGATE	-	TCKPS<2:0	>	—	_	TCS		0000
0E10	TMP5	31:16	_	—	_	_	_	-	-	-	—	—	—	_	—	_	—	_	0000
	TWING	15:0				-	-			TMR5	<15:0>		-	-	-		-		0000
0520	DD5	31:16	_	—	—	_	_	_	_	_	_	—	-	_	_	_	_	—	0000
0220	FNJ	15:0 PR5<15:0>								FFFF									

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

ess		0								, Bi	ts								ú
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
6440		31:16		_	_	_	_	_	_			_			_		_	—	0000
0440	15:0 Baud Rate Generator Prescaler					0000													
6600		31:16	_	—	—	—	—	_	_	—	_	—	—	_	—	—	_	—	0000
0000	OHNODE	15:0	ON	—	SIDL	IREN	RTSMD	_	UEN	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEI	_<1:0>	STSEL	0000
6610	LIASTA(1)	31:16	_	—	—	—	—	_	_	ADM_EN				ADDR	R<7:0>				0000
0010	04017	15:0	UTXISE	EL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXIS	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6620		31:16	_	—	—	—	—	_	_	—	_	_	_	_	_	—	_	—	0000
0020	OFTAILEO	15:0	_	—	—	—	—	_	_	TX8		-		Transmit	Register				0000
6630		31:16	_			_		_	_	—	_	_	—	_	—	—	_	—	0000
0030	OHIVAILEO	15:0	_	—	—	—	—	_	_	RX8		-		Receive	Register				0000
6640		31:16	_	—	—	—	_	_	_	—	_	_	—	_	—	—	_	—	0000
0040	040100	15:0							Bau	d Rate Gen	erator Pres	caler							0000
6800		31:16	_			_		_	_	_			—	_		—		—	0000
0000	CONICDE	15:0	ON		SIDL	IREN	RTSMD	_	UEN	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEI	_<1:0>	STSEL	0000
6810	115STA(1)	31:16	_			_		_	_	ADM_EN				ADDR	R<7:0>				0000
0010	0001/1	15:0	UTXISE	EL<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISI	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	FFFF
6820		31:16	_			_		_	_	_		_	—	_	—	—		—	0000
0020	OUTAILEO	15:0	_			_		_	_	TX8				Transmit	Register				0000
6830		31:16	_	—	—	—	—	_	_	—	_	_	_	_	_	—	_	—	0000
0030	USIVALEO	15:0	_	—	—	—	—	_	_	RX8		-		Receive	Register				0000
6840	U5BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	—	0000
0040	CODICO	15:0							Bau	d Rate Gen	erator Pres	caler							0000

TABLE 20-1: UART1 THROUGH UART5 REGISTER MAP (CONTINUED)

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 ARPT<7:0>: Alarm Repeat Counter Value bits⁽³⁾ 11111111 = Alarm will trigger 256 times

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
10.0	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
7:0	_	_	_	_	_	_	C2OUT	C10UT

REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in IDLE Control bit

1 = All Comparator modules are disabled in IDLE mode

0 = All Comparator modules continue to operate in the IDLE mode

- bit 12-2 Unimplemented: Read as '0'
- bit 1 **C2OUT:** Comparator Output bit
 - 1 = Output of Comparator 2 is a '1'
 - 0 = Output of Comparator 2 is a '0'

bit 0 C1OUT: Comparator Output bit

- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

25.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them. A block diagram of the module is illustrated in Figure 25-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/Vss or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The CVREF module has the following features:

- High and low range selection
- · Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- · Output can be connected to a pin



FIGURE 25-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

30.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- · MPLAB X IDE compatibility

30.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

30.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

30.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility





TABLE 31-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

			Standaro (unless Operatin	$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions		
OC10	TccF	OCx Output Fall Time	_	_		ns	See parameter DO32		
OC11	TccR	OCx Output Rise Time	—	—		ns	See parameter DO31		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 31-9: OCx/PWM MODULE TIMING CHARACTERISTICS



TABLE 31-28: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\label{eq:constraint} \begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param No.	Symbol	Characteristics ⁽¹⁾	Min	Typical ⁽²⁾	Max	Units	Conditions		
OC15	Tfd	Fault Input to PWM I/O Change	—	—	50	ns			
OC20	TFLT	Fault Input Pulse Width	50	_		ns	—		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 31-31: SPIX MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS				$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions		
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	Тscк + 20		_	ns	_		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 31-20: PARALLEL SLAVE PORT TIMING



TABLE 31-38: PARALLEL SLAVE PORT REQUIREMENTS

AC CH	IARACTE	RISTICS	$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$							
Para m.No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions			
PS1	TdtV2wr H	Data In Valid before \overline{WR} or \overline{CS} Inactive (setup time)	20	_	—	ns	_			
PS2	TwrH2dt I	WR or CS Inactive to Data-In Invalid (hold time)	40	—	—	ns	—			
PS3	TrdL2dt V	RD and CS Active to Data-Out Valid	—	—	60	ns	—			
PS4	TrdH2dtl	RD Active or CS Inactive to Data-Out Invalid	0	—	10	ns	—			
PS5	Tcs	CS Active Time	Трв + 40	_	_	ns	—			
PS6	Twr	WR Active Time	Трв + 25	_	—	ns	—			
PS7	Trd	RD Active Time	Трв + 25	_	_	ns	_			

Note 1: These parameters are characterized, but not tested in manufacturing.



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64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	MILLIMETERS				
Dimension	MIN	NOM	MAX			
Contact Pitch	E		0.50 BSC			
Contact Pad Spacing	C1		11.40			
Contact Pad Spacing	C2		11.40			
Contact Pad Width (X64)	X1			0.30		
Contact Pad Length (X64)	Y1			1.50		
Distance Between Pads	G	0.20				

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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