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Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx370f512l-v-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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TABLE 4: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW)^(1,2,3)

PIC32MX330F064L PIC32MX350F128L PIC32MX350F256L PIC32MX370F512L

100

Pin # Full Pin Name Pin # Full Pin Name **RG15** Vss 1 36 2 VDD 37 VDD AN22/RPE5/PMD5/RE5 TCK/CTED2/RA1 3 38 AN23/PMD6/RE6 **RPF13/RF13** 4 39 AN27/PMD7/RE7 RPF12/RF12 5 40 RPC1/RC1 6 41 AN12/PMA11/RB12 RPC2/RC2 AN13/PMA10/RB13 7 42 8 RPC3/RC3 43 AN14/RPB14/CTED5/PMA1/RB14 RPC4/CTED7/RC4 44 AN15/RPB15/OCFB/CTED6/PMA0/RB15 9 10 AN16/C1IND/RPG6/SCK2/PMA5/RG6 45 Vss AN17/C1INC/RPG7/PMA4/RG7 11 46 Voo AN18/C2IND/RPG8/PMA3/RG8 47 RPD14/RD14 12 MCLR 48 RPD15/RD15 13 AN19/C2INC/RPG9/PMA2/RG9 49 RPF4/PMA9/RF4 14 RPF5/PMA8/RF5 15 Vss 50 VDD RPF3/RF3 16 51 TMS/CTED1/RA0 RPF2/RF2 17 52 RPE8/RE8 RPF8/RF8 18 53 RPE9/RE9 RPF7/RF7 54 19 AN5/C1INA/RPB5/RB5 RPF6/SCK1/INT0/RF6 20 55 AN4/C1INB/RB4 SDA1/RG3 21 56 22 PGED3/AN3/C2INA/RPB3/RB3 57 SCL1/RG2 PGEC3/AN2/C2INB/RPB2/CTED13/RB2 SCL2/RA2 58 23 24 PGEC1/AN1/RPB1/CTED12/RB1 59 SDA2/RA3 PGED1/AN0/RPB0/RB0 TDI/CTED9/RA4 25 60 PGEC2/AN6/RPB6/RB6 TDO/RA5 26 61 PGED2/AN7/RPB7/CTED3/RB7 62 VDD 27 VREF-/CVREF-/PMA7/RA9 63 OSC1/CLKI/RC12 28 VREF+/CVREF+/PMA6/RA10 OSC2/CLKO/RC15 29 64 30 AVDD 65 Vss 31 AVss 66 RPA14/RA14 AN8/RPB8/CTED10/RB8 32 67 **RPA15/RA15** AN9/RPB9/CTED4/RB9 RPD8/RTCC/RD8 33 68 CVREFOUT/AN10/RPB10/CTED11PMA13/RB10 RPD9/RD9 69 34 35 AN11/PMA12/RB11 70 RPD10/PMCS2/RD10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 12.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RGx), with the exception of RF6, can be used as a change notification pin (CNAx-CNGx). See Section 12.0 "VO Ports" for more information.

3: RPF6 (pin 55) and RPF7 (pin 54) are only remappable for input functions.

TABLE 5: PIN NAMES FOR 100-PIN DEVICES (CONTINUED)

100-PIN TQFP	(TOP VIEW) ^(1,2)
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PIC32MX430F064L PIC32MX450F128L PIC32MX450F256L PIC32MX470F512L

100

			1
Pin #	Full Pin Name	Pin #	Full Pin Name
71	RPD11/PMCS1/RD11	86	VDD
72	RPD0/INT0/RD0	87	RPF0/PMD11/RF0
73	SOSCI/RPC13/RC13	88	RPF1/PMD10/RF1
74	SOSCO/RPC14/T1CK/RC14	89	RPG1/PMD9/RG1
75	Vss	90	RPG0/PMD8/RG0
76	AN24/RPD1/RD1	91	TRCLK/RA6
77	AN25/RPD2/RD2	92	TRD3/CTED8/RA7
78	AN26/RPD3/RD3	93	PMD0/RE0
79	RPD12/PMD12/RD12	94	PMD1/RE1
80	PMD13/RD13	95	TRD2/RG14
81	RPD4/PMWR/RD4	96	TRD1/RG12
82	RPD5/PMRD/RD5	97	TRD0/RG13
83	PMD14/RD6	98	AN20/CTPLS/PMD2/RE2
84	PMD15/RD7	99	RPE3/PMD3/RE3
85	VCAP	100	AN21/PMD4/RE4

 Note
 1:
 The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 12.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See Section 12.0 "I/O Ports" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS9	IFS8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	IFS7	IFS6	IFS5	IFS4	IFS3	IFS2	IFS1	IFS0

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Legend:

R = Readable bit	Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-0 IFS31-IFS0: Interrupt Flag Status bits

- 1 = Interrupt request has occurred
- 0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 IEC31-IEC0: Interrupt Enable bits

1 = Interrupt is enabled

0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	_	—	—	—	_	_	—
7.0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
7:0					RDWR	DMACH<2:0>		

REGISTER 10-2: DMASTAT: DMA STATUS REGISTER

Legend:

Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-4 Unimplemented: Read as '0'

- bit 3 RDWR: Read/Write Status bit
 - 1 = Last DMA bus access was a read
 - 0 = Last DMA bus access was a write
- bit 2-0 **DMACH<2:0>:** DMA Channel bits These bits contain the value of the most recent active DMA channel.

REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
01.04	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
31:24				DMAADDF	<31:24>					
00.40	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
23:10	DMAADDR<23:16>									
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
15:8	DMAADDR<15:8>									
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
				DMAADD	R<7:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 DMAADDR<31:0>: DMA Module Address bits

These bits contain the address of the most recent DMA access.

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 6 **CRCAPP:** CRC Append Mode bit⁽¹⁾

- 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
- 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5 **CRCTYP:** CRC Type Selection bit
 - 1 = The CRC module will calculate an IP header checksum
 - 0 = The CRC module will calculate a LFSR CRC
- bit 4-3 Unimplemented: Read as '0'
- bit 2-0 CRCCH<2:0>: CRC Channel Select bits
 - 111 = CRC is assigned to Channel 7
 - 110 = CRC is assigned to Channel 6
 - 101 = CRC is assigned to Channel 5
 - 100 = CRC is assigned to Channel 4
 - 011 = CRC is assigned to Channel 3
 - 010 = CRC is assigned to Channel 2
 - 001 = CRC is assigned to Channel 1
 - 000 = CRC is assigned to Channel 0
- **Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0				CHPDA	Γ<7:0>			

REGISTER 10-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode: Data to be matched must be stored in this register to allow terminate on match.

All other modes: Unused.



FIGURE 11-1: PIC32MX430/450/470 USB INTERFACE DIAGRAM

REGISTER 11-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7 Bit 30/22/14/6 U-0 U-0 — —		Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
23.16	U-0 U-0		U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15.0		—	—	—	—	—	—	—	
7.0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS	
7:0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	SESENDIF —		

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit					
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-8 Unimplemented: Read as '0'

- bit 7 IDIF: ID State Change Indicator bit
 - 1 = Change in ID state is detected
 - 0 = No change in ID state is detected

bit 6 T1MSECIF: 1 Millisecond Timer bit

- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 LSTATEIF: Line State Stable Indicator bit

- 1 = USB line state has been stable for 1millisecond, but different from last time
- 0 = USB line state has not been stable for 1 millisecond

bit 4 ACTVIF: Bus Activity Indicator bit

- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected
- bit 3 SESVDIF: Session Valid Change Indicator bit
 - 1 = VBUS voltage has dropped below the session end level
 - 0 = VBUS voltage has not dropped below the session end level

bit 2 SESENDIF: B-Device VBUS Change Indicator bit

- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected
- bit 1 Unimplemented: Read as '0'
- bit 0 VBUSVDIF: A-Device VBUS Change Indicator bit
 - 1 = Change on the session valid input is detected
 - 0 = No change on the session valid input is detected

REGISTER 11-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
23.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.9	U-0	U-0	U-0 U-0		U-0 U-0		U-0	U-0
15.0	—	—	—	—	—	—	—	—
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	STALLIE	ATTACHIE	DESIMEIE			SOFIE	LIFRRIF(1)	URSTIE ⁽²⁾
						CONE		DETACHIE ⁽³⁾

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-8 Unimplemented: Read as '0'

	-
bit 7	STALLIE: STALL Handshake Interrupt Enable bit
	1 = STALL interrupt is enabled
	0 = STALL interrupt is disabled
bit 6	ATTACHIE: ATTACH Interrupt Enable bit
	1 = ATTACH interrupt is enabled
	0 = ATTACH interrupt is disabled
bit 5	RESUMEIE: RESUME Interrupt Enable bit
	1 = RESUME interrupt is enabled
	0 = RESUME interrupt is disabled
bit 4	IDLEIE: Idle Detect Interrupt Enable bit
	1 = Idle interrupt is enabled
	0 = Idle interrupt is disabled
bit 3	TRNIE: Token Processing Complete Interrupt Enable bit
	1 = TRNIF interrupt is enabled
	0 = TRNIF interrupt is disabled
bit 2	SOFIE: SOF Token Interrupt Enable bit
	1 = SOFIF interrupt is enabled
	0 = SOFIF interrupt is disabled
bit 1	UERRIE: USB Error Interrupt Enable bit ⁽¹⁾
	1 = LISB Error interrunt is enabled

- 1 = USB Error interrupt is enabled 0 = USB Error interrupt is disabled
- bit 0 URSTIE: USB Reset Interrupt Enable bit⁽²⁾
 - 1 = URSTIF interrupt is enabled
 - 0 = URSTIF interrupt is disabled
 - DETACHIE: USB Detach Interrupt Enable bit⁽³⁾
 - 1 = DATTCHIF interrupt is enabled
 - 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.

- 2: Device mode.
- 3: Host mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
23.16	U-0	U-0 U-0		U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0 U-0		U-0	U-0
15.0	—	—	—	—	—	—	—	—
7.0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
7:0	UTEYE	UOEMON	— USBSIDI					UASUSPND

REGISTER 11-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Legend:

R = Readable bit	Readable bit W = Writable bit		ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 UTEYE: USB Eye-Pattern Test Enable bit

- 1 = Eye-Pattern Test is enabled
- 0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB OE Monitor Enable bit

1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving
 0 = OE signal is inactive

bit 5 Unimplemented: Read as '0'

- bit 4 USBSIDL: Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode

bit 3-1 Unimplemented: Read as '0'

bit 0 UASUSPND: Automatic Suspend Enable bit

- 1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 11-5.
- 0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

12.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only options.

Peripheral pin select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The peripheral pin select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. Peripheral pin select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

12.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the peripheral pin select feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

12.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the peripheral pin select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the peripheral pin select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral. When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

12.3.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral pin select features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

12.3.4 INPUT MAPPING

The inputs of the peripheral pin select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 12-1, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-1.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: F

REMAPPABLE INPUT EXAMPLE FOR U1RX



Bit Bit Bit Bit Range 31/23/15/7 30/22/14		Bit 30/22/14/6	Bit 29/21/13/5	Bit Bit 28/20/12/4 27/19/11/3		Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0 U-^		U-0	R-0 R-0		R-0	R-0	R-0		
23.16	—	—	—	RXBUFELM<4:0>						
23:16	U-0	U-0	U-0	R-0	R-0	R-0 R-0		R-0		
	—	—	—	TXBUFELM<4:0>						
45.0	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0		
15:8	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR		
7.0	R-0	R/W-0	R-0	U-0	R-1 U-0		R-0	R-0		
7:0	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF		

REGISTER 18-3: SPIxSTAT: SPI STATUS REGISTER

Legend:	C = Clearable bit	HS = Set in hardware					
R = Readable bit	W = Writable bit	V = Writable bit U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

- bit 31-29 Unimplemented: Read as '0'
- bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 23-21 Unimplemented: Read as '0'
- bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 15-13 Unimplemented: Read as '0'
- bit 12 **FRMERR:** SPI Frame Error status bit
 - 1 = Frame error is detected
 - 0 = No Frame error is detected
 - This bit is only valid when FRMEN = 1.
- bit 11 SPIBUSY: SPI Activity Status bit
 - 1 = SPI peripheral is currently busy with some transactions
 - 0 = SPI peripheral is currently idle
- bit 10-9 Unimplemented: Read as '0'
- bit 8 SPITUR: Transmit Under Run bit
 - 1 = Transmit buffer has encountered an underrun condition
 - 0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.

- bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
 - 1 = When SPI module shift register is empty
 - 0 = When SPI module shift register is not empty
- bit 6 SPIROV: Receive Overflow Flag bit
 - 1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
 - 0 = No overflow has occurred

This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.

- bit 5 SPIRBE: RX FIFO Empty bit (valid only when ENHBUF = 1) 1 = RX FIFO is empty (CRPTR = SWPTR)
 - 0 = RX FIFO is not empty (CRPTR \neq SWPTR)
- bit 4 Unimplemented: Read as '0'

REGISTER 19-2: I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware set or clear when Start, Repeated Start or Stop detected.
bit 3	S: Start bit
	 1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last
	Hardware set or clear when Start, Repeated Start or Stop detected.
bit 2	R_W: Read/Write Information bit (when operating as I ² C slave)
	1 = Read – indicates data transfer is output from slave
	0 = Write – indicates data transfer is input to slave
	Hardware set or clear after reception of I ² C device address byte.
bit 1	RBF: Receive Buffer Full Status bit
	1 = Receive complete, I2CxRCV is full
	0 = Receive not complete, I2CxRCV is empty
	Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit
	1 = Transmit in progress, I2CxTRN is full
	0 = Transmit complete, I2CxTRN is empty

Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

22.1 Control Registers

TABLE 22-1: RTCC REGISTER MAP

ess											Bits								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0200	PTCCON	31:16	—	—	—	—	_	—					CAL<	9:0>					0000
0200	RICCON	15:0	ON	_	SIDL	—	_	—	-		RTSECSEL	RTCCLKON	—	_	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210		31:16		_	_	—		_			—	_	_	_	_	_	_	—	0000
	RICALRI	15:0	ALRMEN	CHIME	PIV	ALRMSYNC		AMASK<3:0>			ARPT<7:0>					0000			
0000	DTOTIME	31:16	HR10<3:0>				HR01<3:0>			MIN10<3:0>			MIN01<3:0>			xxxx			
0220	RICHIVIL	15:0	SEC10<3:0>				SEC01<3:0>			_	_	_	_	_	_	_	—	xx00	
0230	DTODATE	31:16		YEAR	10<3:0>		YEAR01<			YEAR01<3:0> MONTH10<3:0> MONTH01<		01<3:0>		xxxx					
0230	RICDAIL	15:0		DAY1	0<3:0>		DAY01<3:0>			_	_	_	_		WDAY0	1<3:0>		xx00	
0240		31:16		HR1	0<3:0>		HR01<3:0>				MIN10<	3:0>			MIN01	<3:0>		xxxx	
0240		15:0		SEC	10<3:0>			SEC0 ²	1<3:0>		_	_	_	_	_	_	_	—	xx00
0250		31:16		_	_	—		_				MONTH10)<3:0>			MONTH	01<3:0>		00xx
		15:0		DAY1	0<3:0>			DAY01	1<3:0>		_	_	—	_		WDAY0	1<3:0>		xx0x

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Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

23.1 **Control Registers**

TABLE 23-1: ADC REGISTER MAP

SSS			Bits																
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000		31:16	-	—	_	_	_	—	—	—	_	—	—	_	—	—	_	—	0000
9000	ADICONT	15:0	ON	_	SIDL	—	_		FORM<2:0	>		SSRC<2:0>	>	CLRASAM	_	ASAM	SAMP	DONE	0000
0010	AD1CON2(1)	31:16			—	—	—	—		—		—		—	—	—			0000
9010	AD ICONZ ⁽)	15:0	,	VCFG<2:0>	>	OFFCAL	—	CSCNA	—	—	BUFS	—		SMPI	<3:0>		BUFM	ALTS	0000
0020		31:16	—	_	—	—	—	—	_	—	—	—	—	_	—	_	—	_	0000
9020	AD ICONS'	15:0	ADRC	—	—		:	SAMC<4:0>						ADCS	\$<7:0>				0000
0040		31:16	CH0NB	_	—		CH0SB<4:0>			CH0NA	_	_		CH0SA<4:0>				0000	
5040	AD ICHS.	15:0		—	-	_	—	—	—	—		—	—	-	—	—		—	0000
0050		31:16	_	CSSL30	CSSL29	CSSL28	CSSL27	CSSL26	CSSL25	CSSL24	CSSL23	CSSL22	CSSL21	CSSL20	CSSL19	CSSL18	CSSL17	CSSL16	0000
9030	AD1033L	15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
0070		31:16	ADC Result Word 0 (ADC1BUE0<31:0>)																
9070	ADCIBOIO	15:0																	
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)													0000			
3000		15:0		0000															
anan		31:16	ADC Booult Mord 2 (ADC181 (52<21:05)													0000			
3030	ADCIDUI 2	15:0															0000		
0040		31:16	ADC Result Word 3 (ADC1BUE3<31:0>)																
3070	ADCIDOI 3	15:0																	
90B0	ADC1BUE4	31:16	ADC Result Word 4 (ADC1BUE4<31:0>)																
0000	1.0010011	15:0	ADC Result Word 4 (ADC IBUF4<31:0>)																
9000	ADC1BUE5	31:16							ADC Res	sult Word 5	(ADC1BUE	5<31.0>)							0000
0000	1.2012010	15:0							71201100		(7.201201	0.01.07							0000
9000	ADC1BUF6	31:16							ADC Res	sult Word 6	(ADC1BUE	6<31.0>)							0000
0020		15:0							1.201.00		(,	• • • • • •							0000
90E0	ADC1BUF7	31:16							ADC Res	sult Word 7	(ADC1BUF	7<31:0>)							0000
		15:0									(, ,							0000
90F0	ADC1BUF8	31:16							ADC Res	sult Word 8	(ADC1BUF	8<31:0>)							0000
		15:0							1.001.00		(,								0000
9100	ADC1BUF9	31:16							ADC Res	sult Word 9	(ADC1BUF	9<31:0>)							0000
		15:0							1.2 0 1.00										0000
Leger	agend: x = unknown value on Reset; = unimplemented, read as '0'. Reset values are shown in hexadecimal.																		

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for details. Note 1:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	_	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	_	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
15:8		VCFG<2:0>		OFFCAL	_	CSCNA	—	—
7.0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	BUFS	—		SMP	9 <3:0>		BUFM	ALTS

REGISTER 23-2: AD1CON2: ADC CONTROL REGISTER 2

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as 'O'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-13 VCFG<2:0>: Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	AVss
001	External VREF+ pin	AVss
010	AVDD	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVss

bit 12 OFFCAL: Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the sample and hold amplifier are connected to VREFL

0 = Disable Offset Calibration mode

The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 Unimplemented: Read as '0'

- bit 10 **CSCNA:** Input Scan Select bit
 - 1 = Scan inputs

0 = Do not scan inputs

bit 9-8 Unimplemented: Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1.

1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7

0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 Unimplemented: Read as '0'

bit 5-2 SMPI<3:0>: Sample/Convert Sequences Per Interrupt Selection bits

```
1111 = Interrupts at the completion of conversion for each 16<sup>th</sup> sample/convert sequence
```

1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence

0001 = Interrupts at the completion of conversion for each 2^{nd} sample/convert sequence 0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 BUFM: ADC Result Buffer Mode Select bit

- 1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
 - 0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 ALTS: Alternate Input Sample Mode Select bit

- 1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
- 0 = Always use Sample A input multiplexer settings

REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

- bit 15-14 FCKSM<1:0>: Clock Switching and Monitor Selection Configuration bits
 - 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
 - 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
 - 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
- bit 13-12 FPBDIV<1:0>: Peripheral Bus Clock Divisor Default Value bits
 - 11 = PBCLK is SYSCLK divided by 8
 - 10 = PBCLK is SYSCLK divided by 4
 - 01 = PBCLK is SYSCLK divided by 2
 - 00 = PBCLK is SYSCLK divided by 1
- bit 11 Reserved: Write '1'
- bit 10 OSCIOFNC: CLKO Enable Configuration bit
 - 1 = CLKO output is disabled
 - 0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)
- bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits
 - 11 = Primary Oscillator is disabled
 - 10 = HS Oscillator mode is selected
 - 01 = XT Oscillator mode is selected
 - 00 = External Clock mode is selected
- bit 7 IESO: Internal External Switchover bit
 - 1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
 - 0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)
- bit 6 **Reserved:** Write '1'
- bit 5 **FSOSCEN:** Secondary Oscillator Enable bit
 - 1 = Enable Secondary Oscillator
 - 0 = Disable Secondary Oscillator
- bit 4-3 Reserved: Write '1'
- bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
 - 111 = Fast RC Oscillator with divide-by-N (FRCDIV)
 - 110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
 - 101 = Low-Power RC Oscillator (LPRC)
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL)
 - 010 = Primary Oscillator (XT, HS, EC)⁽¹⁾
 - 001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
 - 000 = Fast RC Oscillator (FRC)
- **Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

- bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
 - 111 = 12x divider
 - 110 = 10x divider
 - 101 = 6x divider
 - 100 = 5x divider
 - 011 = 4x divider
 - 010 = 3x divider
 - 001 = 2x divider
 - 000 = 1x divider
- Note 1: This bit is available on PIC32MX4XX devices only.

TABLE 31-15: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHA		STICS	$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^\circ C \leq TA \leq +70^\circ C \mbox{ for Commercial} \\ & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$							
Param. No.	Symbol Characteristics		Min.	Тур.	Max.	Units	Comments			
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time.	_	_	10	μs	See Note 1			
D313	DACREFH	CVREF Input Voltage Reference Range	AVss	—	AVdd	V	CVRSRC with CVRSS = 0			
			VREF-	_	VREF+	V	CVRSRC with CVRSS = 1			
D314	DVREF	CVREF Programmable Output Range	0	_	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size			
			0.25 x DACREFH	_	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/ 32 step size			
D315	DACRES	Resolution	_	_	DACREFH/24		CVRCON <cvrr> = 1</cvrr>			
			—	—	DACREFH/32		CVRCON <cvrr> = 0</cvrr>			
D316	DACACC	Absolute Accuracy ⁽²⁾	—	_	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>			
			—	—	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>			

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 31-16: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS				ard Operat s otherwis ing temper	ting Cor se state ature	nditions d) 0°C ≤ TA -40°C ≤ -40°C ≤	: 2.3V to 3.6V $a \le +70^{\circ}$ C for Commercial TA $\le +85^{\circ}$ C for Industrial TA $\le +105^{\circ}$ C for V-temp
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D321	Cefc	External Filter Capacitor Value	8	10		μF	Capacitor must be low series resistance (3 ohm). Typical voltage on the VCAP pin is 1.8V.



FIGURE 31-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

TABLE 31-40: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions		
PM11	Twr	PMWR Pulse Width	_	1 Трв			—		
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	_	2 Трв	_	_	_		
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)		1 Трв					

Note 1: These parameters are characterized, but not tested in manufacturing.