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Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx430f064h-i-pt

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Device Pin Tables

TABL	E 2: PIN NAMES FOR 64-PIN DEVICES		
64	-PIN QFN ^(1,2,3,4) AND TQFP ^(1,2,3,4) (TOP VIEV	V)	
PI PI PI PI	C32MX330F064H C32MX350F128H C32MX350F256H C32MX370F512H		
	64	1	
		(4)	64
	QFN	(+)	TQFP
Pin #	Full Pin Name	Pin	# Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	RPF3/RF3
2	AN23/PMD6/RE6	34	RPF2/RF2
3	AN27/PMD7/RE7	35	RPF6/SCK1/INT0/RF6
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	SDA1/RG3
5	AN17/C1INC/RPG7/PMA4/RG7	37	SCL1/RG2
6	AN18/C2IND/RPG8/PMA3/RG8	38	VDD
7	MCLR	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	Vss	41	Vss
10	Vdd	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/RB5	43	RPD9/RD9
12	AN4/C1INB/RB4	44	RPD10/PMCS2/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMCS1/RD11
14	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	46	RPD0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3//RB7	50	AN25/RPD2/RD2
19	AVdd	51	AN26/RPD3/RD3
20	AVss	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10//RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11//PMA13/RB10	55	RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	Vss	57	VDD
26	VDD	58	RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/KPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31		63	RPE3/GTPLS/PMD3/RE3
32		64	ANZ1/MD4/RE4
NOTE	 The KETT plus can be used by remappable peripherals. See 1 	able 1 10r	the available peripherals and Section 12.3 "Peripheral Pin

1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 12.3 "Peripheral Pin Select" for restrictions.

Every I/O port pin (RBx-RGx), with the exception of RF6, can be used as a change notification pin (CNBx-CNGx). See Section 12.0 "I/O 2: Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

RPF6 (pin 35) is only available for output functions. 4:

2.9 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

2.10 EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations

The use of LDO regulators is preferred to reduce overall system noise and provide a cleaner power source. However, when utilizing switching Buck/ Boost regulators as the local power source for PIC32 devices, as well as in electrically noisy environments or test conditions required for IEC 61000-4-4 and IEC 61000-4-2, users should evaluate the use of T-Filters (i.e., L-C-L) on the power pins, as shown in Figure 2-5. In addition to a more stable power source, use of this type of T-Filter can greatly reduce susceptibility to EMI sources and events.

FIGURE 2-5: EMI/EMC/EFT SUPPRESSION CIRCUIT



TABLE 4-1: SFR MEMORY MAP

	Virtual Ac	ddress
Peripheral	Base	Offset Start
Watchdog Timer		0x0000
RTCC		0x0200
Timer1-5		0x0600
Peripheral Vatchdog Timer CC TCC Timer1-5 Toput Capture 1-5 Output Compare 1-5 CC1 and I2C2 PI1 and SPI2 IART1 and UART2 IMP DC VREF Comparator CTMU Oscillator Device and Revision ID Tash Controller Reset PPS Therrupts Bus Matrix DMA Prefetch USB PORTA-PORTG Configuration		0x2000
Output Compare 1-5		0x3000
Peripheral Vatchdog Timer RTCC Timer1-5 Toput Capture 1-5 Output Compare 1-5 Output Compa		0x5000
		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC	UXDFOU	0x9000
CVREF		0x9800
Comparator		0xA000
CTMU		0xA200
Oscillator		0xF000
Device and Revision ID		0xF200
Flash Controller]	0xF400
Reset		0xF600
PPS		0xFA04
Interrupts		0x1000
Bus Matrix		0x2000
DMA	0.0500	0x3000
Prefetch	UXRF88	0x4000
USB]	0x5040
PORTA-PORTG		0x6000
Configuration	0xBFC0	0x2FF0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—		IP3<2:0>	IS3<1:0>		
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	—	—	—		IP1<2:0>			:1:0>
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_	IP0<2:0>			IS0<	:1:0>

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

REGIST	ER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)
bit 9-8	IS1<1:0>: Interrupt Subpriority bits
	11 = Interrupt subpriority is 3
	10 = Interrupt subpriority is 2
	01 = Interrupt subpriority is 1
	00 = Interrupt subpriority is 0
bit 7-5	Unimplemented: Read as '0'
bit 4-2	IP0<2:0>: Interrupt Priority bits
	111 = Interrupt priority is 7
	•
	010 = Interrupt priority is 2
	001 = Interrupt priority is 1
	000 = Interrupt is disabled
bit 1-0	IS0<1:0>: Interrupt Subpriority bits
	11 = Interrupt subpriority is 3
	10 = Interrupt subpriority is 2
	01 = Interrupt subpriority is 1
	00 = Interrupt subpriority is 0
Note:	This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit
Note.	definitions.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
31.24	CHEW1<31:24>									
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
23:10	CHEW1<23:16>									
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15.0	CHEW1<15:8>									
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
7.0				CHEW1	<7:0>					

REGISTER 9-6: CHEW1: CACHE WORD 1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW1<31:0>:** Word 1 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

REGISTER 9-7: CHEW2: CACHE WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31.24	CHEW2<31:24>								
22:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23.10	CHEW2<23:16>								
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15.0	CHEW2<15:8>								
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
7.0				CHEW2	<7:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW2<31:0>:** Word 2 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

'0' = Bit is cleared

x = Bit is unknown

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
	CHEHIT<31:24>									
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
23.10	CHEHIT<23:16>									
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15.0	CHEHIT<15:8>									
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
7.0	CHEHIT<7:0>									
Legend										
R = Rea	dable bit		W = Writable	bit	U = Unimple	emented bit, re	ad as '0'			

REGISTER 9-10: CHEHIT: CACHE HIT STATISTICS REGISTER

bit 31-0 CHEHIT<31:0>: Cache Hit Count bits

-n = Value at POR

Incremented each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

'1' = Bit is set

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
31.24				CHEMIS<	<31:24>			
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:10				CHEMIS<	<23:16>			
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15.8				CHEMIS	<15:8>			
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7:0				CHEMIS	6<7:0>			
Legend								
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'								
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknowr				known				

bit 31-0 CHEMIS<31:0>: Cache Miss Count bits

Incremented each time the processor issues an instruction fetch from a cacheable region that misses the prefetch cache. Non-cacheable accesses do not modify this value.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	_	—	—	—	_	_	—
7.0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
7:0					RDWR	[DMACH<2:0>	•

REGISTER 10-2: DMASTAT: DMA STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 Unimplemented: Read as '0'

- bit 3 RDWR: Read/Write Status bit
 - 1 = Last DMA bus access was a read
 - 0 = Last DMA bus access was a write
- bit 2-0 **DMACH<2:0>:** DMA Channel bits These bits contain the value of the most recent active DMA channel.

REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
01.04	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
31:24				DMAADDF	<31:24>				
00.40	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
23:10	DMAADDR<23:16>								
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
15:8	DMAADDR<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
				DMAADD	R<7:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 DMAADDR<31:0>: DMA Module Address bits

These bits contain the address of the most recent DMA access.

PIC32MX330/350/370/430/450/470

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
31:24	—	—	BYTC)<1:0>	WBO ⁽¹⁾	—	_	BITO ⁽¹⁾
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	_	_	—	_	_	—
45.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	—	—	—			PLEN<4:0>		
7.0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
7:0	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	_	(CRCCH<2:0>	•

Legend:

Logena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

- bit 29-28 BYTO<1:0>: CRC Byte Order Selection bits
 - 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
 - 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
 - 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
 - 00 = No swapping (i.e., source byte order)
- bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾
 - 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
 - 0 = Source data is written to the destination unaltered
- bit 26-25 Unimplemented: Read as '0'
- bit 24 BITO: CRC Bit Order Selection bit⁽¹⁾

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode):

- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 Unimplemented: Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits⁽¹⁾

<u>When CRCTYP (DCRCCON<15>) = 1</u> (CRC module is in IP Header mode): These bits are unused.

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode): Denotes the length of the polynomial - 1.

- bit 7 CRCEN: CRC Enable bit
 - 1 = CRC module is enabled and channel transfers are routed through the CRC module
 - 0 = CRC module is disabled and channel transfers proceed normally
- Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

TABLE 12-2. UUTP	UT FIN SELECTION		
RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect
RPG8	RPG8R	RPG8R<3:0>	0001 = U3TX
RPF4	RPF4R	RPF4R<3:0>	- 0010 = U4RIS
RPD10	RPD10R	RPD10R<3:0>	0100 = Reserved
RPF1	RPF1R	RPF1R<3:0>	0101 = Reserved
RPB9	RPB9R	RPB9R<3:0>	0110 = SDO2
RPB10	RPB10R	RPB10R<3:0>	0111 = Reserved
RPC14	RPC14R	RPC14R<3:0>	1000 = Reserved
RPB5	RPB5R	RPB5R<3:0>	1010 = Reserved
RPC1 ⁽⁴⁾	RPC1R	RPC1R<3:0>	1011 = OC3
RPD14 ⁽⁴⁾	RPD14R	RPD14R<3:0>	1100 = Reserved
RPG1 ⁽⁴⁾	RPG1R	RPG1R<3:0>	1110 = Reserved
RPA14 ⁽⁴⁾	RPA14R	RPA14R<3:0>	1111 = Reserved
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect
RPG7	RPG7R	RPG7R<3:0>	0001 = U2TX
RPF5	RPF5R	RPF5R<3:0>	0010 = Reserved
RPD11	RPD11R	RPD11R<3:0>	-0011 = U1TX
RPF0	RPF0R	RPF0R<3:0>	-0100 = OSRIS()
RPB1	RPB1R	RPB1R<3:0>	0110 = SDO2
RPE5	RPE5R	RPE5R<3:0>	0111 = Reserved
RPC13	RPC13R	RPC13R<3:0>	1000 = SDO1
RPB3	RPB3R	RPB3R<3:0>	1001 = Reserved
RPF3 ⁽²⁾	RPF3R	RPF3R<3:0>	1010 = Reserved
RPC4 ⁽⁴⁾	RPC4R	RPC4R<3:0>	$\frac{1100}{1100} = \text{Reserved}$
RPD15 ⁽⁴⁾	RPD15R	RPD15R<3:0>	1101 = Reserved
RPG0 ⁽⁴⁾	RPG0R	RPG0R<3:0>	1110 = Reserved
RPA15 ⁽⁴⁾	RPA15R	RPA15R<3:0>	1111 = Reserved

TABLE 12-2: OUTPUT PIN SELECTION

Note 1: This selection is only available on General Purpose devices.

2: This selection is only available on 64-pin General Purpose devices.

3: This selection is only available on 100-pin General Purpose devices.

4: This selection is only available on 100-pin USB and General Purpose devices.

5: This selection is not available on 64-pin USB devices.

14.0 TIMER2/3, TIMER4/5

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MX330/350/370/430/450/470 family of devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- · Synchronous external 16-bit timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

- · Synchronous internal 32-bit timer
- · Synchronous internal 32-bit gated timer
- · Synchronous external 32-bit timer
- Note: In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through 5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or 4; 'y' represents Timer3 or 5.

14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 in 16-bit mode, Timer2/ 3 in 32-bit mode)
- Fast bit manipulation using CLR, SET, and INV registers

FIGURE 14-1: TIMER2, 3, 4, 5 BLOCK DIAGRAM (16-BIT)





FIGURE 14-2: TIMER2/3, 4/5 BLOCK DIAGRAM (32-BIT)⁽¹⁾

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	_	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ^(1,2)	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	_		SWDTPS<4:0>					WDTCLR

REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Legend:	y = Values set from Configuration bits on POR				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	set '0' = Bit is cleared x = Bit is unknown			

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Watchdog Timer Enable bit^(1,2)
 - 1 = Enables the WDT if it is not enabled by the device configuration
 - 0 = Disable the WDT if it was enabled in software
- bit 14-7 Unimplemented: Read as '0'
- bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.
- bit 1 WDTWINEN: Watchdog Timer Window Enable bit
 - 1 = Enable windowed Watchdog Timer
 - 0 = Disable windowed Watchdog Timer
- bit 0 WDTCLR: Watchdog Timer Reset bit
 - 1 = Writing a '1' will clear the WDT
 - 0 = Software cannot force this bit to a '0'
- **Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
 - 2: When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 16-1: ICXCON: INPUT CAPTURE 'X' CONTROL REGISTER (CONTINUED)

- bit 2-0 ICM<2:0>: Input Capture Mode Select bits
 - 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
 - 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
 - 101 = Prescaled Capture Event mode every sixteenth rising edge
 - 100 = Prescaled Capture Event mode every fourth rising edge
 - 011 = Simple Capture Event mode every rising edge
 - 010 = Simple Capture Event mode every falling edge
 - 001 = Edge Detect mode every edge (rising and falling)
 - 000 = Input Capture module is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
31:24	—	—	—	—	—	—	FWDTWI	NSZ<1:0>
23:16	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	—	WDTPS<4:0>				
45.0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
15:8	FCKSM<1:0>		FPBDI	V<1:0>	—	OSCIOFNC	POSCM	OD<1:0>
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	F	NOSC<2:0>	

REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 Reserved: Write '1'

bit 25-24 FWDTWINSZ<1:0>: Watchdog Timer Window Size bits

- 11 = Window size is 25%
- 10 = Window size is 37.5%
- 01 = Window size is 50%
- 00 = Window size is 75%

bit 23 FWDTEN: Watchdog Timer Enable bit

- 1 = Watchdog Timer is enabled and cannot be disabled by software
- 0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 WINDIS: Watchdog Timer Window Enable bit

- 1 = Watchdog Timer is in non-Window mode
- 0 = Watchdog Timer is in Window mode

bit 21 Reserved: Write '1'

bit 20-16 WDTPS<4:0>: Watchdog Timer Postscale Select bits

•
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

30.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

30.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

30.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

30.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming[™] (ICSP[™]).

30.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 31-18: EXTERNAL CLOCK TIMING REQUIREMENTS

			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)						
AC CH	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				r Commercial for Industrial C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions		
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	_	50 50	MHz MHz	EC (Note 4) ECPLL (Note 3)		
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT (Note 4)		
OS12			4		10	MHz	XTPLL (Notes 3,4)		
OS13			10	—	25	MHz	HS (Note 4)		
OS14			10		25	MHz	HSPLL (Notes 3,4)		
OS15			32	32.768	100	kHz	Sosc (Note 4)		
OS20	Tosc	Tosc = 1/Fosc = Tcy (Note 2)	_	—	_	_	See parameter OS10 for Fosc value		
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.45 x Tosc	—	—	ns	EC (Note 4)		
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	_	—	0.05 x Tosc	ns	EC (Note 4)		
OS40	Tost	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	_	1024	_	Tosc	(Note 4)		
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 4)		
OS42	Gм	External Oscillator Transconductance (Primary Oscillator only)	_	12		mA/V	VDD = 3.3V, TA = +25°C (Note 4)		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

- 2: Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.
- **3:** PLL input requirements: 4 MHz \leq FPLLIN \leq 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 4: This parameter is characterized, but not tested in manufacturing.



FIGURE 31-12: SPIX MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

TABLE 31-31: SPIX MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS				$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions			
SP70	TscL	SCKx Input Low Time (Note 3)	Tsck/2	—	—	ns	—			
SP71	TscH	SCKx Input High Time (Note 3)	Tsck/2	—	_	ns	—			
SP72	TscF	SCKx Input Fall Time	—		—	ns	See parameter DO32			
SP73	TscR	SCKx Input Rise Time	—	_		ns	See parameter DO31			
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	_			ns	See parameter DO32			
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	_		ns	See parameter DO31			
SP35	TscH2doV,	SDOx Data Output Valid after	—	—	15	ns	VDD > 2.7V			
	TscL2DoV	SCKx Edge			20	ns	VDD < 2.7V			
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10			ns	_			
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10			ns	_			
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \uparrow or SCKx Input	175	—		ns	_			
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance (Note 3)	5	_	25	ns	_			

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 3: The minimum clock period for SCKx is 40 ns.
- 4: Assumes 50 pF load on all SPIx pins.

AC CHARACTERISTICS			$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions		
Clock Parameters									
AD50	TAD	ADC Clock Period ⁽²⁾	65	—	_	ns	See Table 31-36		
Conversion Rate									
AD55	ΤΟΟΝΛ	Conversion Time	—	12 Tad	_		—		
AD56	FCNV	Throughput Rate (Sampling Speed) ⁽⁴⁾		—	1000	ksps	AVDD = 3.0V to 3.6V		
				—	400	ksps	AVDD = 2.5V to 3.6V		
AD57	TSAMP	Sample Time	2 TAD	—	—	_	—		
Timing	Paramete	rs							
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾	_	1.0 Tad	—	_	Auto-Convert Trigger (SSRC<2:0> = 111) not selected		
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 Tad		1.5 TAD	_	—		
AD62	Tcss	Conversion Completion to Sample Start (ASAM = 1) ⁽³⁾	_	0.5 TAD	_		_		
AD63	Tdpu	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽³⁾	—	_	2	μS	—		

TABLE 31-37: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: Refer to Table 31-36 for detailed conditions.



PIC32MX330/350/370/430/450/470