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#### Details

|                            |                                                                                                                                                                               |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Obsolete                                                                                                                                                                      |
| Core Processor             | MIPS32® M4K™                                                                                                                                                                  |
| Core Size                  | 32-Bit Single-Core                                                                                                                                                            |
| Speed                      | 80MHz                                                                                                                                                                         |
| Connectivity               | I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG                                                                                                                 |
| Peripherals                | Brown-out Detect/Reset, DMA, POR, PWM, WDT                                                                                                                                    |
| Number of I/O              | 85                                                                                                                                                                            |
| Program Memory Size        | 64KB (64K x 8)                                                                                                                                                                |
| Program Memory Type        | FLASH                                                                                                                                                                         |
| EEPROM Size                | -                                                                                                                                                                             |
| RAM Size                   | 16K x 8                                                                                                                                                                       |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V                                                                                                                                                                   |
| Data Converters            | A/D 28x10b                                                                                                                                                                    |
| Oscillator Type            | Internal                                                                                                                                                                      |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                             |
| Mounting Type              | Surface Mount                                                                                                                                                                 |
| Package / Case             | 124-VFTLA Dual Rows, Exposed Pad                                                                                                                                              |
| Supplier Device Package    | 124-VTLA (9x9)                                                                                                                                                                |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx430f064lt-i-tl">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx430f064lt-i-tl</a> |

# PIC32MX330/350/370/430/450/470

## 1.0 DEVICE OVERVIEW

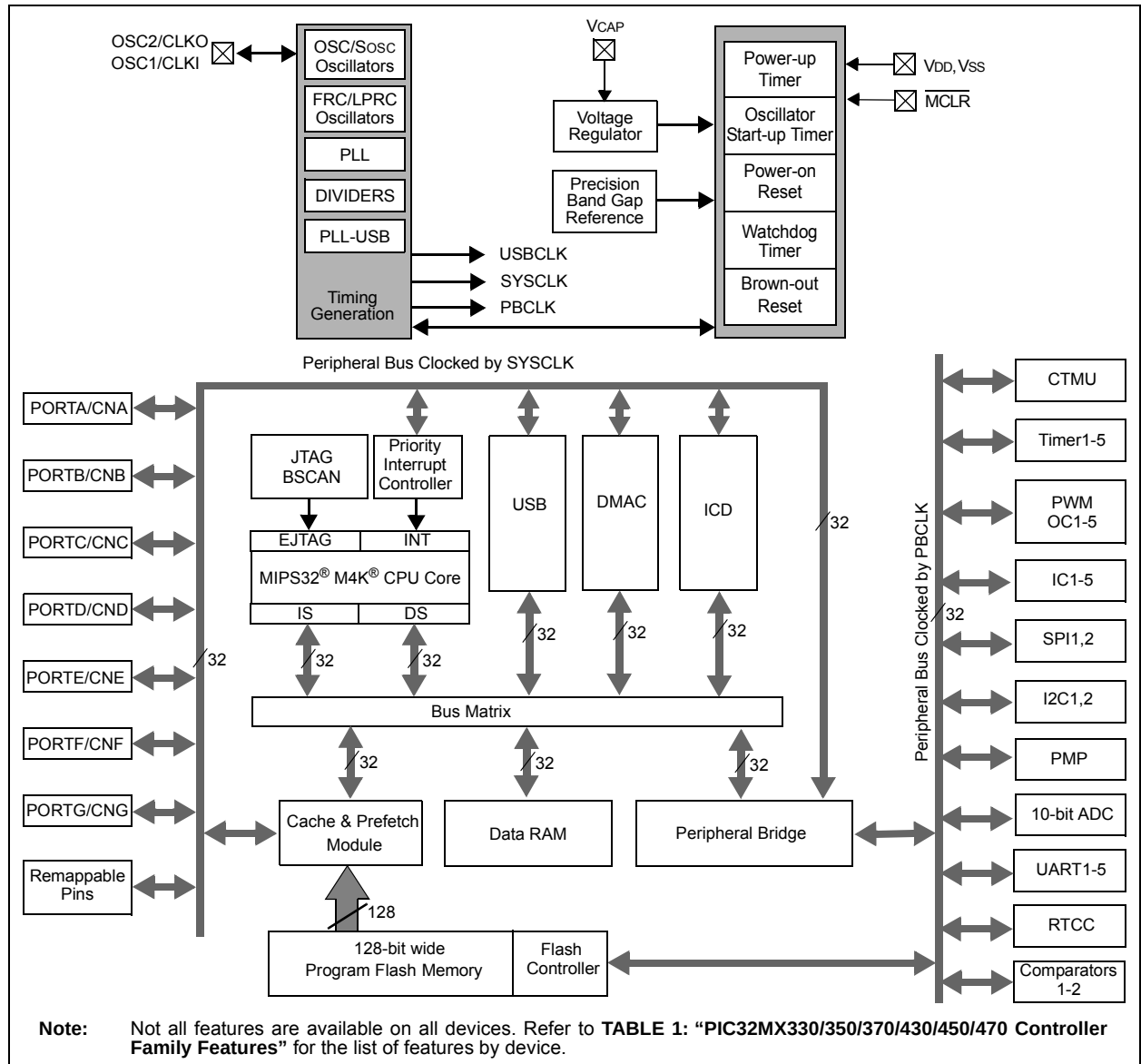
**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

This document contains device-specific information for PIC32MX330/350/370/430/450/470 devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX330/350/370/430/450/470 family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: PIC32MX330/350/370/430/450/470 BLOCK DIAGRAM**



## 4.2 Bus Matrix Registers

**TABLE 4-2: BUS MATRIX REGISTER MAP**

| Virtual Address<br>(BF88_#) | Register<br>Name        | Bit Range | Bits            |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | All<br>Resets |
|-----------------------------|-------------------------|-----------|-----------------|-------|-------|-------|-------|-----------|------|------|------|----------|------|-----------------|-----------|-------------|----------|----------|---------------|
|                             |                         |           | 31/15           | 30/14 | 29/13 | 28/12 | 27/11 | 26/10     | 25/9 | 24/8 | 23/7 | 22/6     | 21/5 | 20/4            | 19/3      | 18/2        | 17/1     | 16/0     |               |
| 2000                        | BMXCON <sup>(1)</sup>   | 31:16     | —               | —     | —     | —     | —     | BMXCHEDMA | —    | —    | —    | —        | —    | BMXERRIXI       | BMXERRICD | BMXERRDMA   | BMXERRDS | BMXERRIS | 041F          |
|                             |                         | 15:0      | —               | —     | —     | —     | —     | —         | —    | —    | —    | BMXWSDRM | —    | —               | —         | BMXARB<2:0> |          |          | 0047          |
| 2010                        | BMXDKPBA <sup>(1)</sup> | 31:16     | —               | —     | —     | —     | —     | —         | —    | —    | —    | —        | —    | —               | —         | —           | —        | —        | 0000          |
|                             |                         | 15:0      | BMXDKPBA<15:0>  |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | 0000          |
| 2020                        | BMXDUDBA <sup>(1)</sup> | 31:16     | —               | —     | —     | —     | —     | —         | —    | —    | —    | —        | —    | —               | —         | —           | —        | —        | 0000          |
|                             |                         | 15:0      | BMXDUDBA<15:0>  |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | 0000          |
| 2030                        | BMXDUPBA <sup>(1)</sup> | 31:16     | —               | —     | —     | —     | —     | —         | —    | —    | —    | —        | —    | —               | —         | —           | —        | —        | 0000          |
|                             |                         | 15:0      | BMXDUPBA<15:0>  |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | 0000          |
| 2040                        | BMXDRMSZ                | 31:16     | BMXDRMSZ<31:0>  |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | XXXX          |
|                             |                         | 15:0      |                 |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | XXXX          |
| 2050                        | BMXPUPBA <sup>(1)</sup> | 31:16     | —               | —     | —     | —     | —     | —         | —    | —    | —    | —        | —    | BMXPUPBA<19:16> |           |             |          |          | 0000          |
|                             |                         | 15:0      | BMXPUPBA<15:0>  |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | 0000          |
| 2060                        | BMXPFMSZ                | 31:16     | BMXPFMSZ<31:0>  |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | XXXX          |
|                             |                         | 15:0      |                 |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | XXXX          |
| 2070                        | BMXBOOTSZ               | 31:16     | BMXBOOTSZ<31:0> |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | 0000          |
|                             |                         | 15:0      |                 |       |       |       |       |           |      |      |      |          |      |                 |           |             |          |          | 0000          |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 “CLR, SET, and INV Registers” for more information.

## 6.0 RESETS

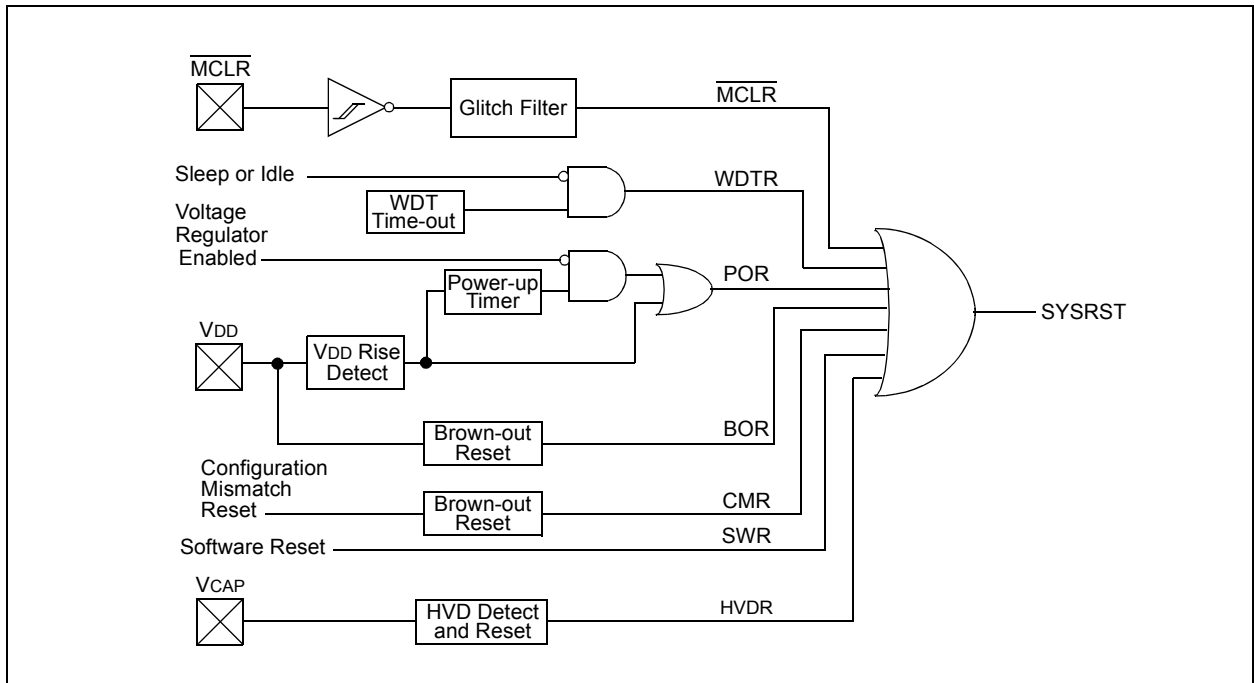
**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS60001118), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Master Clear Reset pin
- SWR: Software Reset
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset
- HVDR: High Voltage Detect Reset

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

**FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM**



## 6.1 Reset Control Registers

**TABLE 6-1: SYSTEM CONTROL REGISTER MAP**

| Virtual Address<br>(BF80_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits  |       |       |       |       |       |      |       |      |      |      |      |       |      |      |       | All Resets          |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|-------|-------|------|-------|------|------|------|------|-------|------|------|-------|---------------------|
|                             |                                 |           | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8  | 23/7 | 22/6 | 21/5 | 20/4 | 19/3  | 18/2 | 17/1 | 16/0  |                     |
| F600                        | RCON                            | 31:16     | —     | —     | HVDR  | —     | —     | —     | —    | —     | —    | —    | —    | —    | —     | —    | —    | —     | 0000                |
|                             |                                 | 15:0      | —     | —     | —     | —     | —     | —     | CMR  | VREGS | EXTR | SWR  | —    | WDTO | SLEEP | IDLE | BOR  | POR   | xxxx <sup>(2)</sup> |
| F610                        | RSWRST                          | 31:16     | —     | —     | —     | —     | —     | —     | —    | —     | —    | —    | —    | —    | —     | —    | —    | —     | 0000                |
|                             |                                 | 15:0      | —     | —     | —     | —     | —     | —     | —    | —     | —    | —    | —    | —    | —     | —    | —    | SWRST | 0000                |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.
- 2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

## REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

- bit 6     **CRCAPP:** CRC Append Mode bit<sup>(1)</sup>  
1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA  
0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5     **CRCTYP:** CRC Type Selection bit  
1 = The CRC module will calculate an IP header checksum  
0 = The CRC module will calculate a LFSR CRC
- bit 4-3   **Unimplemented:** Read as '0'
- bit 2-0   **CRCCH<2:0>:** CRC Channel Select bits  
111 = CRC is assigned to Channel 7  
110 = CRC is assigned to Channel 6  
101 = CRC is assigned to Channel 5  
100 = CRC is assigned to Channel 4  
011 = CRC is assigned to Channel 3  
010 = CRC is assigned to Channel 2  
001 = CRC is assigned to Channel 1  
000 = CRC is assigned to Channel 0

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

**TABLE 12-5: PORTC REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, PIC32MX370F512L, PIC32MX430F064L, PIC32MX450F128L, PIC32MX450F256L, AND PIC32MX470F512L DEVICES ONLY**

| Virtual Address<br>(BF88_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits      |           |           |           |       |       |      |      |      |      |      |          |          |          |          |      | All<br>Resets |
|-----------------------------|---------------------------------|-----------|-----------|-----------|-----------|-----------|-------|-------|------|------|------|------|------|----------|----------|----------|----------|------|---------------|
|                             |                                 |           | 31/15     | 30/14     | 29/13     | 28/12     | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4     | 19/3     | 18/2     | 17/1     | 16/0 |               |
| 6210                        | TRISC                           | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | TRISC15   | TRISC14   | TRISC13   | TRISC12   | —     | —     | —    | —    | —    | —    | —    | TRISC4   | TRISC3   | TRISC2   | TRISC1   | —    | xxxx          |
| 6220                        | PORTC                           | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | RC15      | RC14      | RC13      | RC12      | —     | —     | —    | —    | —    | —    | —    | RC4      | RC3      | RC2      | RC1      | —    | xxxx          |
| 6230                        | LATC                            | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | LATC15    | LATC14    | LATC13    | LATC12    | —     | —     | —    | —    | —    | —    | —    | LATC4    | LATC3    | LATC2    | LATC1    | —    | xxxx          |
| 6240                        | ODCC                            | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | ODCC15    | ODCC14    | ODCC13    | ODCC12    | —     | —     | —    | —    | —    | —    | —    | ODCC4    | ODCC3    | ODCC2    | ODCC1    | —    | xxxx          |
| 6250                        | CNPUC                           | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | CNPUC15   | CNPUC14   | CNPUC13   | CNPUC12   | —     | —     | —    | —    | —    | —    | —    | CNPUC4   | CNPUC3   | CNPUC2   | CNPUC1   | —    | xxxx          |
| 6260                        | CNPDC                           | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | CNPDC15   | CNPDC14   | CNPDC13   | CNPDC12   | —     | —     | —    | —    | —    | —    | —    | CNPDC4   | CNPDC3   | CNPDC2   | CNPDC1   | —    | xxxx          |
| 6270                        | CNCONC                          | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | ON        | —         | SIDL      | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
| 6280                        | CNENC                           | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | CNIEC15   | CNIEC14   | CNIEC13   | CNIEC12   | —     | —     | —    | —    | —    | —    | —    | CNIEC4   | CNIEC3   | CNIEC2   | CNIEC1   | —    | xxxx          |
| 6290                        | CNSTATC                         | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                                 | 15:0      | CNSTATC15 | CNSTATC14 | CNSTATC13 | CNSTATC12 | —     | —     | —    | —    | —    | —    | —    | CNSTATC4 | CNSTATC3 | CNSTATC2 | CNSTATC1 | —    | xxxx          |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

# PIC32MX330/350/370/430/450/470

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## REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 2      **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:

1 = External clock input is synchronized

0 = External clock input is not synchronized

When TCS = 0:

This bit is ignored.

bit 1      **TCS:** Timer Clock Source Select bit

1 = External clock from TxCKI pin

0 = Internal peripheral clock

bit 0      **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.



## 14.0 TIMER2/3, TIMER4/5

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The PIC32MX330/350/370/430/450/470 family of devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

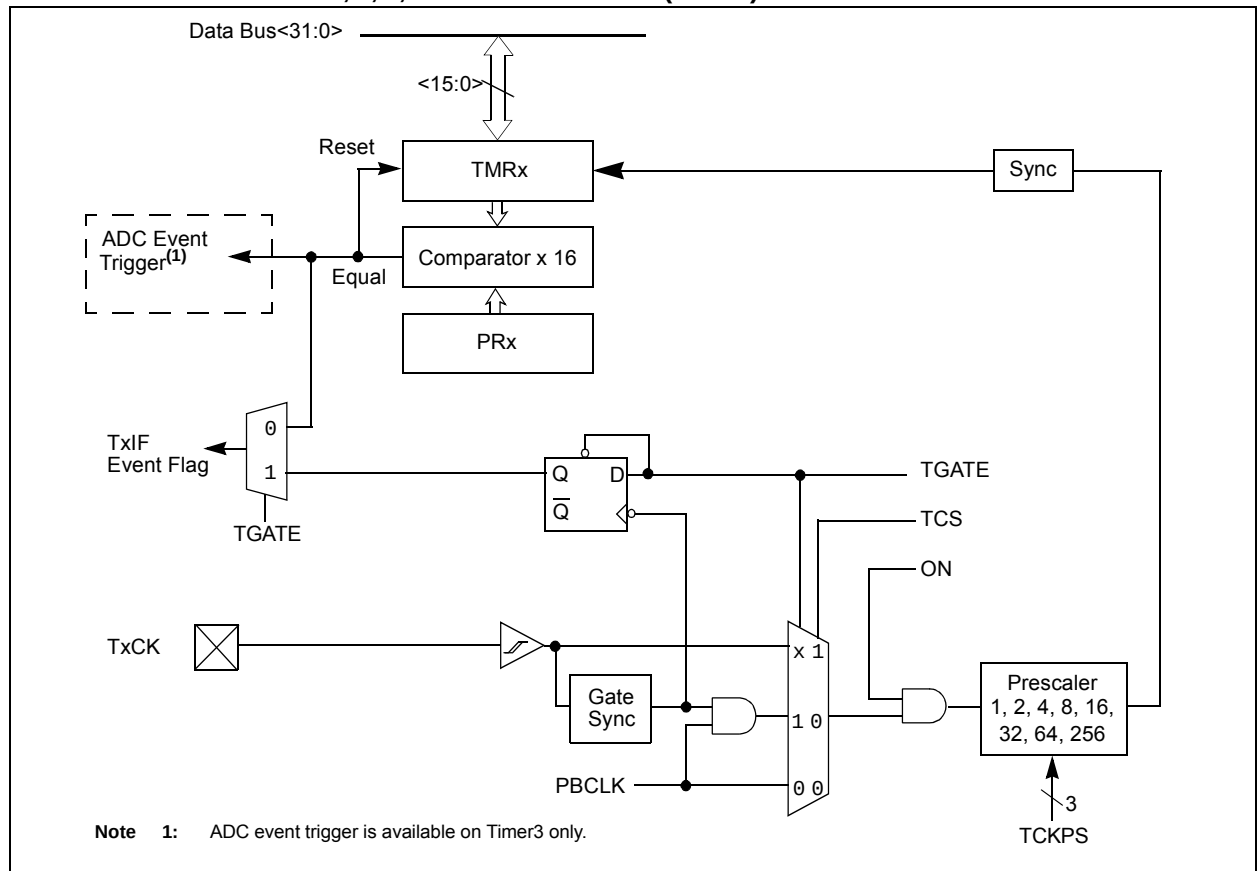
- Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

**Note:** In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through 5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or 4; 'y' represents Timer3 or 5.

### 14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 in 16-bit mode, Timer2/3 in 32-bit mode)
- Fast bit manipulation using CLR, SET, and INV registers

**FIGURE 14-1: TIMER2, 3, 4, 5 BLOCK DIAGRAM (16-BIT)**



# PIC32MX330/350/370/430/450/470

## 15.0 WATCHDOG TIMER (WDT)

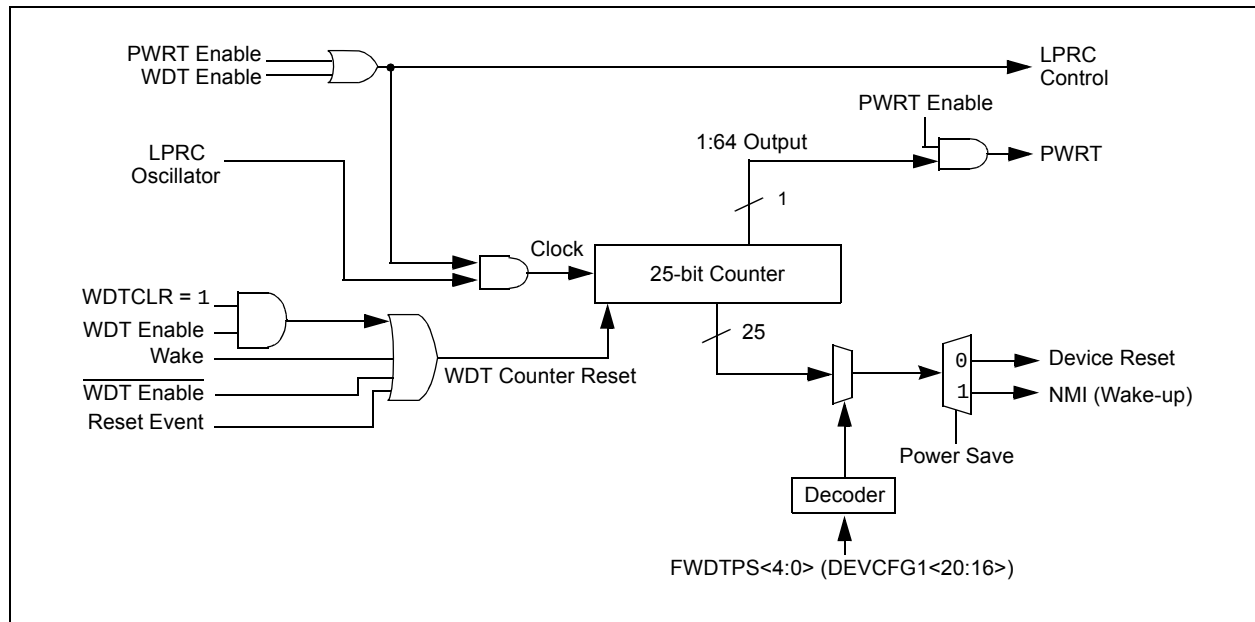
**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog, Deadman, and Power-up Timers”** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

**FIGURE 15-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM**



## 17.0 OUTPUT COMPARE

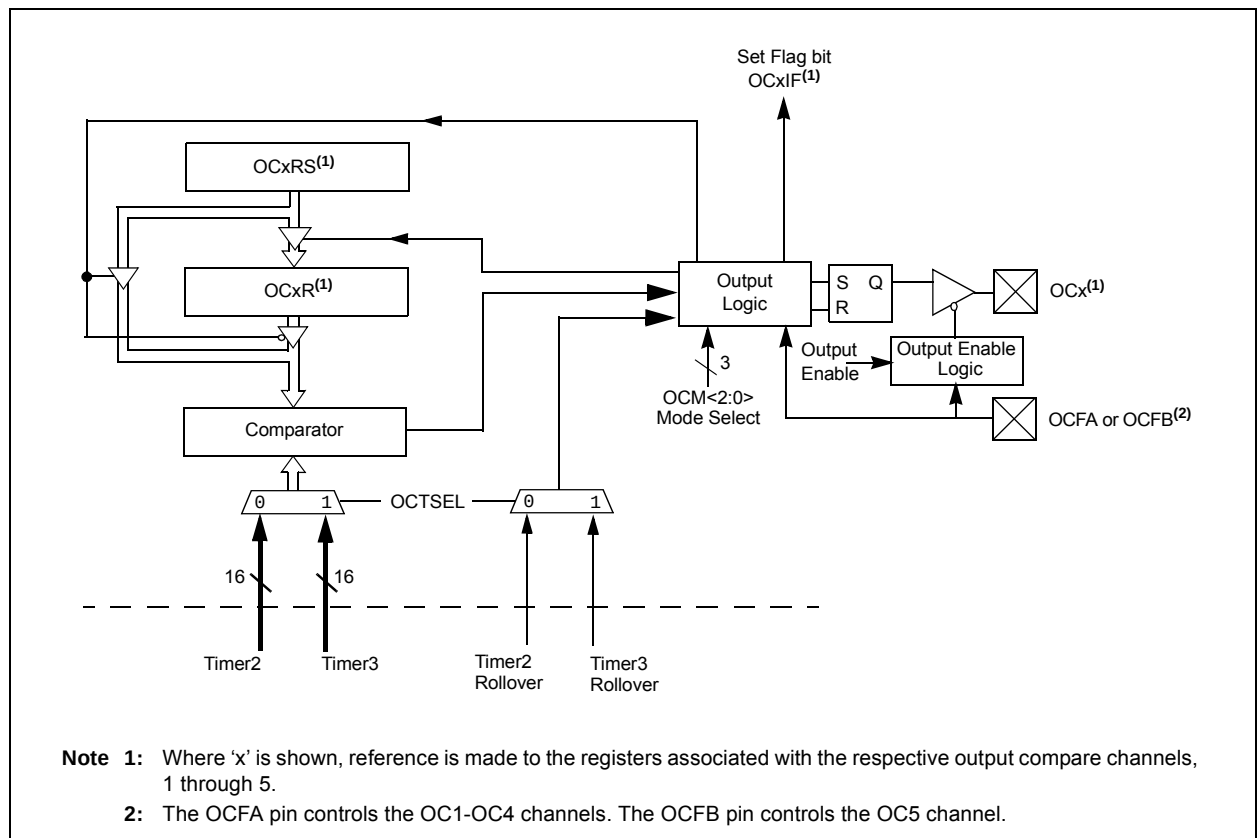
**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. “Output Compare”** (DS60001111), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of this module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

**FIGURE 17-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM**



# PIC32MX330/350/370/430/450/470

**REGISTER 18-2: SPIxCON2: SPI CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7                | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4    | Bit 27/19/11/3                    | Bit 26/18/10/2    | Bit 25/17/9/1                         | Bit 24/16/8/0   |
|-----------|-------------------------------|----------------|----------------|-------------------|-----------------------------------|-------------------|---------------------------------------|-----------------|
| 31:24     | U-0<br>—                      | U-0<br>—       | U-0<br>—       | U-0<br>—          | U-0<br>—                          | U-0<br>—          | U-0<br>—                              | U-0<br>—        |
| 23:16     | U-0<br>—                      | U-0<br>—       | U-0<br>—       | U-0<br>—          | U-0<br>—                          | U-0<br>—          | U-0<br>—                              | U-0<br>—        |
| 15:8      | R/W-0<br>SPISGNEXT            | U-0<br>—       | U-0<br>—       | R/W-0<br>FRMERREN | R/W-0<br>SPIROVEN                 | R/W-0<br>SPITUREN | R/W-0<br>IGNROV                       | R/W-0<br>IGNTUR |
| 7:0       | R/W-0<br>AUDEN <sup>(1)</sup> | U-0<br>—       | U-0<br>—       | U-0<br>—          | R/W-0<br>AUDMONO <sup>(1,2)</sup> | U-0<br>—          | R/W-0<br>AUDMOD<1:0> <sup>(1,2)</sup> | R/W-0<br>—      |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit

1 = Data from RX FIFO is sign extended

0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit

1 = Frame Error overflow generates error events

0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit

1 = Receive overflow generates error events

0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit

1 = Transmit Underrun Generates Error Events

0 = Transmit Underrun Does Not Generates Error Events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)

1 = A ROV is not a critical error; during ROV data in the fifo is not overwritten by receive data

0 = A ROV is a critical error which stop SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)

1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty

0 = A TUR is a critical error which stop SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit<sup>(1)</sup>

1 = Audio protocol is enabled

0 = Audio protocol is disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit<sup>(1,2)</sup>

1 = Audio data is mono (Each data word is transmitted on both left and right channels)

0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit<sup>(1,2)</sup>

11 = PCM/DSP mode

10 = Right Justified mode

01 = Left Justified mode

00 = I<sup>2</sup>S mode

**Note 1:** This bit can only be written when the ON bit = 0.

**2:** This bit is only valid for AUDEN = 1.

## 19.0 INTER-INTEGRATED CIRCUIT (I<sup>2</sup>C)

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I<sup>2</sup>C)”** (DS60001116), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The I<sup>2</sup>C module provides complete hardware support for both Slave and Multi-Master modes of the I<sup>2</sup>C serial communication standard. Figure 19-1 illustrates the I<sup>2</sup>C module block diagram.

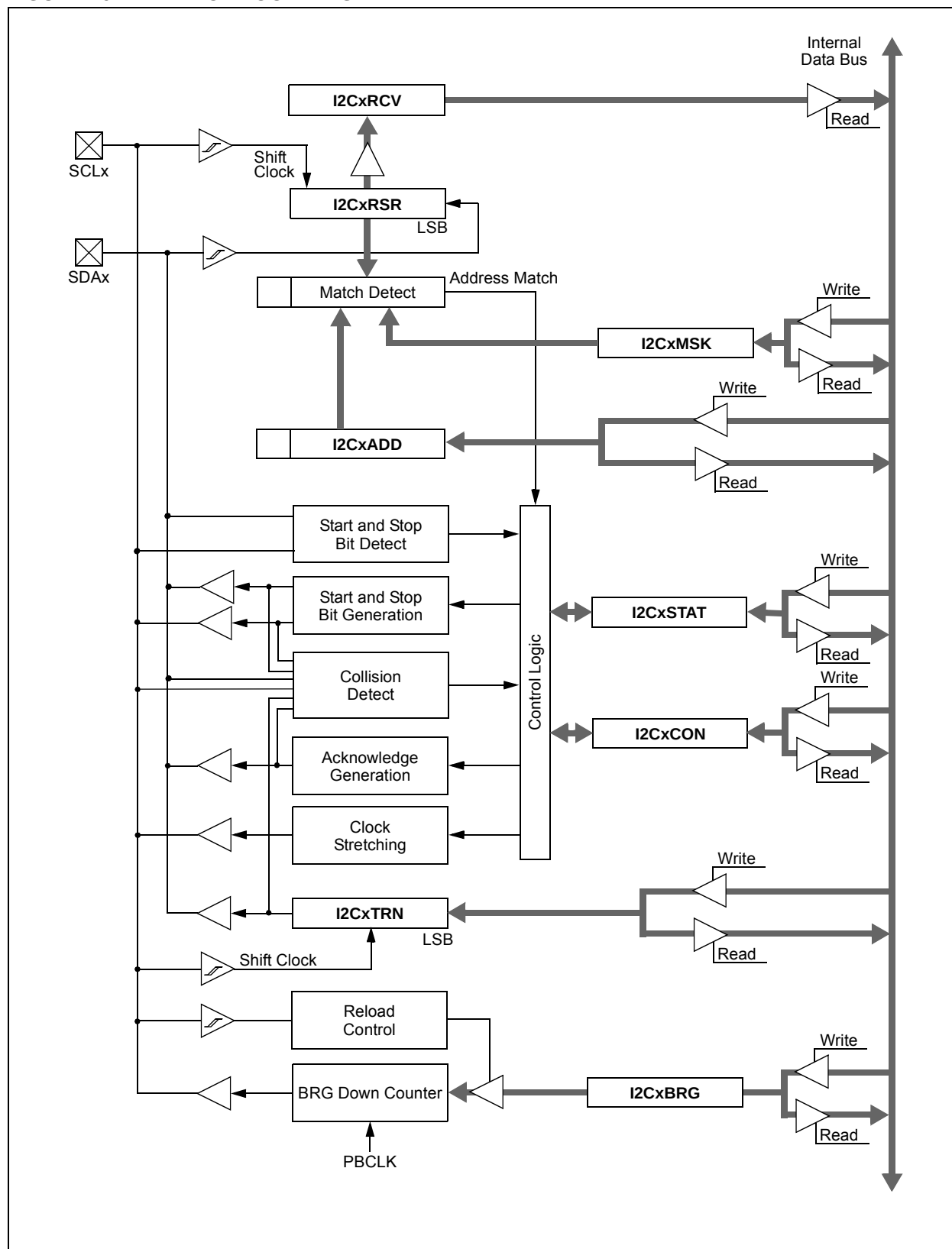
Each I<sup>2</sup>C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I<sup>2</sup>C module offers the following key features:

- I<sup>2</sup>C interface supporting both master and slave operation
- I<sup>2</sup>C Slave mode supports 7-bit and 10-bit addressing
- I<sup>2</sup>C Master mode supports 7-bit and 10-bit addressing
- I<sup>2</sup>C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I<sup>2</sup>C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I<sup>2</sup>C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

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FIGURE 19-1: I<sup>2</sup>C BLOCK DIAGRAM



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NOTES:

## 25.1 Control Register

**TABLE 25-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP**

| Virtual Address<br>(BF80_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits  |       |       |       |       |       |      |      |      |       |      |       |          |      |      |      | All Resets |
|-----------------------------|---------------------------------|-----------|-------|-------|-------|-------|-------|-------|------|------|------|-------|------|-------|----------|------|------|------|------------|
|                             |                                 |           | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6  | 21/5 | 20/4  | 19/3     | 18/2 | 17/1 | 16/0 |            |
| 9800                        | CVRCON                          | 31:16     | —     | —     | —     | —     | —     | —     | —    | —    | —    | —     | —    | —     | —        | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | ON    | —     | —     | —     | —     | —     | —    | —    | —    | CVROE | CVRR | CVRSS | CVR<3:0> |      |      |      | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.



## REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

- bit 10 **EDGSEQEN**: Edge Sequence Enable bit  
 1 = Edge 1 must occur before Edge 2 can occur  
 0 = No edge sequence is needed
- bit 9 **IDISSEN**: Analog Current Source Control bit<sup>(2)</sup>  
 1 = Analog current source output is grounded  
 0 = Analog current source output is not grounded
- bit 8 **CTTRIG**: Trigger Control bit  
 1 = Trigger output is enabled  
 0 = Trigger output is disabled
- bit 7-2 **ITRIM<5:0>**: Current Source Trim bits  
 011111 = Maximum positive change from nominal current  
 011110  
 .  
 .  
 .  
 000001 = Minimum positive change from nominal current  
 000000 = Nominal current output specified by IRNG<1:0>  
 111111 = Minimum negative change from nominal current  
 .  
 .  
 .  
 100010  
 100001 = Maximum negative change from nominal current
- bit 1-0 **IRNG<1:0>**: Current Range Select bits<sup>(3)</sup>  
 11 = 100 times base current  
 10 = 10 times base current  
 01 = Base current level  
 00 = 1000 times base current<sup>(4)</sup>

- Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
- 2:** The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
- 3:** Refer to the CTMU Current Source Specifications (Table 31-42) in **Section 31.0 "Electrical Characteristics"** for current values.
- 4:** This bit setting is not available for the CTMU temperature diode.

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## REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

- bit 15-14 **FCKSM<1:0>**: Clock Switching and Monitor Selection Configuration bits  
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled  
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled  
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
- bit 13-12 **FPBDIV<1:0>**: Peripheral Bus Clock Divisor Default Value bits  
11 = PBCLK is SYSCLK divided by 8  
10 = PBCLK is SYSCLK divided by 4  
01 = PBCLK is SYSCLK divided by 2  
00 = PBCLK is SYSCLK divided by 1
- bit 11 **Reserved**: Write '1'
- bit 10 **OSCIOFNC**: CLKO Enable Configuration bit  
1 = CLKO output is disabled  
0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)
- bit 9-8 **POSCMOD<1:0>**: Primary Oscillator Configuration bits  
11 = Primary Oscillator is disabled  
10 = HS Oscillator mode is selected  
01 = XT Oscillator mode is selected  
00 = External Clock mode is selected
- bit 7 **IESO**: Internal External Switchover bit  
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)  
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)
- bit 6 **Reserved**: Write '1'
- bit 5 **FSOSCEN**: Secondary Oscillator Enable bit  
1 = Enable Secondary Oscillator  
0 = Disable Secondary Oscillator
- bit 4-3 **Reserved**: Write '1'
- bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits  
111 = Fast RC Oscillator with divide-by-N (FRCDIV)  
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler  
101 = Low-Power RC Oscillator (LPRC)  
100 = Secondary Oscillator (Sosc)  
011 = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL)  
010 = Primary Oscillator (XT, HS, EC)<sup>(1)</sup>  
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)  
000 = Fast RC Oscillator (FRC)

**Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

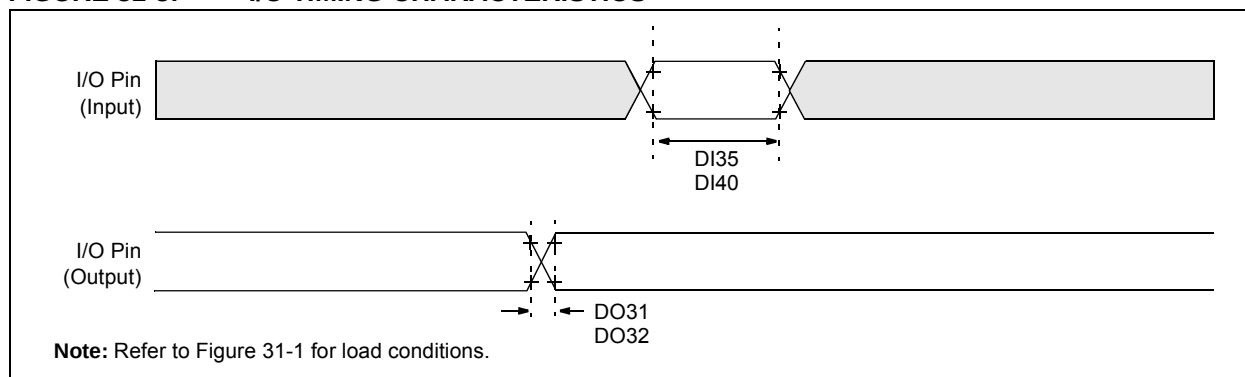
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**TABLE 31-21: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS                    |                 | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for Commercial<br>$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial<br>$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp |         |      |       |            |
|---------------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------|-------|------------|
| Param. No.                            | Characteristics | Min.                                                                                                                                                                                                                                                                                                                    | Typical | Max. | Units | Conditions |
| <b>LPRC @ 31.25 kHz<sup>(1)</sup></b> |                 |                                                                                                                                                                                                                                                                                                                         |         |      |       |            |
| F21                                   | LPRC            | -15                                                                                                                                                                                                                                                                                                                     | —       | +15  | %     | —          |

**Note 1:** Change of LPRC frequency as VDD changes.

**FIGURE 31-3: I/O TIMING CHARACTERISTICS**



**TABLE 31-22: I/O TIMING REQUIREMENTS**

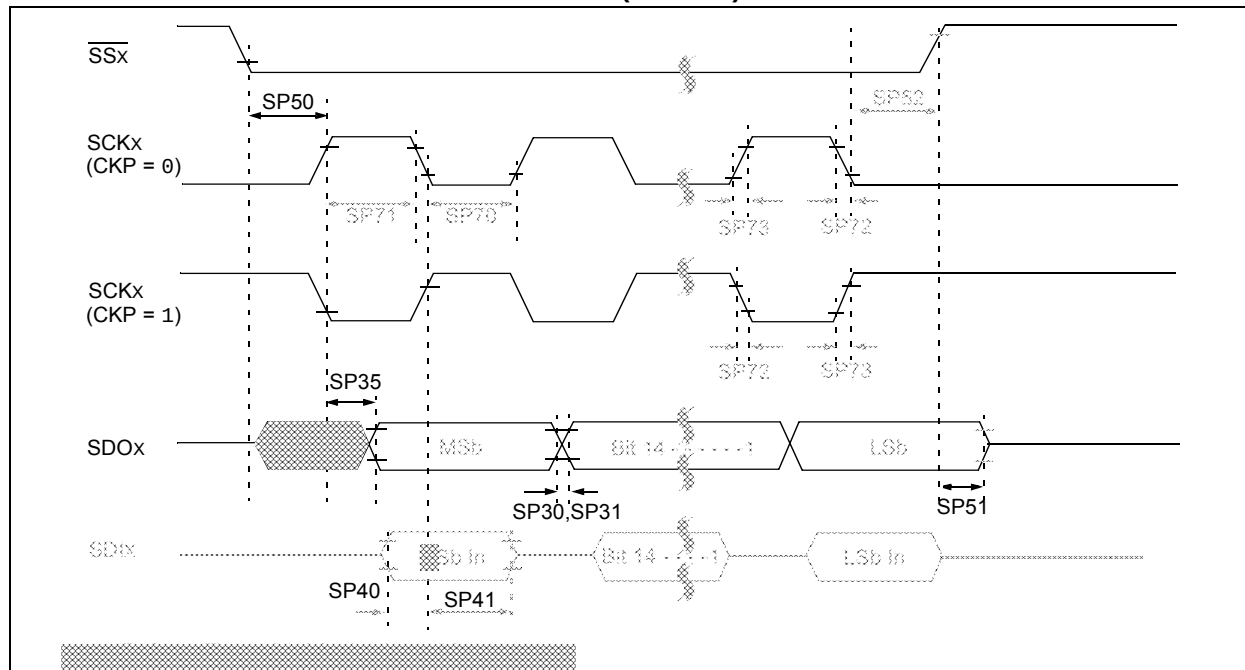
| AC CHARACTERISTICS |        | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for Commercial<br>$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial<br>$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp |      |                        |      |         |            |
|--------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------------------------|------|---------|------------|
| Param. No.         | Symbol | Characteristics <sup>(2)</sup>                                                                                                                                                                                                                                                                                          | Min. | Typical <sup>(1)</sup> | Max. | Units   | Conditions |
| DO31               | TioR   | Port Output Rise Time                                                                                                                                                                                                                                                                                                   | —    | 5                      | 15   | ns      | VDD < 2.5V |
|                    |        |                                                                                                                                                                                                                                                                                                                         | —    | 5                      | 10   | ns      | VDD > 2.5V |
| DO32               | TioF   | Port Output Fall Time                                                                                                                                                                                                                                                                                                   | —    | 5                      | 15   | ns      | VDD < 2.5V |
|                    |        |                                                                                                                                                                                                                                                                                                                         | —    | 5                      | 10   | ns      | VDD > 2.5V |
| DI35               | TINP   | INTx Pin High or Low Time                                                                                                                                                                                                                                                                                               | 10   | —                      | —    | ns      | —          |
| DI40               | TRBP   | CNx High or Low Time (input)                                                                                                                                                                                                                                                                                            | 2    | —                      | —    | TSYSCLK | —          |

**Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

**Note 2:** This parameter is characterized, but not tested in manufacturing.

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**FIGURE 31-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS**



**TABLE 31-31: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS |                       |                                                 |        | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |      |       |                    |
|--------------------|-----------------------|-------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|--------------------|
| Param. No.         | Symbol                | Characteristics <sup>(1)</sup>                  | Min.   | Typ. <sup>(2)</sup>                                                                                                                                                                                      | Max. | Units | Conditions         |
| SP70               | TscL                  | SCKx Input Low Time (Note 3)                    | Tsck/2 | —                                                                                                                                                                                                        | —    | ns    | —                  |
| SP71               | TscH                  | SCKx Input High Time (Note 3)                   | Tsck/2 | —                                                                                                                                                                                                        | —    | ns    | —                  |
| SP72               | TscF                  | SCKx Input Fall Time                            | —      | —                                                                                                                                                                                                        | —    | ns    | See parameter DO32 |
| SP73               | TscR                  | SCKx Input Rise Time                            | —      | —                                                                                                                                                                                                        | —    | ns    | See parameter DO31 |
| SP30               | Tdof                  | SDOx Data Output Fall Time (Note 4)             | —      | —                                                                                                                                                                                                        | —    | ns    | See parameter DO32 |
| SP31               | Tdor                  | SDOx Data Output Rise Time (Note 4)             | —      | —                                                                                                                                                                                                        | —    | ns    | See parameter DO31 |
| SP35               | Tsch2doV,<br>TscL2doV | SDOx Data Output Valid after<br>SCKx Edge       | —      | —                                                                                                                                                                                                        | 15   | ns    | VDD > 2.7V         |
|                    |                       |                                                 | —      | —                                                                                                                                                                                                        | 20   | ns    | VDD < 2.7V         |
| SP40               | TdIV2sch,<br>TdIV2scl | Setup Time of SDIx Data Input<br>to SCKx Edge   | 10     | —                                                                                                                                                                                                        | —    | ns    | —                  |
| SP41               | Tsch2diL,<br>TscL2diL | Hold Time of SDIx Data Input<br>to SCKx Edge    | 10     | —                                                                                                                                                                                                        | —    | ns    | —                  |
| SP50               | TssL2sch,<br>TssL2scl | SSx ↓ to SCKx ↑ or SCKx Input                   | 175    | —                                                                                                                                                                                                        | —    | ns    | —                  |
| SP51               | TssH2doZ              | SSx ↑ to SDOx Output<br>High-Impedance (Note 3) | 5      | —                                                                                                                                                                                                        | 25   | ns    | —                  |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**Note 2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

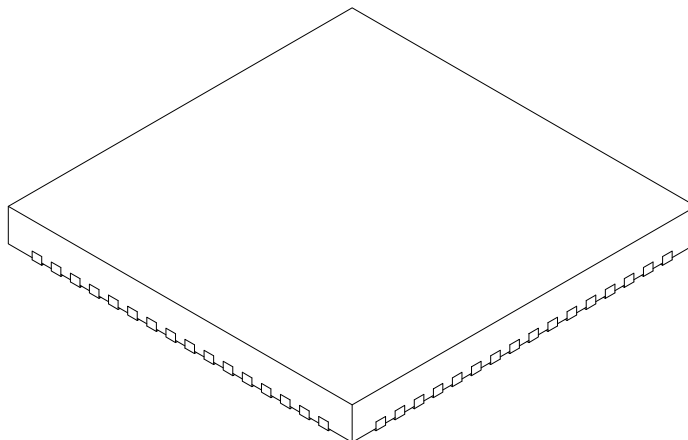
**Note 3:** The minimum clock period for SCKx is 40 ns.

**Note 4:** Assumes 50 pF load on all SPIx pins.

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## 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                  |    | MILLIMETERS |      |      |
|------------------------|----|-------------|------|------|
| Dimension Limits       |    | MIN         | NOM  | MAX  |
| Number of Pins         | N  | 64          |      |      |
| Pitch                  | e  | 0.50 BSC    |      |      |
| Overall Height         | A  | 0.80        | 0.90 | 1.00 |
| Standoff               | A1 | 0.00        | 0.02 | 0.05 |
| Contact Thickness      | A3 | 0.20 REF    |      |      |
| Overall Width          | E  | 9.00 BSC    |      |      |
| Exposed Pad Width      | E2 | 5.30        | 5.40 | 5.50 |
| Overall Length         | D  | 9.00 BSC    |      |      |
| Exposed Pad Length     | D2 | 5.30        | 5.40 | 5.50 |
| Contact Width          | b  | 0.20        | 0.25 | 0.30 |
| Contact Length         | L  | 0.30        | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K  | 0.20        | -    | -    |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2