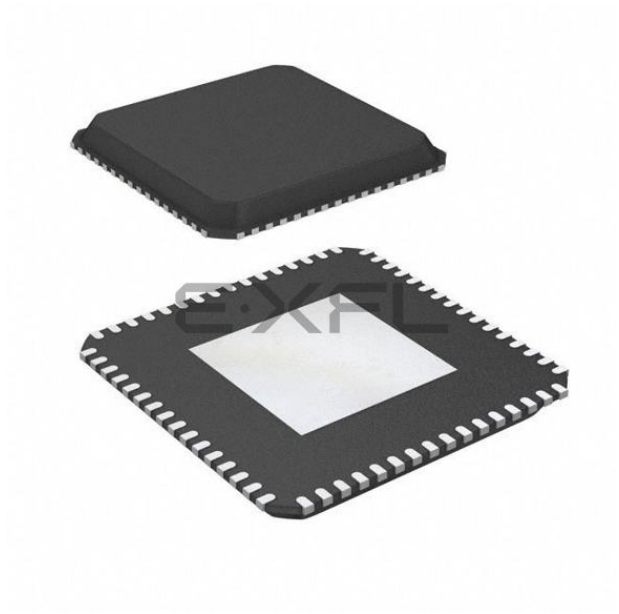

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx450f128h-v-rg

TABLE 4: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW)(1,2,3)

PIC32MX330F064L
PIC32MX350F128L
PIC32MX350F256L
PIC32MX370F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RG15	36	VSS
2	VDD	37	VDD
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	RPF13/RF13
5	AN27/PMD7/RE7	40	RPF12/RF12
6	RPC1/RC1	41	AN12/PMA11/RB12
7	RPC2/RC2	42	AN13/PMA10/RB13
8	RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	VSS
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD
12	AN18/C2IND/RPG8/PMA3/RG8	47	RPD14/RD14
13	$\overline{\text{MCLR}}$	48	RPD15/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	VSS	50	RPF5/PMA8/RF5
16	VDD	51	RPF3/RF3
17	TMS/CTED1/RA0	52	RPF2/RF2
18	RPE8/RE8	53	RPF8/RF8
19	RPE9/RE9	54	RPF7/RF7
20	AN5/C1INA/RPB5/RB5	55	RPF6/SCK1/INT0/RF6
21	AN4/C1INB/RB4	56	SDA1/RG3
22	PGED3/AN3/C2INA/RPB3/RB3	57	SCL1/RG2
23	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/CVREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	RPA14/RA14
32	AN8/RPB8/CTED10/RB8	67	RPA15/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/PMCS2/RD10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx), with the exception of RF6, can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: RPF6 (pin 55) and RPF7 (pin 54) are only remappable for input functions.

TABLE 4: PIN NAMES FOR 100-PIN DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)(1,2,3)

PIC32MX330F064L
PIC32MX350F128L
PIC32MX350F256L
PIC32MX370F512L

Pin #	Full Pin Name	Pin #	Full Pin Name
71	RPD11/PMCS1/RD11	86	VDD
72	RPD0/RD0	87	RPF0/PMD11/RF0
73	SOSCI/RPC13/RC13	88	RPF1/PMD10/RF1
74	SOSCO/RPC14/T1CK/RC14	89	RPG1/PMD9/RG1
75	VSS	90	RPG0/PMD8/RG0
76	AN24/RPD1/RD1	91	TRCLK/RA6
77	AN25/RPD2/RD2	92	TRD3/CTED8/RA7
78	AN26/RPD3/RD3	93	PMD0/RE0
79	RPD12/PMD12/RD12	94	PMD1/RE1
80	PMD13/RD13	95	TRD2/RG14
81	RPD4/PMWR/RD4	96	TRD1/RG12
82	RPD5/PMRD/RD5	97	TRD0/RG13
83	PMD14/RD6	98	AN20/PMD2/RE2
84	PMD15/RD7	99	RPE3/CTPLS/PMD3/RE3
85	VCAP	100	AN21/PMD4/RE4

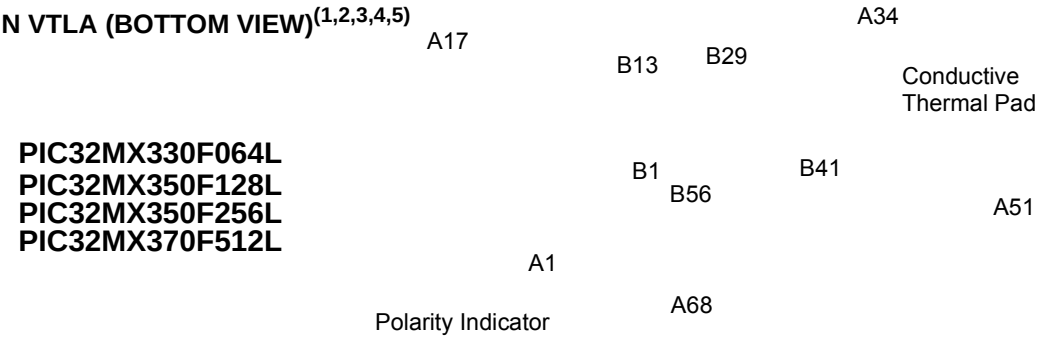
Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx), with the exception of RF6, can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: RPF6 (pin 55) and RPF7 (pin 54) are only remappable for input functions.

TABLE 6: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)(1,2,3,4,5)



Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
B7	$\overline{MCLR}$	B32	SDA2/RA3
B8	VSS	B33	TDO/RA5
B9	TMS/CTED1/RA0	B34	OSC1/CLKI/RC12
B10	RPE9/RE9	B35	No Connect
B11	AN4/C1INB/RB4	B36	RPA14/RA14
B12	VSS	B37	RPD8/RTCC/RD8
B13	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	B38	RPD10/PMCS2/RD10
B14	PGED1/AN0/RPB0/RB0	B39	RPD0/RD0
B15	No Connect	B40	SOSCO/RPC14/T1CK/RC14
B16	PGED2/AN7/RPB7/CTED3/RB7	B41	VSS
B17	VREF+/CVREF+/PMA6/RA10	B42	AN25/RPD2/RD2
B18	AVSS	B43	RPD12/PMD12/RD12
B19	AN9/RPB9/CTED4/RB9	B44	RPD4/PMWR/RD4
B20	AN11/PMA12/RB11	B45	PMD14/RD6
B21	VDD	B46	No Connect
B22	RPF13/RF13	B47	No Connect
B23	AN12/PMA11/RB12	B48	VCAP
B24	AN14/RPB14/CTED5/PMA1/RB14	B49	RPF0/PMD11/RF0
B25	VSS	B50	RPG1/PMD9/RG1
B26	RPD14/RD14	B51	TRCLK/RA6
B27	RPF4/PMA9/RF4	B52	PMD0/RE0
B28	No Connect	B53	VDD
B29	RPF8/RF8	B54	TRD2/RG14
B30	RPF6/SCKI/INT0/RF6	B55	TRD0/RG13
B31	SCL1/RG2	B56	RPE3/CTPLS/PMD3/RE3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx), with the exception of RF6, can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: RPF6 (bump B30) and RPF7 (bump A37) are only remappable for input functions.

4: Shaded package bumps are 5V tolerant.

5: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

NOTES:

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
Watchdog Timer	0xBF80	0x0000
RTCC		0x0200
Timer1-5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
I2C1 and I2C2		0x5000
SPI1 and SPI2		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC		0x9000
CVREF		0x9800
Comparator		0xA000
CTMU		0xA200
Oscillator		0xF000
Device and Revision ID		0xF200
Flash Controller		0xF400
Reset		0xF600
PPS		0xFA04
Interrupts	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
Prefetch		0x4000
USB		0x5040
PORTA-PORTG		0x6000
Configuration	0xBFC0	0x2FF0

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
			Flag	Enable	Priority	Sub-priority	
CNB – PORTB Input Change Interrupt	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>	Yes
CNC – PORTC Input Change Interrupt	46	33	IFS1<14>	IEC1<14>	IPC8<12:10>	IPC8<9:8>	Yes
CND – PORTD Input Change Interrupt	47	33	IFS1<15>	IEC1<15>	IPC8<12:10>	IPC8<9:8>	Yes
CNE – PORTE Input Change Interrupt	48	33	IFS1<16>	IEC1<16>	IPC8<12:10>	IPC8<9:8>	Yes
CNF – PORTF Input Change Interrupt	49	33	IFS1<17>	IEC1<17>	IPC8<12:10>	IPC8<9:8>	Yes
CNG – PORTG Input Change Interrupt	50	33	IFS1<18>	IEC1<18>	IPC8<12:10>	IPC8<9:8>	Yes
PMP – Parallel Master Port	51	34	IFS1<19>	IEC1<19>	IPC8<20:18>	IPC8<17:16>	Yes
PMPE – Parallel Master Port Error	52	34	IFS1<20>	IEC1<20>	IPC8<20:18>	IPC8<17:16>	Yes
SPI2E – SPI2 Fault	53	35	IFS1<21>	IEC1<21>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2RX – SPI2 Receive Done	54	35	IFS1<22>	IEC1<22>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2TX – SPI2 Transfer Done	55	35	IFS1<23>	IEC1<23>	IPC8<28:26>	IPC8<25:24>	Yes
U2E – UART2 Error	56	36	IFS1<24>	IEC1<24>	IPC9<4:2>	IPC9<1:0>	Yes
U2RX – UART2 Receiver	57	36	IFS1<25>	IEC1<25>	IPC9<4:2>	IPC9<1:0>	Yes
U2TX – UART2 Transmitter	58	36	IFS1<26>	IEC1<26>	IPC9<4:2>	IPC9<1:0>	Yes
I2C2B – I2C2 Bus Collision Event	59	37	IFS1<27>	IEC1<27>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2S – I2C2 Slave Event	60	37	IFS1<28>	IEC1<28>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2M – I2C2 Master Event	61	37	IFS1<29>	IEC1<29>	IPC9<12:10>	IPC9<9:8>	Yes
U3E – UART3 Error	62	38	IFS1<30>	IEC1<30>	IPC9<20:18>	IPC9<17:16>	Yes
U3RX – UART3 Receiver	63	38	IFS1<31>	IEC1<31>	IPC9<20:18>	IPC9<17:16>	Yes
U3TX – UART3 Transmitter	64	38	IFS2<0>	IEC2<0>	IPC9<20:18>	IPC9<17:16>	Yes
U4E – UART4 Error	65	39	IFS2<1>	IEC2<1>	IPC9<28:26>	IPC9<25:24>	Yes
U4RX – UART4 Receiver	66	39	IFS2<2>	IEC2<2>	IPC9<28:26>	IPC9<25:24>	Yes
U4TX – UART4 Transmitter	67	39	IFS2<3>	IEC2<3>	IPC9<28:26>	IPC9<25:24>	Yes
U5E – UART5 Error	68	40	IFS2<4>	IEC2<4>	IPC10<4:2>	IPC10<1:0>	Yes
U5RX – UART5 Receiver	69	40	IFS2<5>	IEC2<5>	IPC10<4:2>	IPC10<1:0>	Yes
U5TX – UART5 Transmitter	70	40	IFS2<6>	IEC2<6>	IPC10<4:2>	IPC10<1:0>	Yes
CTMU – CTMU Event	71	41	IFS2<7>	IEC2<7>	IPC10<12:10>	IPC10<9:8>	Yes
DMA0 – DMA Channel 0	72	42	IFS2<8>	IEC2<8>	IPC10<20:18>	IPC10<17:16>	No
DMA1 – DMA Channel 1	73	43	IFS2<9>	IEC2<9>	IPC10<28:26>	IPC10<25:24>	No
DMA2 – DMA Channel 2	74	44	IFS2<10>	IEC2<10>	IPC11<4:2>	IPC11<1:0>	No
DMA3 – DMA Channel 3	75	45	IFS2<11>	IEC2<11>	IPC11<12:10>	IPC11<9:8>	No
Lowest Natural Order Priority							

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX330/350/370/430/450/470 Controller Family Features"** for the list of available peripherals.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 18-16 **PLLMULT<2:0>:** Phase-Locked Loop (PLL) Multiplier bits
- 111 = Clock is multiplied by 24
- 110 = Clock is multiplied by 21
- 101 = Clock is multiplied by 20
- 100 = Clock is multiplied by 19
- 011 = Clock is multiplied by 18
- 010 = Clock is multiplied by 17
- 001 = Clock is multiplied by 16
- 000 = Clock is multiplied by 15

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits
- 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC (FRC) Oscillator divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (POSC) with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (POSC) (XT, HS or EC)
- 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast RC (FRC) Oscillator

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits
- 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC Oscillator (FRC) divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (XT, HS or EC)
- 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):
- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):
Clock and PLL selections are never locked and may be modified.

bit 6 **ULOCK:** USB PLL Lock Status bit(1)
- 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
- 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled

bit 5 **SLOCK:** PLL Lock Status bit
- 1 = PLL module is in lock or PLL module start-up timer is satisfied
- 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **SLPEN:** Sleep Mode Enable bit
- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

Note 1: This bit is available on PIC32MX4XX devices only.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FFF8
3200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3210	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3220	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 11-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = Change in ID state is detected
- 0 = No change in ID state is detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1millisecond, but different from last time
- 0 = USB line state has not been stable for 1 millisecond

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = Change on the session valid input is detected
- 0 = No change on the session valid input is detected

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDL	TWDIS	TWIP	—	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Timer is enabled
- 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
- 1 = Writes to TMR1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:
- 1 = Asynchronous write to TMR1 register in progress
- 0 = Asynchronous write to TMR1 register complete

In Synchronous Timer mode:
This bit is read as '0'.

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value

bit 3 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

bit 3 **T32:** 32-Bit Timer Mode Select bit(2)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(3)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is available only on even numbered timers (Timer2 and Timer4).

3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.

4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

30.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

30.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 31-15: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time.	—	—	10	µs	See **Note 1**
D313	DACREFH	CVREF Input Voltage Reference Range	AVSS	—	AVDD	V	CVRSRC with CVRSS = 0
			VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24		CVRCON<CVRR> = 1
			—	—	DACREFH/32		CVRCON<CVRR> = 0
D316	DACACC	Absolute Accuracy(2)	—	—	1/4	LSB	DACREFH/24, CVRCON<CVRR> = 1
			—	—	1/2	LSB	DACREFH/32, CVRCON<CVRR> = 0

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 31-16: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

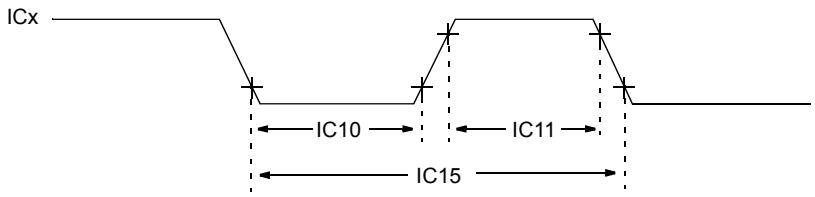
DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Comments**
D321	CEFC	External Filter Capacitor Value	8	10	—	µF	Capacitor must be low series resistance (3 ohm). Typical voltage on the VCAP pin is 1.8V.

TABLE 31-25: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**		**Min.**	**Max.**	**Units**	**Conditions**	
TB10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter TB15	
TB15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of [(25 ns or 2 TPB)/N] + 30 ns	—	ns	VDD > 2.7V	
				[(Greater of [(25 ns or 2 TPB)/N] + 50 ns	—	ns	VDD < 2.7V	
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPB	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 31-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



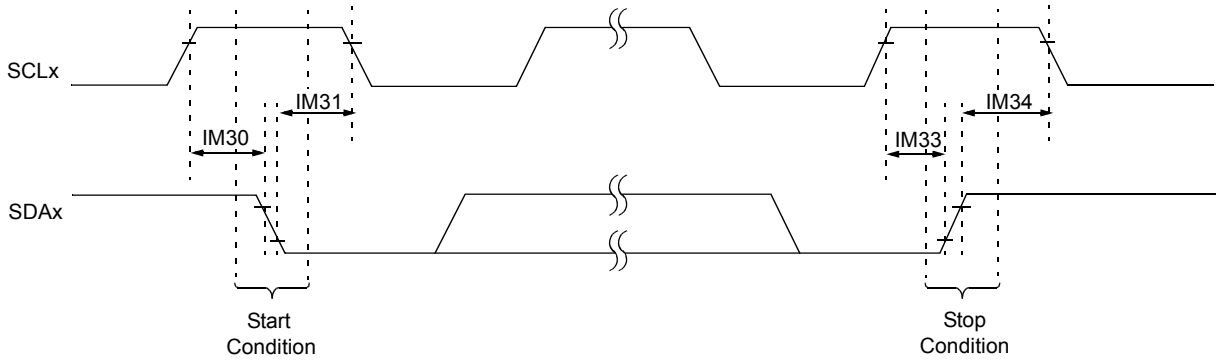
Note: Refer to Figure 31-1 for load conditions.

TABLE 31-26: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TCCL	ICx Input Low Time	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	TCCH	ICx Input High Time	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter IC15.	
IC15	TCCP	ICx Input Period	[(25 ns or 2 TPB)/N] + 50 ns	—	ns	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 31-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 31-1 for load conditions.

FIGURE 31-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

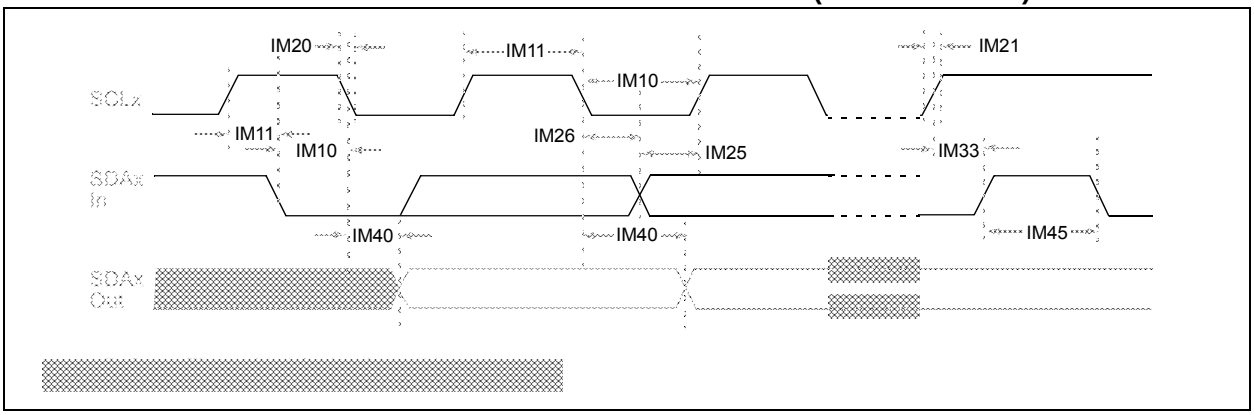
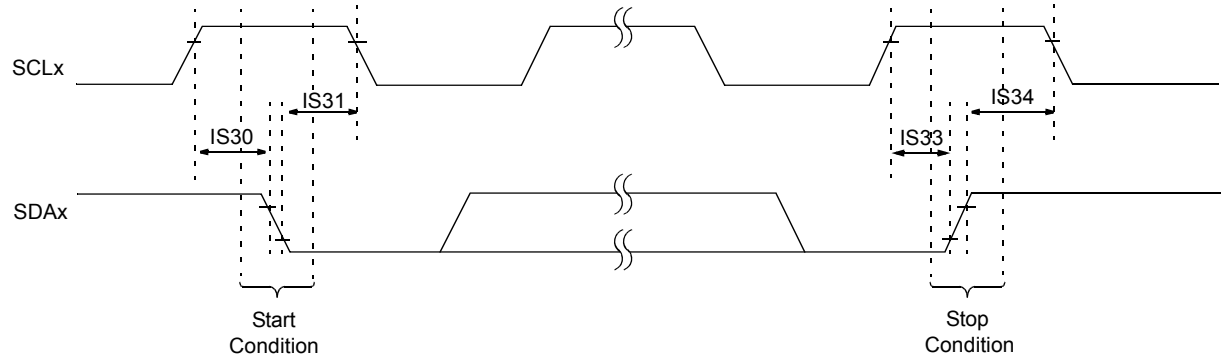


FIGURE 31-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 31-1 for load conditions.

FIGURE 31-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

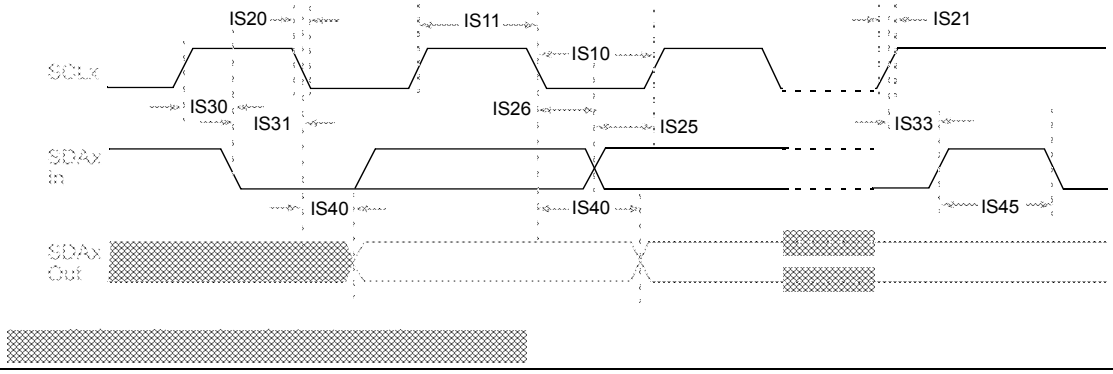


FIGURE 31-21: PARALLEL MASTER PORT READ TIMING DIAGRAM

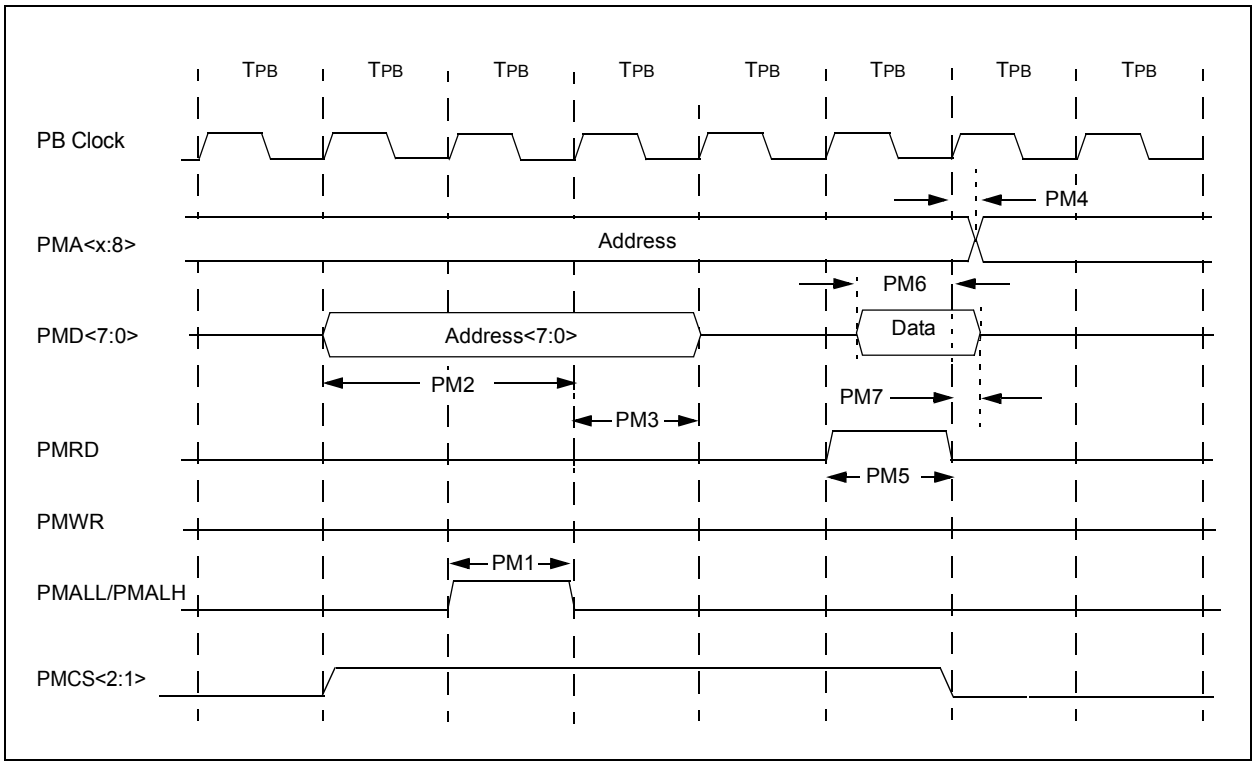


TABLE 31-39: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	—
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)	—	2 TPB	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	1 TPB	—	—	—	PMP Clock

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 31-41: OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	—
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 32-13: TYPICAL IDD CURRENT @ VDD = 3.3V

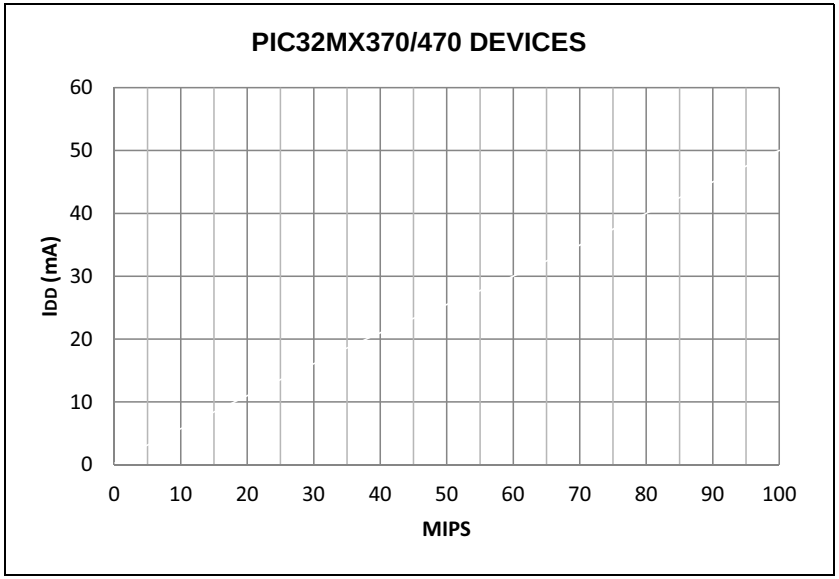


FIGURE 32-14: TYPICAL FRC FREQUENCY @ VDD = 3.3V

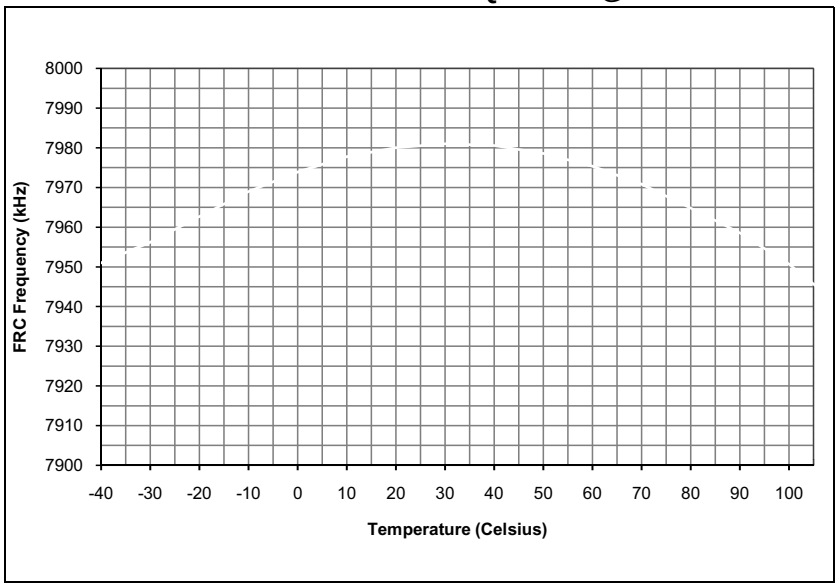


FIGURE 32-15: TYPICAL LPRC FREQUENCY @ VDD = 3.3V

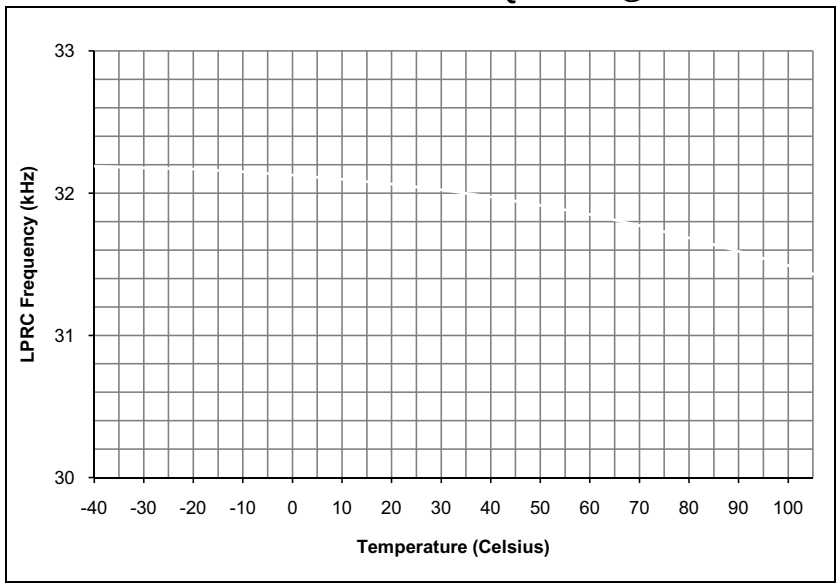
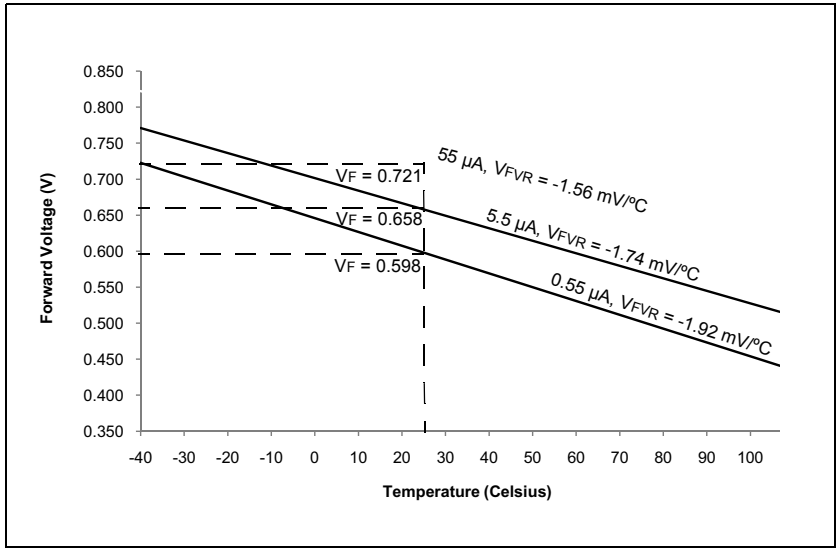


FIGURE 32-16: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE



Revision E (October 2015)

This revision includes the following updates, as listed in Table A-4.

TABLE A-4: MAJOR SECTION UPDATES

Section	Update Description
2.0 "Guidelines for Getting Started with 32-bit MCUs"	**Section 2.10 "Sosc Design Recommendations**" was removed.
31.0 "Electrical Characteristics"	The Power-Down Current (IPD) DC Characteristics were updated (see Table 31-7).

Revision F (September 2016)

This revision includes the following updates, as listed in Table A-5.

TABLE A-5: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Audio/ Graphics/Touch (HMI), USB, and Advanced Analog"	The PIC32MX450F128HB and PIC32MX470F512LB devices and Note 4 were added to the family features table (see Table 1). Note 2 in the 64-pin device pin table was updated (see Table 2). Note 2 in the 64-pin device pin table was updated and Note 4 was removed (see Table 3). Note 2 and Note 3 in the 100-pin device pin table was updated (see Table 4). Note 3 in the 124-pin device pin table was updated (see Table 6). Note 2 in the 124-pin device pin table was updated (see Table 7). RPF3 was removed from USB devices (see Table 3, Table 5, and Table 7).
1.0 "Device Overview"	The Pinout I/O Descriptions for pins $\overline{\text{U5CTS}}$, $\overline{\text{U5RTS}}$, U5RX, and U5TX in 64-pin QFN/TQFP packages were updated (see Table 1-1).
2.0 "Guidelines for Getting Started with 32-bit MCUs"	**2.10 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations"** was added.
8.0 "Oscillator Configuration"	The Clock Diagram was updated (see Figure 8-1). The Center Frequency values in the TUN<5:0> bits (OSCTUN<5:0>) were updated (see Register 8-2).
12.0 "I/O Ports"	Note references in the Input Pin Selection table were updated (see Table 12-1). Note references in the Output Pin Selection table were updated (see Table 12-2). PORTF Register Maps were updated (see Table 12-11 and Table 12-3). Note 1 was added to the Peripheral Pin Select Input Register Map (see Table 12-17).
31.0 "Electrical Characteristics"	The conditions for parameter DI60b (IICH) were updated (see Table 31-8). Parameter DO50a (CSOSC) was removed. The maximum value for parameter OS10 (FOSC) was updated (see Table 31-18). Parameter PM7 (TDHOLD) was updated (see Table 31-39). Note 1 was added to the DC Characteristics: Program Memory (see Table 31-12).
33.0 "Packaging Information"	The Land Pattern for 64-pin QFN packages was updated.
"Product Identification System"	The Software Targeting category was added.