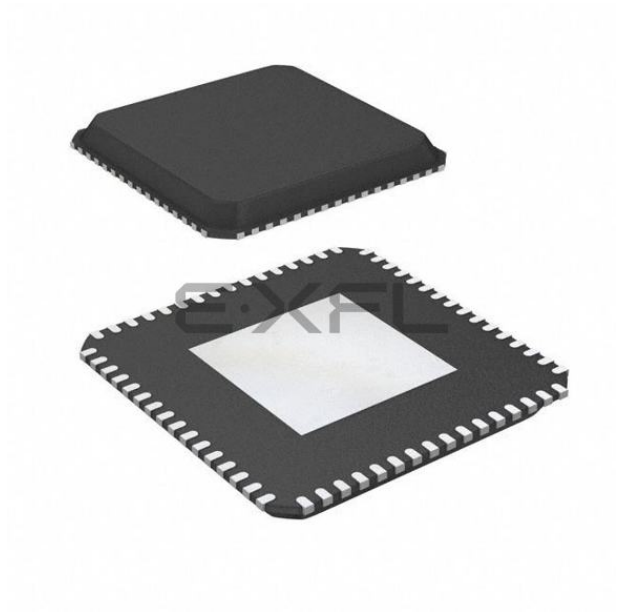
# Microchip Technology - PIC32MX450F128HT-V/RG Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 49 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 28x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx450f128ht-v-rg |

**TABLE 1: PIC32MX330/350/370/430/450/470 CONTROLLER FAMILY FEATURES**

| Device | Pins | Packages | Program Memory (KB)(1) | Data Memory (KB) | Remappable Peripherals | | | | | 10-bit 1 Msps ADC (Channels) | Analog Comparators | USB On-The-Go (OTG) | CTMU | $I^2C$ | PMP | RTCC | DMA Channels (Programmable/Dedicated) | I/O Pins | JTAG | Trace |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Remappable Pins | Timers/Capture/Compare(2) | UART | SPI/$I^2S$ | External Interrupts(3) | | | | | | | | | | | |
| PIC32MX330F064H | 64 | QFN, TQFP | 64+12 | 16 | 37 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | N | Y | 2 | Y | Y | 4/0 | 53 | Y | N |
| PIC32MX330F064L | 100 | TQFP | 64+12 | 16 | 54 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | N | Y | 2 | Y | Y | 4/0 | 85 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |
| PIC32MX350F128H | 64 | QFN, TQFP | 128+12 | 32 | 37 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | N | Y | 2 | Y | Y | 4/0 | 53 | Y | N |
| PIC32MX350F128L | 100 | TQFP | 128+12 | 32 | 54 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | N | Y | 2 | Y | Y | 4/0 | 85 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |
| PIC32MX350F256H | 64 | QFN, TQFP | 256+12 | 64 | 37 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | N | Y | 2 | Y | Y | 4/0 | 53 | Y | N |
| PIC32MX350F256L | 100 | TQFP | 256+12 | 64 | 54 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | N | Y | 2 | Y | Y | 4/0 | 85 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |
| PIC32MX370F512H | 64 | QFN, TQFP | 512+12 | 128 | 37 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | N | Y | 2 | Y | Y | 4/0 | 53 | Y | N |
| PIC32MX370F512L | 100 | TQFP | 512+12 | 128 | 54 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | N | Y | 2 | Y | Y | 4/0 | 85 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |
| PIC32MX430F064H | 64 | QFN, TQFP | 64+12 | 16 | 34 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 49 | Y | N |
| PIC32MX430F064L | 100 | TQFP | 64+12 | 16 | 51 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 81 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |
| PIC32MX450F128H | 64 | QFN, TQFP | 128+12 | 32 | 34 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 49 | Y | N |
| PIC32MX450F128HB (see **Note 4**) | 64 | QFN, TQFP | 128+12 | 32 | 34 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 49 | Y | N |
| PIC32MX450F128L | 100 | TQFP | 128+12 | 32 | 51 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 81 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |
| PIC32MX450F256H | 64 | QFN, TQFP | 256+12 | 64 | 34 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 49 | Y | N |
| PIC32MX450F256L | 100 | TQFP | 256+12 | 64 | 51 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 81 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |
| PIC32MX470F512H | 64 | QFN, TQFP | 512+12 | 128 | 34 | 5/5/5 | 4 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 49 | Y | N |
| PIC32MX470F512L | 100 | TQFP | 512+12 | 128 | 51 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 81 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |
| PIC32MX470F512LB (see **Note 4**) | 100 | TQFP | 512+12 | 128 | 51 | 5/5/5 | 5 | 2/2 | 5 | 28 | 2 | Y | Y | 2 | Y | Y | 4/2 | 81 | Y | Y |
| | 124 | VTLA | | | | | | | | | | | | | | | | | | |

**Note 1:** All devices feature 12 KB of Boot Flash memory.

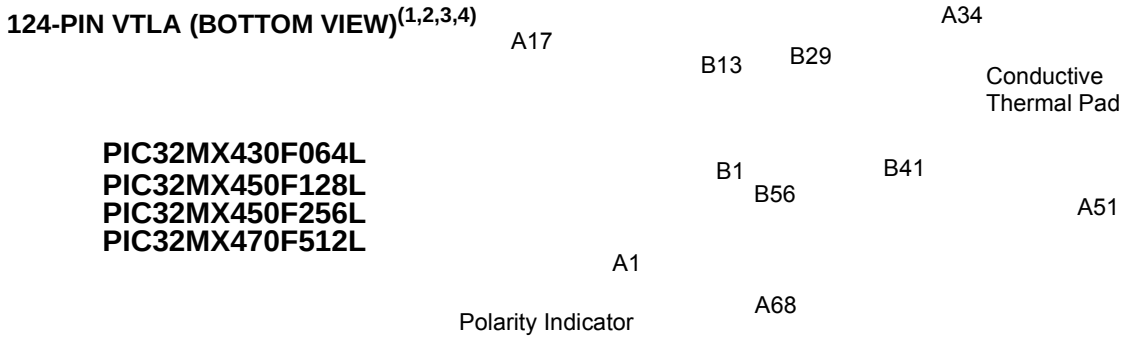
**2:** Four out of five timers are remappable.

**3:** Four out of five external interrupts are remappable.

**4:** This PIC32 device is targeted to specific audio software packages that are tracked for licensing royalty purposes. All peripherals and electrical characteristics are identical to their corresponding base part numbers

**TABLE 7: PIN NAMES FOR 124-PIN DEVICES**

**124-PIN VTLA (BOTTOM VIEW)(1,2,3,4)**




| Package Bump # | Full Pin Name | Package Bump # | Full Pin Name |
|---|---|---|---|
| A1 | No Connect | A38 | D- |
| A2 | RG15 | A39 | SCL2/RA2 |
| A3 | VSS | A40 | TDI/CTED9/RA4 |
| A4 | AN23/PMD6/RE6 | A41 | VDD |
| A5 | RPC1/RC1 | A42 | OSC2/CLKO/RC15 |
| A6 | RPC3/RC3 | A43 | VSS |
| A7 | AN16/C1IND/RPG6/SCK2/PMA5/RG6 | A44 | SDA1/RPA15/RA15 |
| A8 | AN18/C2IND/RPG8/PMA3/RG8 | A45 | RPD9/RD9 |
| A9 | AN19/C2INC/RPG9/PMA2/RG9 | A46 | RPD11/PMCS1/RD11 |
| A10 | VDD | A47 | SOSCI/RPC13/RC13 |
| A11 | RPE8/RE8 | A48 | VDD |
| A12 | AN5/C1INA/RPB5/VBUSON/RB5 | A49 | No Connect |
| A13 | PGED3/AN3/C2INA/RPB3/RB3 | A50 | No Connect |
| A14 | VDD | A51 | No Connect |
| A15 | PGEC1/AN1/RPB1/CTED12/RB1 | A52 | AN24/RPD1/RD1 |
| A16 | No Connect | A53 | AN26/RPD3/RD3 |
| A17 | No Connect | A54 | PMD13/RD13 |
| A18 | No Connect | A55 | RPD5/PMRD/RD5 |
| A19 | No Connect | A56 | PMD15/RD7 |
| A20 | PGEC2/AN6/RPB6/RB6 | A57 | No Connect |
| A21 | VREF-/CVREF-/PMA7/RA9 | A58 | No Connect |
| A22 | AVDD | A59 | VDD |
| A23 | AN8/RPB8/CTED10/RB8 | A60 | RPF1/PMD10/RF1 |
| A24 | CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10 | A61 | RPG0/PMD8/RG0 |
| A25 | VSS | A62 | TRD3/CTED8/RA7 |
| A26 | TCK/CTED2/RA1 | A63 | VSS |
| A27 | RPF12/RF12 | A64 | PMD1/RE1 |
| A28 | AN13/PMA10/RB13 | A65 | TRD1/RG12 |
| A29 | AN15/RPB15/OCFB/CTED6/PMA0/RB15 | A66 | AN20/PMD2/RE2 |
| A30 | VDD | A67 | AN21/PMD4/RE4 |
| A31 | RPD15/RD15 | A68 | No Connect |
| A32 | RPF5/PMA8/RF5 | B1 | VDD |
| A33 | No Connect | B2 | AN22/RPE5/PMD5/RE5 |
| A34 | No Connect | B3 | AN27/PMD7/RE7 |
| A35 | USBID/RF3 | B4 | RPC2/RC2 |
| A36 | RPF2/RF2 | B5 | RPC4/CTED7/RC4 |
| A37 | VBUS | B6 | AN17/C1INC/RPG7/PMA4/RG7 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

**3:** Shaded package bumps are 5V tolerant.

**4:** It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

**NOTES:**

### 2.8.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- COUT = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e.,12 mm length) = 2.5 pF

**EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION**

Crystal manufacturer recommended: $C1 = C2 = 15\ pF$

Therefore:

$$C_{LOAD} = \{( [C_{IN} + C1] * [C_{OUT} + C2] ) / [C_{IN} + C1 + C2 + C_{OUT}] \} + \text{estimated oscillator PCB stray capacitance}$$
$$= \{( [5 + 15][5 + 15] ) / [5 + 15 + 15 + 5] \} + 2.5\ pF$$
$$= \{( [20][20]) / [40] \} + 2.5$$
$$= 10 + 2.5 = 12.5\ pF$$

Rounded to the nearest standard value or 13 pF in this example for Primary Oscillator crystals “C1” and “C2”.

The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

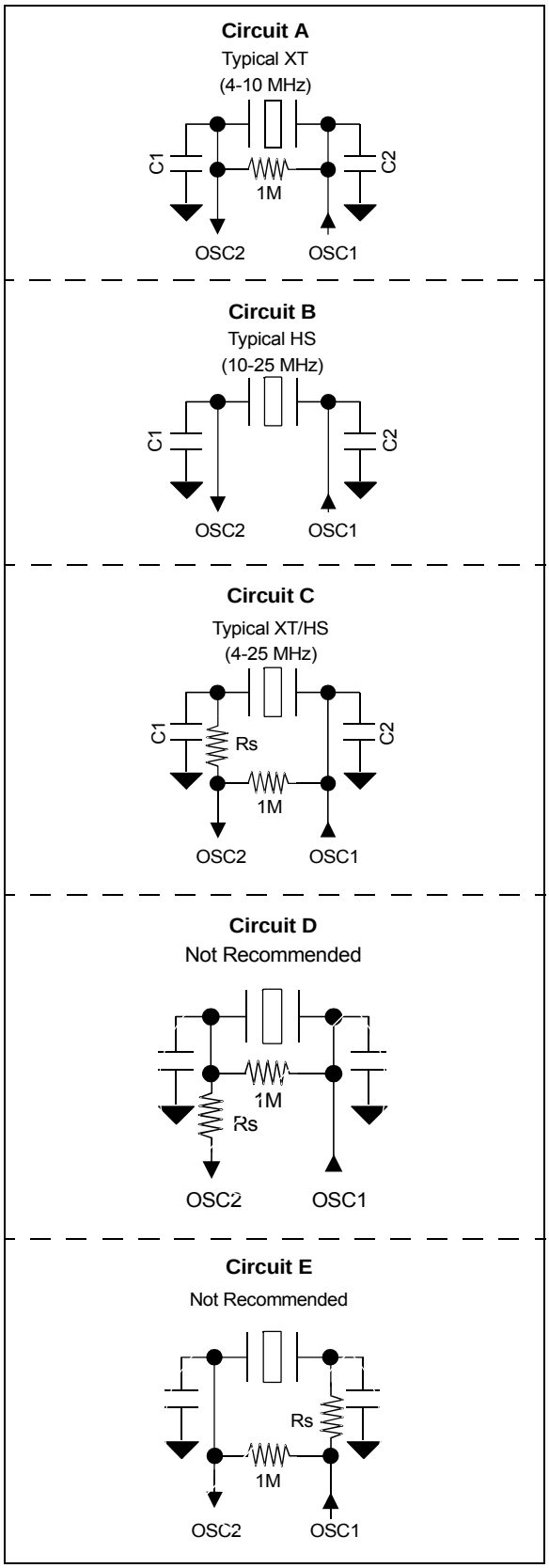
- Select a crystal with a lower “minimum” power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing “ESR” rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.

**Note:** Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, RS, as shown in circuit “C” in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to ~VDD-0.6V. When measuring the oscillator signal you must use a FET scope probe or a probe with ≤ 1.5 pF or the scope probe itself will unduly change the gain and peak-to-peak levels.

#### 2.8.1.1 Additional Microchip References

- AN588 *“PICmicro® Microcontroller Oscillator Design Guide”*
- AN826 *“Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices”*
- AN849 *“Basic PICmicro® Oscillator Design”*

**FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS**



**REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 | U-0 | U-0 | U-0 |
| | WR | WREN | WRERR(1) | LVDERR(1) | LVDSTAT(1) | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | NVMOP<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit
This bit is writable when WREN = 1 and the unlock sequence is followed.
1 = Initiate a Flash operation. Hardware clears this bit when the operation completes
0 = Flash operation complete or inactive

bit 14 **WREN:** Write Enable bit
1 = Enable writes to WR bit and enables LVD circuit
0 = Disable writes to WR bit and disables LVD circuit
This is the only bit in this register reset by a device Reset.

bit 13 **WRERR:** Write Error bit(1)
This bit is read-only and is automatically set by hardware.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit (LVD circuit must be enabled)(1)
This bit is read-only and is automatically set by hardware.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **LVDSTAT:** Low-Voltage Detect Status bit (LVD circuit must be enabled)(1)
This bit is read-only and is automatically set, and cleared, by hardware.
1 = Low-voltage event active
0 = Low-voltage event NOT active

bit 10-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits
These bits are writable when WREN = 0.
1111 = Reserved
•
•
•
0111 = Reserved
0110 = No operation
0101 = Program Flash (PFM) erase operation: erases PFM, if all pages are not write-protected
0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected
0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected
0010 = No operation
0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected
0000 = No operation

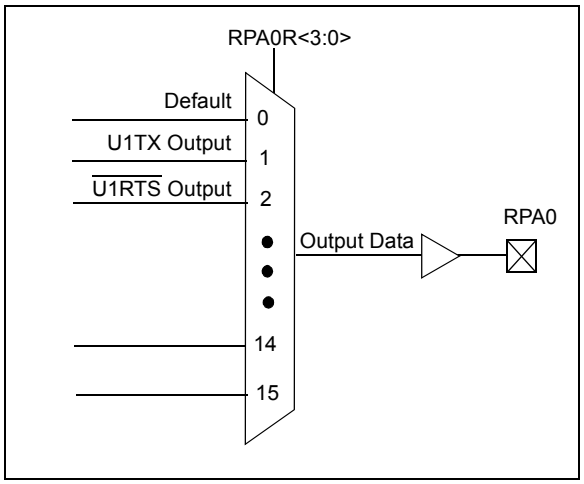
**Note 1:** This bit is cleared by setting NVMOP = 0000, and initiating a Flash operation (i.e., WR).

### 12.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 12-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 12-2 and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

**FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPA0**




### 12.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

#### 12.3.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

#### 12.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

**TABLE 12-2: OUTPUT PIN SELECTION**

| RPn Port Pin | RPnR SFR | RPnR bits | RPnR Value to Peripheral Selection |
|---|---|---|---|
| RPD2 | RPD2R | RPD2R<3:0> | 0000 = No Connect<br>0001 = U3TX<br>0010 = U4RTS<br>0011 = Reserved<br>0100 = Reserved<br>0101 = Reserved<br>0110 = SDO2<br>0111 = Reserved<br>1000 = Reserved<br>1001 = Reserved<br>1010 = Reserved<br>1011 = OC3<br>1100 = Reserved<br>1101 = C2OUT<br>1110 = Reserved<br>1111 = Reserved |
| RPG8 | RPG8R | RPG8R<3:0> | |
| RPF4 | RPF4R | RPF4R<3:0> | |
| RPD10 | RPD10R | RPD10R<3:0> | |
| RPF1 | RPF1R | RPF1R<3:0> | |
| RPB9 | RPB9R | RPB9R<3:0> | |
| RPB10 | RPB10R | RPB10R<3:0> | |
| RPC14 | RPC14R | RPC14R<3:0> | |
| RPB5 | RPB5R | RPB5R<3:0> | |
| RPC1(4) | RPC1R | RPC1R<3:0> | |
| RPD14(4) | RPD14R | RPD14R<3:0> | |
| RPG1(4) | RPG1R | RPG1R<3:0> | |
| RPA14(4) | RPA14R | RPA14R<3:0> | |
| RPD3 | RPD3R | RPD3R<3:0> | 0000 = No Connect<br>0001 = U2TX<br>0010 = Reserved<br>0011 = U1TX<br>0100 = U5RTS(4)<br>0101 = Reserved<br>0110 = SDO2<br>0111 = Reserved<br>1000 = SDO1<br>1001 = Reserved<br>1010 = Reserved<br>1011 = OC4<br>1100 = Reserved<br>1101 = Reserved<br>1110 = Reserved<br>1111 = Reserved |
| RPG7 | RPG7R | RPG7R<3:0> | |
| RPF5 | RPF5R | RPF5R<3:0> | |
| RPD11 | RPD11R | RPD11R<3:0> | |
| RPF0 | RPF0R | RPF0R<3:0> | |
| RPB1 | RPB1R | RPB1R<3:0> | |
| RPE5 | RPE5R | RPE5R<3:0> | |
| RPC13 | RPC13R | RPC13R<3:0> | |
| RPB3 | RPB3R | RPB3R<3:0> | |
| RPF3(2) | RPF3R | RPF3R<3:0> | |
| RPC4(4) | RPC4R | RPC4R<3:0> | |
| RPD15(4) | RPD15R | RPD15R<3:0> | |
| RPG0(4) | RPG0R | RPG0R<3:0> | |
| RPA15(4) | RPA15R | RPA15R<3:0> | |

**Note 1:** This selection is only available on General Purpose devices.

**2:** This selection is only available on 64-pin General Purpose devices.

**3:** This selection is only available on 100-pin General Purpose devices.

**4:** This selection is only available on 100-pin USB and General Purpose devices.

**5:** This selection is not available on 64-pin USB devices.

**TABLE 12-5: PORTC REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, PIC32MX370F512L, PIC32MX430F064L, PIC32MX450F128L, PIC32MX450F256L, AND PIC32MX470F512L DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6210 | TRISC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | TRISC4 | TRISC3 | TRISC2 | TRISC1 | — | xxxx |
| 6220 | PORTC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | RC4 | RC3 | RC2 | RC1 | — | xxxx |
| 6230 | LATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | LATC4 | LATC3 | LATC2 | LATC1 | — | xxxx |
| 6240 | ODCC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCC15 | ODCC14 | ODCC13 | ODCC12 | — | — | — | — | — | — | — | ODCC4 | ODCC3 | ODCC2 | ODCC1 | — | xxxx |
| 6250 | CNPUC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUC15 | CNPUC14 | CNPUC13 | CNPUC12 | — | — | — | — | — | — | — | CNPUC4 | CNPUC3 | CNPUC2 | CNPUC1 | — | xxxx |
| 6260 | CNPDC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDC15 | CNPDC14 | CNPDC13 | CNPDC12 | — | — | — | — | — | — | — | CNPDC4 | CNPDC3 | CNPDC2 | CNPDC1 | — | xxxx |
| 6270 | CNCONC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6280 | CNENC | 31:16 | — | — | | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIEC15 | CNIEC14 | CNIEC13 | CNIEC12 | — | — | — | — | — | — | — | CNIEC4 | CNIEC3 | CNIEC2 | CNIEC1 | — | xxxx |
| 6290 | CNSTATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNSTATC15 | CNSTATC14 | CNSTATC13 | CNSTATC12 | — | — | — | — | — | — | — | CNSTATC4 | CNSTATC3 | CNSTATC2 | CNSTATC1 | — | xxxx |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

## 16.1 Control Register

**REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | — | FEDGE | C32 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 |
| | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit |
| -n = Bit Value at POR: ('0', '1', x = unknown) | P = Programmable bit | r = Reserved bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit(1)
- 1 = Module is enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in CPU Idle mode
- 0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
- 0 = Timer3 is the counter source for capture
- 1 = Timer2 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow has occurred
- 0 = No input capture overflow has occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)**

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)
For Master mode 1 (MODE<1:0> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

**2:** These bits have no effect when their corresponding pins are used as address lines.

**NOTES:**

**REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EDG1MOD | EDG1POL | EDG1SEL<3:0> | | | | EDG2STAT | EDG1STAT |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | EDG2MOD | EDG2POL | EDG2SEL<3:0> | | | | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON | — | CTMUSIDL | TGEN(1) | EDGEN | EDGSEQEN | IDISSEN(2) | CTTRIG |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ITRIM<5:0> | | | | | | IRNG<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **EDG1MOD:** Edge 1 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 programmed for a positive edge response
0 = Edge 1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = Reserved
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = IC3 Capture Event is selected
1011 = IC2 Capture Event is selected
1010 = IC1 Capture Event is selected
1001 = CTED8 pin is selected
1000 = CTED7 pin is selected
0111 = CTED6 pin is selected
0110 = CTED5 pin is selected
0101 = CTED4 pin is selected
0100 = CTED3 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 25 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control edge source
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

**Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

**2:** The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**3:** Refer to the CTMU Current Source Specifications (Table 31-42) in **Section 31.0 "Electrical Characteristics"** for current values.

**4:** This bit setting is not available for the CTMU temperature diode.

**TABLE 31-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **Parameter No.** | **Typical(3)** | **Maximum** | **Units** | **Conditions** | |
| **Operating Current (IDD)(1,2)** | | | | | |
| DC20 | 2.5 | 4 | mA | 4 MHz | |
| DC21 | 6 | 9 | mA | 10 MHz **(Note 4)** | |
| DC22 | 11 | 17 | mA | 20 MHz **(Note 4)** | |
| DC23 | 21 | 32 | mA | 40 MHz **(Note 4)** | |
| DC24 | 30 | 45 | mA | 60 MHz **(Note 4)** | |
| DC25 | 40 | 60 | mA | 80 MHz | |
| DC25a | 50 | 75 | mA | 100 MHz, -40°C ≤ TA ≤ +85°C | |
| DC25c | 72 | 84 | mA | 120 MHz, 0°C ≤ TA ≤ +70°C | |
| DC26 | 100 | — | µA | +25ºC, 3.3V | LPRC (31 kHz) **(Note 4)** |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

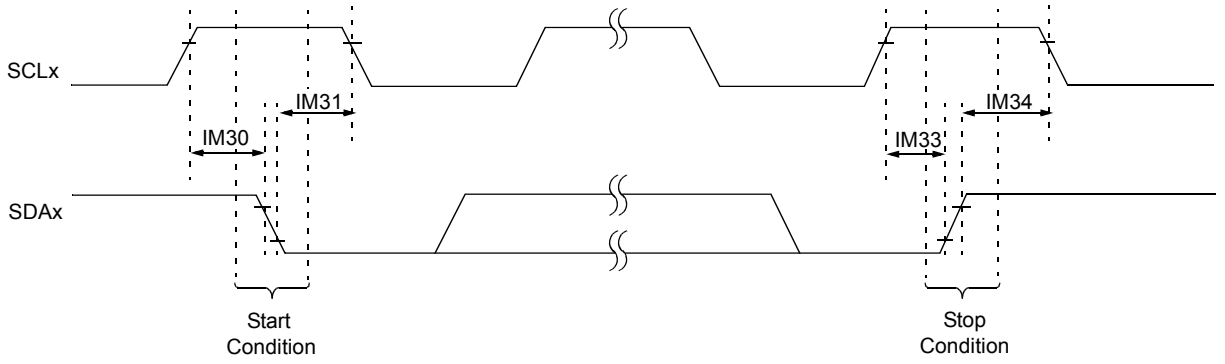
**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 7, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating (ON bit = 0), but the associated PMD bit is clear
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 31-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 31-1 for load conditions.

**FIGURE 31-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**

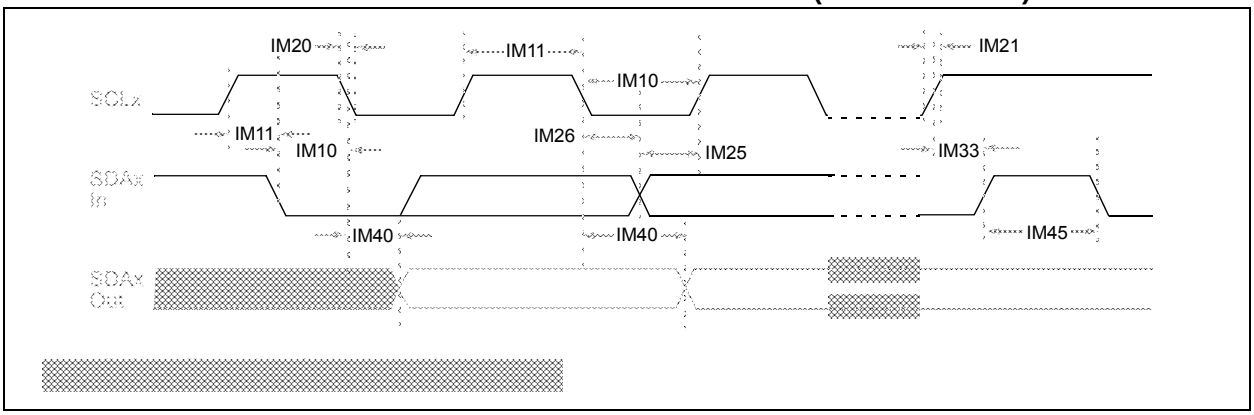


**TABLE 31-34: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode **(Note 1)** | 250 | | ns | |
| IS40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | 0 | 3500 | ns | — |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode **(Note 1)** | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | The amount of time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode **(Note 1)** | 0.5 | — | µs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | — |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**NOTES:**

## 32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 32-1: VOH – 4x DRIVER PINS**

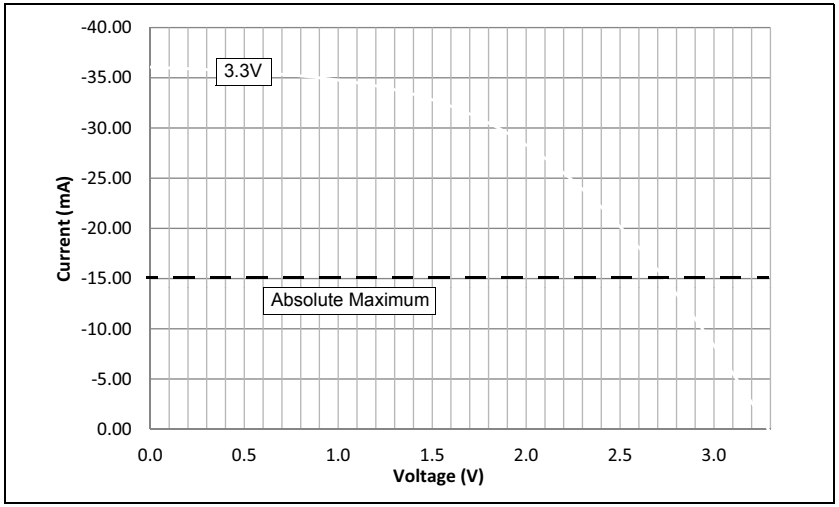



**FIGURE 32-2: VOH – 8x DRIVER PINS**

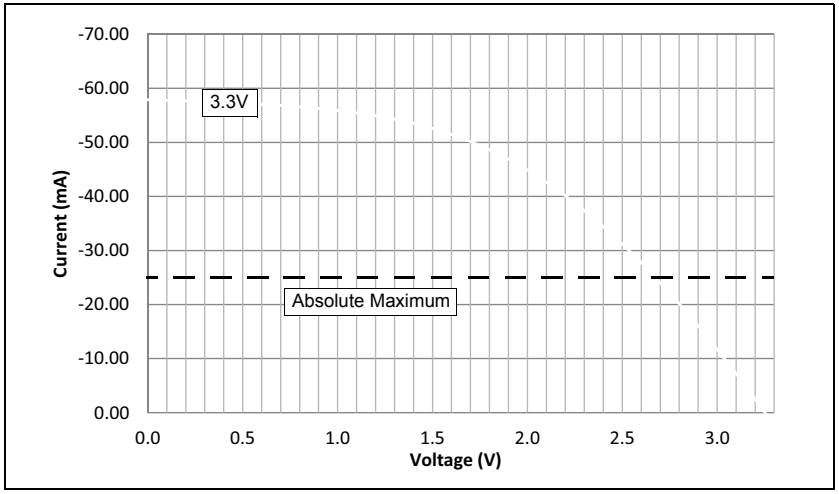



**FIGURE 32-3: VOL – 4x DRIVER PINS**

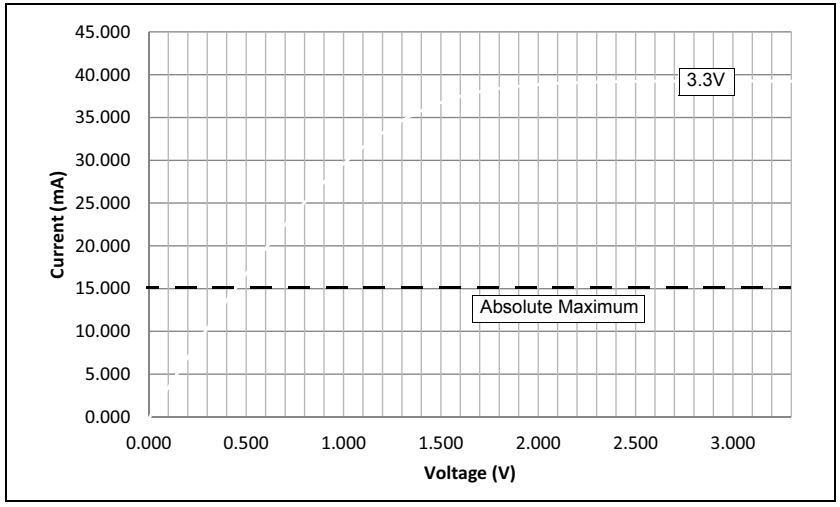
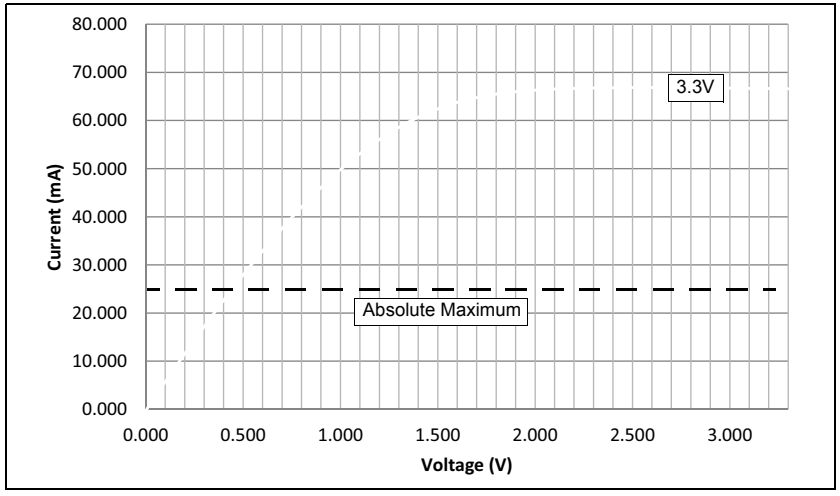
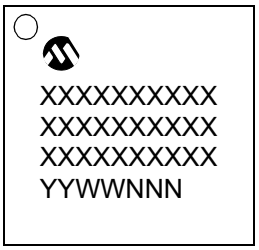



**FIGURE 32-4: VOL – 8x DRIVER PINS**

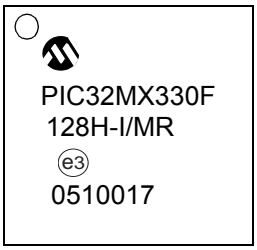


### 33.1 Package Marking Information (Continued)

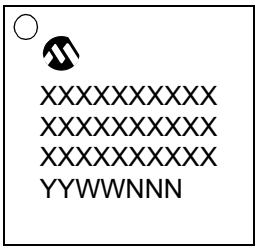
64-Lead QFN (9x9x0.9 mm) with 5.40x5.40 Exposed Pad



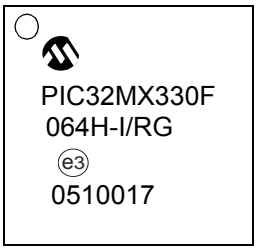

Example



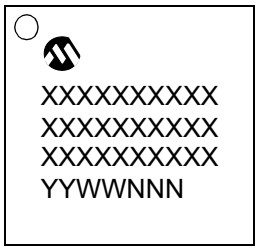

64-Lead QFN (9x9x0.9 mm) with 4.7x4.7 Exposed Pad



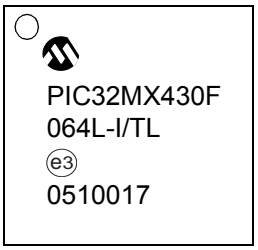

Example




124-Lead VTLA (9x9x0.9 mm)




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## Revision C (October 2013)

This revision includes the following updates, as listed in Table A-2.

**TABLE A-2: MAJOR SECTION UPDATES**

| Section | Update Description |
|---|---|
| **"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Audio/Graphics/Touch (HMI), USB, and Advanced Analog"** | The Operating Conditions and Core sections were updated in support of 100 MHz (-40ºC to +85ºC) devices.<br>Added Notes 2 and 3 regarding the conductive thermal pad to the 124-pin VTLA pin diagrams. |
| **2.0 "Guidelines for Getting Started with 32-bit MCUs"** | Updated the recommended minimum connection (see Figure 2-1).<br>Added **2.10 "Sosc Design Recommendation"**. |
| **20.0 "Parallel Master Port (PMP)"** | Updated the Parallel Port Control register, PMCON (see Register 20-1).<br>Updated the Parallel Port Mode register, PMMODE (see Register 20-2).<br>Updated the Parallel Port Pin Enable register, PMAEN (see Register 20-4). |
| **30.0 "Electrical Characteristics"** | Removed Note 4 from the Absolute Maximum Ratings.<br>The maximum frequency for parameter DC5 In Operating MIPS vs. Voltage was changed to 100 MHz (see Table 30-1).<br>Parameter DC25a was added to DC Characteristics: Operating Current (IDD) (see Table 30-5).<br>Parameter DC34c was added to DC Characteristics: Idle Current (IIDLE) (see Table 30-5).<br>Added parameters for PIC32MX370/470 devices and removed Note 5 from DC Characteristics: Power-Down Current (IPD) (see Table 30-7).<br>Updated the Minimum, Typical, and Maximum values and added a reference to Note 3 for parameter DI30 (ICNPU) in DC Characteristics: I/O Pin Input Specifications (see Table 30-8).<br>The SYSCLK values for all required Flash Wait states were updated (see Table 30-13).<br>Added parameter DO50A (CSOSC) to the Capacitive Loading Requirements on Output Pins (see Table 30-16).<br>Updated the maximum values for parameter OS10, and the Characteristics definition of parameter OS42 (GM) in the External Clock Timing Characteristics (see Table 30-17). |
| **31.0 "DC and AC Device Characteristics Graphs"** | Updated the IPD, IIDLE, and IDD graphs, and added new graphs for the PIC32MX370/470 devices (see Figure 31-5 through Figure 31-13). |

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