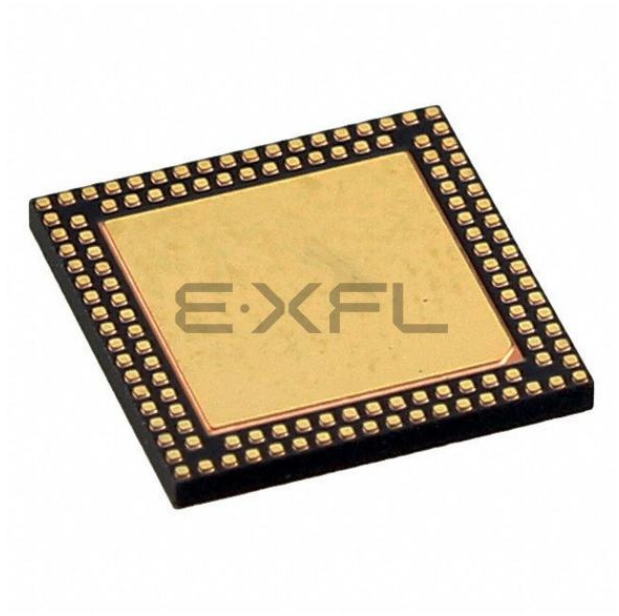

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 28x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 124-VFTLA Dual Rows, Exposed Pad |
| Supplier Device Package | 124-VTLA (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx450f128l-v-tl |

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | 124-pin VTLA | | | |
| U1CTS | PPS | PPS | PPS | I | ST | UART1 Clear to Send |
| U1RTS | PPS | PPS | PPS | O | — | UART1 Ready to Send |
| U1RX | PPS | PPS | PPS | I | ST | UART1 Receive |
| U1TX | PPS | PPS | PPS | O | — | UART1 Transmit |
| U2CTS | PPS | PPS | PPS | I | ST | UART2 Clear to Send |
| U2RTS | PPS | PPS | PPS | O | — | UART2 Ready to Send |
| U2RX | PPS | PPS | PPS | I | ST | UART2 Receive |
| U2TX | PPS | PPS | PPS | O | — | UART2 Transmit |
| U3CTS | PPS | PPS | PPS | I | ST | UART3 Clear to Send |
| U3RTS | PPS | PPS | PPS | O | — | UART3 Ready to Send |
| U3RX | PPS | PPS | PPS | I | ST | UART3 Receive |
| U3TX | PPS | PPS | PPS | O | — | UART3 Transmit |
| U4CTS | PPS | PPS | PPS | I | ST | UART4 Clear to Send |
| U4RTS | PPS | PPS | PPS | O | — | UART4 Ready to Send |
| U4RX | PPS | PPS | PPS | I | ST | UART4 Receive |
| U4TX | PPS | PPS | PPS | O | — | UART4 Transmit |
| U5CTS(3) | — | PPS | PPS | I | ST | UART5 Clear to Send |
| U5RTS(3) | — | PPS | PPS | O | — | UART5 Ready to Send |
| U5RX(3) | — | PPS | PPS | I | ST | UART5 Receive |
| U5TX(3) | — | PPS | PPS | O | — | UART5 Transmit |
| SCK1 | 35(1), 50(2) | 55(1), 70(2) | B30(1), B38(2) | I/O | ST | Synchronous Serial Clock Input/Output for SPI1 |
| SDI1 | PPS | PPS | PPS | O | — | SPI1 Data In |
| SDO1 | PPS | PPS | PPS | I/O | ST | SPI1 Data Out |
| SS1 | PPS | PPS | PPS | I/O | — | SPI1 Slave Synchronization for Frame Pulse I/O |
| SCK2 | 4 | 10 | A7 | I/O | ST | Synchronous Serial Clock Input/Output for SPI2 |
| SDI2 | PPS | PPS | PPS | O | — | SPI2 Data In |
| SDO2 | PPS | PPS | PPS | I/O | ST | SPI2 Data Out |
| SS2 | PPS | PPS | PPS | I/O | — | SPI2 Slave Synchronization for Frame Pulse I/O |
| SCL1 | 37(1), 44(2) | 57(1), 66(2) | B31(1), B36(2) | I/O | ST | Synchronous Serial Clock Input/Output for I2C1 |
| SDA1 | 36(1), 43(2) | 56(1), 67(2) | A38(1), A44(2) | I/O | ST | Synchronous Serial Data Input/Output for I2C1 |
| SCL2 | 32 | 58 | A39 | I/O | ST | Synchronous Serial Clock Input/Output for I2C2 |
| SDA2 | 31 | 59 | B32 | I/O | ST | Synchronous Serial Data Input/Output for I2C2 |
| TMS | 23 | 17 | B9 | I | ST | JTAG Test Mode Select Pin |
| TCK | 27 | 38 | A26 | I | ST | JTAG Test Clock Input Pin |
| TDI | 28 | 60 | A40 | I | — | JTAG Test Clock Input Pin |
| TDO | 24 | 61 | B33 | O | — | JTAG Test Clock Output Pin |
| RTCC | 42 | 68 | B37 | O | — | Real-Time Clock Alarm Output |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

**Note 1:** This pin is only available on devices without a USB module.
**2:** This pin is only available on devices with a USB module.
**3:** This pin is not available on 64-pin devices.

## 5.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Program Memory"** (DS60001121), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX330/350/370/430/450/470 devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "*PIC32 Flash Programming Specification*" (DS60001145), which can be downloaded from the Microchip web site.

**Note:** On PIC32MX330/350/370/430/450/470 devices, the Flash page size is 4 KB and the row size is 512 bytes (1024 IW and 128 IW, respectively).

**REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | — | — | — | — | — | — | — | SS0 |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MVEC | — | TPC<2:0> | | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-17 **Unimplemented:** Read as '0'

bit 16 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow register set
0 = Single vector is not presented with a shadow register set

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multi Vector Configuration bit
1 = Interrupt controller configured for multi vectored mode
0 = Interrupt controller configured for single vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
001 = Interrupts of group priority 1 start the Interrupt Proximity timer
000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP3<2:0> | | | IS3<1:0> | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP2<2:0> | | | IS2<1:0> | |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP1<2:0> | | | IS1<1:0> | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP0<2:0> | | | IS0<1:0> | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP1<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

**REGISTER 11-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 |
| | IDIE | T1MSECIE | LSTATEIE | ACTVIE | SESVDIE | SESENDIE | — | VBUSVDIE |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = ID interrupt is enabled
0 = ID interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = 1 millisecond timer interrupt is enabled
0 = 1 millisecond timer interrupt is disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit
1 = Line state interrupt is enabled
0 = Line state interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = ACTIVITY interrupt is enabled
0 = ACTIVITY interrupt is disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Session valid interrupt is enabled
0 = Session valid interrupt is disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit
1 = B-session end interrupt is enabled
0 = B-session end interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit
1 = A-VBUS valid interrupt is enabled
0 = A-VBUS valid interrupt is disabled

**TABLE 12-7: PORTD REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, PIC32MX370F512L, PIC32MX430F064L, PIC32MX450F128L, PIC32MX450F256L, AND PIC32MX470F512L DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6300 | ANSELD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | ANSELD3 | ANSELD2 | ANSELD1 | — | 000E |
| 6310 | TRISD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISD15 | TRISD14 | TRISD13 | TRISD12 | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | xxxx |
| 5320 | PORTD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| 6330 | LATD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATD15 | LATD14 | LATD13 | LATD12 | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| 6340 | ODCD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCD15 | ODCD14 | ODCD13 | ODCD12 | ODCD11 | ODCD10 | ODCD9 | ODCD8 | ODCD7 | ODCD6 | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | xxxx |
| 6350 | CNPUD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPUD15 | CNPUD14 | CNPUD13 | CNPUD12 | CNPUD11 | CNPUD10 | CNPUD9 | CNPUD8 | CNPUD7 | CNPUD6 | CNPUD5 | CNPUD4 | CNPUD3 | CNPUD2 | CNPUD1 | CNPUD0 | xxxx |
| 6360 | CNPDD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNPDD15 | CNPDD14 | CNPDD13 | CNPDD12 | CNPDD11 | CNPDD10 | CNPDD9 | CNPDD8 | CNPDD7 | CNPDD6 | CNPDD5 | CNPDD4 | CNPDD3 | CNPDD2 | CNPDD1 | CNPDD0 | xxxx |
| 6370 | CNCOND | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6380 | CNEND | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNIED15 | CNIED14 | CNIED13 | CNIED12 | CNIED11 | CNIED10 | CNIED9 | CNIED8 | CNIED7 | CNIED6 | CNIED5 | CNIED4 | CNIED3 | CNIED2 | CNIED1 | CNIED0 | xxxx |
| 6390 | CNSTATD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CNS TATD15 | CN STATD14 | CN STATD13 | CN STATD12 | CN STATD11 | CN STATD10 | CN STATD9 | CN STATD8 | CN STATD7 | CN STATD6 | CN STATD5 | CN STATD4 | CN STATD3 | CN STATD2 | CN STATD1 | CN STATD0 | xxxx |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

**TABLE 12-16: PORTG REGISTER MAP FOR PIC32MX330F064H, PIC32MX350F128H, PIC32MX350F256H, PIC32MX370F512H, PIC32MX430F064H, PIC32MX450F128H, PIC32MX450F256H, AND PIC32MX470F512H DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6600 | ANSELG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ANSELG9 | ANSELG8 | ANSELG7 | ANSELG6 | — | — | — | — | — | — | 01C0 |
| 6610 | TRISG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | TRISG3 | TRISG2 | — | — | xxxx |
| 6620 | PORTG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3(2) | RG2(2) | — | — | xxxx |
| 6630 | LATG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | LATG3 | LATG2 | — | — | xxxx |
| 6640 | ODCG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ODCG9 | ODCG8 | ODCG7 | ODCG6 | — | — | ODCG3 | ODCG2 | — | — | xxxx |
| 6650 | CNPUG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | — | — | CNPUG3 | CNPUG2 | — | — | xxxx |
| 6660 | CNPDG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | — | — | CNPDG3 | CNPDG2 | — | — | xxxx |
| 6670 | CNCONG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6680 | CNENG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | — | — | CNIEG3 | CNIEG2 | — | — | xxxx |
| 6690 | CNSTATG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CN STATG9 | CN STATG8 | CN STATG7 | CN STATG6 | — | — | CN STATG3 | CN STATG2 | — | — | xxxx |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

**2:** This bit is only available on devices without a USB module.

## 14.2 Control Register

**TABLE 14-1: TIMER2 THROUGH TIMER5 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0800 | T2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | T32 | — | TCS | — | 0000 |
| 0810 | TMR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR2<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0820 | PR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR2<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0A00 | T3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | — | — | TCS | — | 0000 |
| 0A10 | TMR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR3<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0A20 | PR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR3<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0C00 | T4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | T32 | — | TCS | — | 0000 |
| 0C10 | TMR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR4<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0C20 | PR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR4<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0E00 | T5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | — | — | TCS | — | 0000 |
| 0E10 | TMR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR5<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0E20 | PR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR5<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

**REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)**

bit 3 **T32:** 32-Bit Timer Mode Select bit(2)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(3)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is available only on even numbered timers (Timer2 and Timer4).

**3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.

**4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | IREN | RTSMD | — | UEN<1:0> | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit(1)
- 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
- 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation in Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
- 1 = Wake-up is enabled
- 0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)**

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(3)

11111111 = Alarm will trigger 256 times

•

•

•

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

**Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

**2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

**3:** This assumes a CPU read will execute in less than 32 PBCLKs.

| **Note:** | This register is reset only on a Power-on Reset (POR). |
|---|---|

## 23.1 Control Registers

**TABLE 23-1: ADC REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9000 | AD1CON1(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | FORM<2:0> | | | SSRC<2:0> | | | CLRASAM | — | ASAM | SAMP | DONE | 0000 |
| 9010 | AD1CON2(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | VCFG<2:0> | | | OFFCAL | — | CSCNA | — | — | BUFS | — | SMPI<3:0> | | | | BUFM | ALTS | 0000 |
| 9020 | AD1CON3(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ADRC | — | — | SAMC<4:0> | | | | | ADCS<7:0> | | | | | | | | 0000 |
| 9040 | AD1CHS(1) | 31:16 | CH0NB | — | — | CH0SB<4:0> | | | | | CH0NA | — | — | CH0SA<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 9050 | AD1CSSL(1) | 31:16 | — | CSSL30 | CSSL29 | CSSL28 | CSSL27 | CSSL26 | CSSL25 | CSSL24 | CSSL23 | CSSL22 | CSSL21 | CSSL20 | CSSL19 | CSSL18 | CSSL17 | CSSL16 | 0000 |
| | | 15:0 | CSSL15 | CSSL14 | CSSL13 | CSSL12 | CSSL11 | CSSL10 | CSSL9 | CSSL8 | CSSL7 | CSSL6 | CSSL5 | CSSL4 | CSSL3 | CSSL2 | CSSL1 | CSSL0 | 0000 |
| 9070 | ADC1BUF0 | 31:16 | ADC Result Word 0 (ADC1BUF0<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9080 | ADC1BUF1 | 31:16 | ADC Result Word 1 (ADC1BUF1<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9090 | ADC1BUF2 | 31:16 | ADC Result Word 2 (ADC1BUF2<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90A0 | ADC1BUF3 | 31:16 | ADC Result Word 3 (ADC1BUF3<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90B0 | ADC1BUF4 | 31:16 | ADC Result Word 4 (ADC1BUF4<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90C0 | ADC1BUF5 | 31:16 | ADC Result Word 5 (ADC1BUF5<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90D0 | ADC1BUF6 | 31:16 | ADC Result Word 6 (ADC1BUF6<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90E0 | ADC1BUF7 | 31:16 | ADC Result Word 7 (ADC1BUF7<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90F0 | ADC1BUF8 | 31:16 | ADC Result Word 8 (ADC1BUF8<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9100 | ADC1BUF9 | 31:16 | ADC Result Word 9 (ADC1BUF9<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for details.

**REGISTER 24-1: CMxCON: COMPARATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R-0 |
| | ON(1) | COE | CPOL(2) | — | — | — | — | COUT |
| 7:0 | R/W-1 | R/W-1 | U-0 | R/W-0 | U-0 | U-0 | R/W-1 | R/W-1 |
| | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit(1)
- 1 = Module is enabled. Setting this bit does not affect the other bits in this register
- 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is driven on the output CxOUT pin
- 0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit(2)
- 1 = Output is inverted
- 0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
- 1 = Output of the Comparator is a '1'
- 0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
- 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
- 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
- 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
- 00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit
- 1 = Comparator non-inverting input is connected to the internal $CV_{REF}$
- 0 = Comparator non-inverting input is connected to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
- 11 = Comparator inverting input is connected to the $IV_{REF}$
- 10 = Comparator inverting input is connected to the CxIND pin
- 01 = Comparator inverting input is connected to the CxINC pin
- 00 = Comparator inverting input is connected to the CxINB pin

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

### 27.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

**Note 1:** Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a POSC of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.

**2:** Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from POSC to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to POSC, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

### 27.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The peripheral bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

**REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)**

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

111 = 12x divider
110 = 10x divider
101 = 6x divider
100 = 5x divider
011 = 4x divider
010 = 3x divider
001 = 2x divider
000 = 1x divider

**Note 1:** This bit is available on PIC32MX4XX devices only.

## 29.0 INSTRUCTION SET

The PIC32MX330/350/370/430/450/470 family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

**Note:** Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

**TABLE 31-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(2)** | **Maximum** | **Units** | **Conditions** | | |
| **Idle Current (IIDLE): Core Off, Clock on Base Current (Note 1)** | | | | | | |
| DC30a | 1 | 2.2 | mA | 4 MHz | | |
| DC31a | 3 | 5 | mA | 10 MHz **(Note 3)** | | |
| DC32a | 5 | 7 | mA | 20 MHz **(Note 3)** | | |
| DC33a | 8 | 13 | mA | 40 MHz **(Note 3)** | | |
| DC34a | 11 | 18 | mA | 60 MHz **(Note 3)** | | |
| DC34b | 15 | 24 | mA | 80 MHz | | |
| DC34c | 19 | 29 | mA | 100 MHz, -40°C ≤ TA ≤ +85°C | | |
| DC34d | 25 | 34 | mA | 120 MHz, 0°C ≤ TA ≤ +70°C | | |
| DC37a | 100 | — | µA | -40°C | 3.3V | LPRC (31 kHz) **(Note 3)** |
| DC37b | 250 | — | µA | +25°C | | |
| DC37c | 380 | — | µA | +85°C | | |

**Note 1:** The test conditions for IIDLE measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core is halted), program Flash memory Wait states = 7, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 31-5: EXTERNAL RESET TIMING CHARACTERISTICS**

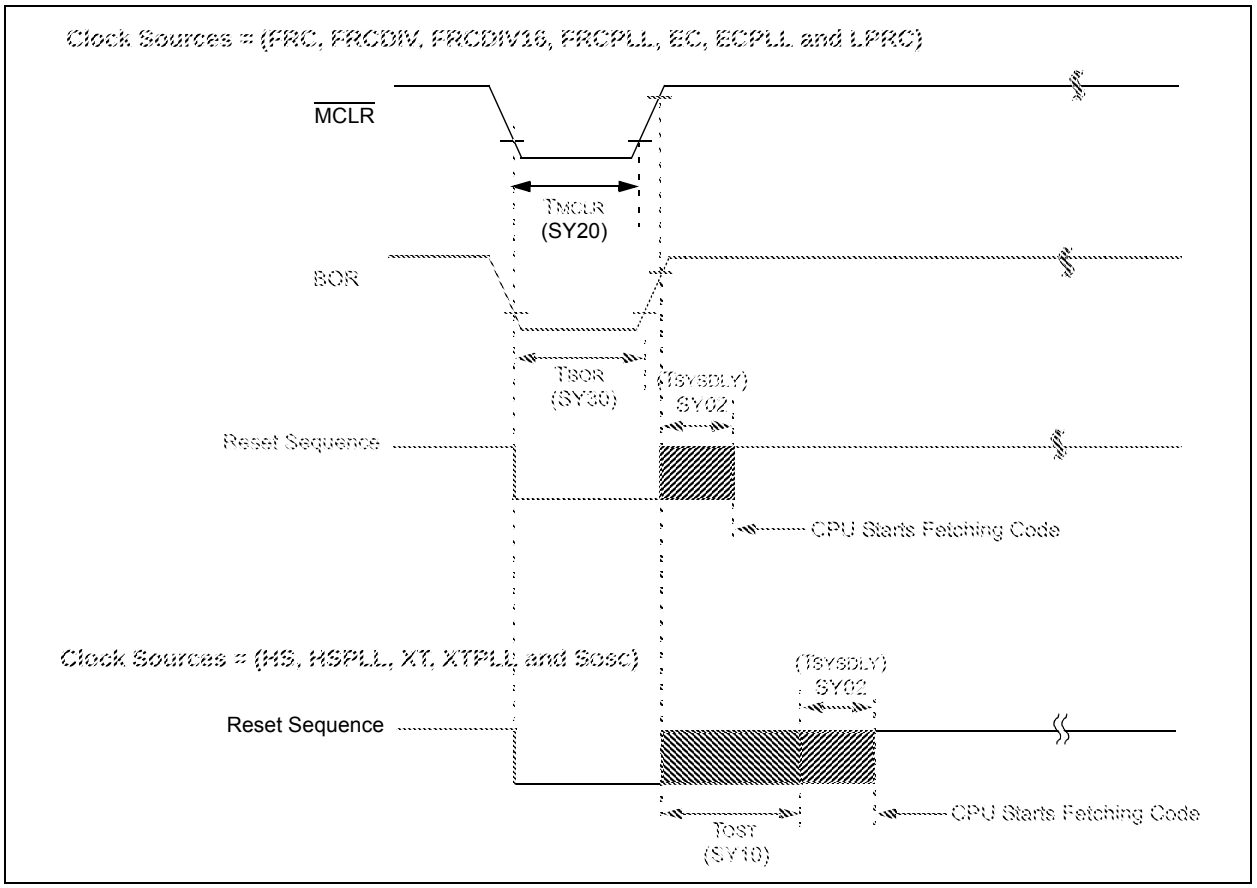


**TABLE 31-23: RESETS TIMING**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SY00 | TPU | Power-up Period<br>Internal Voltage Regulator Enabled | — | 400 | 600 | μs | — |
| SY02 | TSYSDLY | System Delay Period:<br>Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched. | — | 1 μs + 8 SYSCLK cycles | — | — | — |
| SY20 | TMCLR | $\overline{\text{MCLR}}$ Pulse Width (low) | 2 | — | — | μs | — |
| SY30 | TBOR | BOR Pulse Width (low) | — | 1 | — | μs | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

**NOTES:**

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