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Details

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Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx450f256ht-v-mr

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FIGURE 2-8: LOW-COST CONTROLLERLESS (LCC) GRAPHICS APPLICATION WITH PROJECTED CAPACITIVE TOUCH



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	-	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R-0	R-0	R-0	U-0	U-0	U-0
15:8	WR	WREN	WRERR ⁽¹⁾	LVDERR ⁽¹⁾	LVDSTAT ⁽¹⁾	—	—	—
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	-	—	—	NVMOP<3:0>			

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	nd as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15	WR: Write Control bit
	This bit is writable when WREN = 1 and the unlock sequence is followed.
	1 = Initiate a Flash operation. Hardware clears this bit when the operation completes
	0 = Flash operation complete or inactive
bit 14	WREN: Write Enable bit
	1 = Enable writes to WR bit and enables LVD circuit
	0 = Disable writes to WR bit and disables LVD circuit
	This is the only bit in this register reset by a device Reset.
bit 13	WRERR: Write Error bit ⁽¹⁾
	This bit is read-only and is automatically set by hardware.
	 Program or erase sequence did not complete successfully
	0 = Program or erase sequence completed normally
bit 12	LVDERR: Low-Voltage Detect Error bit (LVD circuit must be enabled) ⁽¹⁾
	This bit is read-only and is automatically set by hardware.
	1 = Low-voltage detected (possible data corruption, if WRERR is set)
	0 = Voltage level is acceptable for programming
bit 11	LVDSTAT: Low-Voltage Detect Status bit (LVD circuit must be enabled) ⁽¹⁾
	This bit is read-only and is automatically set, and cleared, by hardware.
	1 = Low-voltage event active
	0 = Low-voltage event NOT active
bit 10-4	Unimplemented: Read as '0'
bit 3-0	NVMOP<3:0>: NVM Operation bits
	These bits are writable when WREN = 0.
	1111 = Reserved
	0111 = Reserved
	0110 = No operation
	0101 = Program Flash (PFM) erase operation: erases PFM, if all pages are not write-protected
	0100 = Page erase operation: erases page selected by NVMADDR, if it is not write protected
	0011 = No operation
	0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected
	0000 = No operation

Note 1: This bit is cleared by setting NVMOP = 0000, and initiating a Flash operation (i.e., WR).

7.0 INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 8. "Interrupt Controller" (DS60001108), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX330/350/370/430/450/470 devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX330/350/370/430/450/470 interrupt module includes the following features:

- Up to 76 interrupt sources
- · Up to 46 interrupt vectors
- · Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Dedicated shadow set configurable for any priority level (see the FSRSSEL<2:0> bits (DEVCFG3<18:16>) in 28.0 "Special Features" for more information)
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

FIGURE 7-1: INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
31.24				CHEW1<	:31:24>					
	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
23:10	CHEW1<23:16>									
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15.0	CHEW1<15:8>									
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
				CHEW1	<7:0>					

REGISTER 9-6: CHEW1: CACHE WORD 1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW1<31:0>:** Word 1 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

REGISTER 9-7: CHEW2: CACHE WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31.24				CHEW2<	:31:24>				
22:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23.10	CHEW2<23:16>								
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15.0	CHEW2<15:8>								
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
				CHEW2	<7:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW2<31:0>:** Word 2 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

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REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
31:24	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	_	BITO ⁽¹⁾
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	_	_	—	_	_	—
45.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	—	—	—		PLEN<4:0>			
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	— — CRCCH<2:0>				•

Legend:

Logena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

- bit 29-28 BYTO<1:0>: CRC Byte Order Selection bits
 - 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
 - 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
 - 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
 - 00 = No swapping (i.e., source byte order)
- bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾
 - 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
 - 0 = Source data is written to the destination unaltered
- bit 26-25 Unimplemented: Read as '0'
- bit 24 BITO: CRC Bit Order Selection bit⁽¹⁾

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode):

- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 Unimplemented: Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits⁽¹⁾

<u>When CRCTYP (DCRCCON<15>) = 1</u> (CRC module is in IP Header mode): These bits are unused.

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode): Denotes the length of the polynomial - 1.

- bit 7 CRCEN: CRC Enable bit
 - 1 = CRC module is enabled and channel transfers are routed through the CRC module
 - 0 = CRC module is disabled and channel transfers proceed normally
- Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24				CHSSA<	:31:24>				
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23.10	CHSSA<23:16>								
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	CHSSA<15:8>								
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0				CHSSA	<7:0>				

REGISTER 10-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

 bit 31-0
 CHSSA<31:0> Channel Source Start Address bits

 Channel source start address.

 Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0						
21.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
31:24				CHDSA<	31:24>									
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
23:10	CHDSA<23:16>													
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
15:8				CHDSA	<15:8>									
7.0	R/W-0	R/W-0	R/W-0 R/W-0 R/W-0			R/W-0	R/W-0	R/W-0						
7:0	CHDSA<7:0>													

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits Channel destination start address.

 $\ensuremath{\textbf{Note:}}$ This must be the physical address of the destination.

TABLE 11-1: USB REGISTER MAP (CONTINUED)

ess		6									Bit	s							
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5390	LI1EP9	31:16	_					—	—	—	—	-	—	—	-	-	—	_	0000
0000	OTEL 9	15:0		—	—	—	—	—	—	—			—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5340		31:16		—	—	—	—	—	—	—	—			—	_	_	—		0000
5570	UTEI TU	15:0	_	_	_	_	_	—	_	_	—	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53R0	U1EP11	31:16		_	_	_	_	_	_	_	—		_	—			-		0000
5560		15:0		—	—	—	—	—		_	—	-	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5300		31:16		_	_	_	_	_	_	_	—		_	—			-		0000
5500	UILF 12	15:0		—	—	—	—	—		_	—	-	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5200		31:16	—	_	_	_	_	—	_	-	—	—	_	—	—	—	—	—	0000
55D0	UIEF 13	15:0	—	_	_	_	_	—	_	-	—	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_	_	_	_	_	_	_	_	_	_	—	_	_	_	_	0000
53E0	UTEP14	15:0	_					_	_		_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5250		31:16	_					_	_	_	_	_	_	—	_	—	_	_	0000
53FU	UTEP15	15:0									_			EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	-	—	—			—	
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	-	—	—			—	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	-	—	—			—	
7.0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
7.0	UACTPND			USLPGRD	USBBUSY ⁽¹⁾		USUSPEND	USBPWR

REGISTER 11-5: U1PWRC: USB POWER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 UACTPND: USB Activity Pending bit
 - 1 = USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
 0 = An interrupt is not pending
- bit 6-5 Unimplemented: Read as '0'
- bit 4 USLPGRD: USB Sleep Entry Guard bit
 - 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
 - 0 = USB module does not block Sleep entry
- bit 3 USBBUSY: USB Module Busy bit⁽¹⁾
 - 1 = USB module is active or disabled, but not ready to be enabled
 - 0 = USB module is not active and is ready to be enabled
 - **Note:** When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.
- bit 2 Unimplemented: Read as '0'
- bit 1 USUSPEND: USB Suspend Mode bit
 - 1 = USB module is placed in Suspend mode
 - (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
 - 0 = USB module operates normally
- bit 0 USBPWR: USB Operation Enable bit
 - 1 = USB module is turned on
 - 0 = USB module is disabled

(Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

12.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 12. "I/O Ports" (DS60001120), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

General purpose I/O pins are the simplest of peripherals. They allow the PIC[®] MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin. Following are key features of this module:

- · Individual output pin open-drain enable/disable
- · Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt
 when change in pin state is detected
- Operation during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.



	TIU32WIA43UFU04L, FIU32WIA43UF128L, FIU32WIA43UF236L, AND FIU32WIA47UF312L DEVIUES UNLY																		
ess										Bits	6								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6300		31:16	—	_	—	_		—	—	—	—	—	—	—	-	—	—	_	0000
0000	ANOLLD	15:0	—	_	_	—	—	—	—		—		—	—	ANSELD3	ANSELD2	ANSELD1	_	000E
6310	TRISD	31:16	—	_	—	—	_	—	—	—	—	—	—	—	—	—	—	—	0000
0010	ITRIOD	15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	xxxx
5320	PORTD	31:16	—	—	—	—	-	—	—	—	—	—	—	—	—	—	—	—	0000
0020		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
6330	LATD	31:16	_	—	—	—		—	—	—	—	_		_	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	XXXX
6340	ODCD	31:16	—	—	—	—	—	-	—	—	—		_	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	xxxx
6350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	_	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	XXXX
6360	CNPDD	31:16	-	-	-	-	-	—	-	-	-	-	-	-	-	_	-	-	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	XXXX
6370	CNCOND	31:16	-	_	-	_							_	_					0000
		15:0	ON		SIDL	_							_	_					0000
6380	CNEND	31:16	-			-			-	-	-		-	-		-		-	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	UNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	XXXX
6300	CNISTATO	31:16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0000
0390	CINGTATD	15:0	TATD15	STATD14	STATD13	STATD12	STATD11	STATD10	STATD9	STATD8	STATD7	STATD6	STATD5	STATD4	STATD3	STATD2	STATD1	STATD0	xxxx

TABLE 12-7: PORTD REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, PIC32MX370F512L,

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

TABLE 12-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

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o Technology	
Inc	

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ss			Bits or																
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FC14	RPE5R	31:16	—	—	—	—	—	—	-	_	_	—	—	—	_	—	—	_	0000
1014		15:0	-	—	—	—	—	—	—	_	_	—	—	—		RPE5	<3:0>		0000
FC20	RPF8R(1)	31:16	_		—	—	—	—	—	—	_	—	_	—	—	—	_	—	0000
. 010	14 2014	15:0	_		_	_	-	-	_			_		—		RPE8	<3:0>		0000
FC24	RPF9R ⁽¹⁾	31:16			—	—	—	—	—		_	—	_	—	—			—	0000
	14 2014	15:0			—	—	—	—	—		_	—	_	—		RPE9	<3:0>		0000
FC40	RPF0R	31:16	_		_	_	-	-	_			_		—	_			—	0000
		15:0			—	—	—	—	—		_	—	_	—		RPF0	<3:0>		0000
FC44	RPF1R	31:16			—	—	—	—	—		_	—	_	—	—			—	0000
		15:0			_	_	—	—						—		RPF1	<3:0>		0000
FC48	RPF2R ⁽³⁾	31:16			—	—	—	—						—				—	0000
		15:0			—	—	—	—						—		RPF2	<3:0>		0000
FC4C	RPF3R(2)	31:16			—	—	—	—	—			—	_	—		—	—	—	0000
		15:0	_		_	_	-	-	_			_		—		RPF3	<3:0>		0000
FC50	RPF4R	31:16			—	—	—	—	—		_	—	_	—	—			—	0000
1 000		15:0	_	-	-	-	-	—	_	_	_	—	_	—		RPF4	<3:0>		0000
FC54	RPE5R	31:16	_	—	—	—	—	—		_	_	_	_	—	_	_		—	0000
1001		15:0	—	-	—	—	—	—	_	_	_	_	—	—		RPF5	<3:0>		0000
FC58	RPF6R(2)	31:16	_	—	—	—	—	—		_	_	_	_	—	_	—		—	0000
1 000		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPF6	<3:0>		0000
EC.60	RPE8R(1)	31:16	_	—	—	—	—	—	—	_	_	—	_	—	—	—	—	—	0000
1000		15:0	_	—	—	—	—	—		_	_	_	_	—		RPF8	<3:0>		0000
FC70	RPF12R(1)	31:16	_	—	—	—	—	—		_	_	_	_	—	_	_		—	0000
1010	1011210	15:0	—	-	—	—	—	—	_	_	_	_	—	—		RPF12	2<3:0>		0000
FC74	RPF13R(1)	31:16	_	—	—	—	—	—	_	_	—	—	—	—	_	—	_	—	0000
10/1		15:0	_	—	—	—	—	—		_	_	_	_	—		RPF13	3<3:0>		0000
FC80		31:16	_	—	—	—	—	—		_	_		_	_	_			_	0000
1000		15:0	_	—	—	—	—	—		_	_	_	_	—		RPG0	<3:0>		0000
FC.84	RPG1R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	_	0000
1004		15:0	—	—	—	—	—	—	—	—	—	—	—	—		RPG1	<3:0>		0000
FC08	PPG6P	31:16	_	—	_	_	_	_		—					_			_	0000
1090	NEGOR	15:0	_	—	—	—	—	—	—	_	_	—	_	—		RPG6	6<3:0>		0000
ECOC	PPC7P	31:16	—	-	—	—	—	—	—	—	_	—	—	—	—	—	_	-	0000
FUBU	KFG/K	15:0	—	_	_	_	_	_		_	_	—	_	_		RPG7	<3:0>		0000
Legend	d: x = un	known v	alue on Re	eset: — = u	nimplement	ted, read as	s '0'. Reset	values are	shown in h	exadecimal									

Note 1: This register is not available on 64-pin devices.

2: This register is only available on devices without a USB module.

3: This register is not available on 64-pin devices with a USB module.

17.0 OUTPUT COMPARE

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 16. "Output Compare" (DS60001111), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of this module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Can operate from either of two available 16-bit time bases or a single 32-bit time base



FIGURE 17-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM

REGISTER 18-2:	SPIxCON2: SPI CONTROL REGISTER 2
----------------	----------------------------------

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7.0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7.0	AUDEN ⁽¹⁾	_	_	—	AUDMONO ^(1,2)	_	AUDMOD)<1:0> ^(1,2)

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 SPISGNEXT: Sign Extend Read Data from the RX FIFO bit
 - 1 = Data from RX FIFO is sign extended
 - 0 = Data from RX FIFO is not sign extened
- bit 14-13 Unimplemented: Read as '0'
- bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
 - 1 = Frame Error overflow generates error events
 - 0 = Frame Error does not generate error events
- bit 11 SPIROVEN: Enable Interrupt Events via SPIROV bit
 - 1 = Receive overflow generates error events
 - 0 = Receive overflow does not generate error events
- bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
 - 1 = Transmit Underrun Generates Error Events
 - 0 = Transmit Underrun Does Not Generates Error Events
- bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
 - 1 = A ROV is not a critical error; during ROV data in the fifo is not overwritten by receive data
 - 0 = A ROV is a critical error which stop SPI operation
- bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
 - 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
 - 0 = A TUR is a critical error which stop SPI operation
- bit 7 AUDEN: Enable Audio CODEC Support bit⁽¹⁾
 - 1 = Audio protocol is enabled
 - 0 = Audio protocol is disabled
- bit 6-5 Unimplemented: Read as '0'

bit 3 AUDMONO: Transmit Audio Data Format bit^(1,2)

- 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
 0 = Audio data is stereo
- bit 2 Unimplemented: Read as '0'
- bit 1-0 AUDMOD<1:0>: Audio Protocol Mode bit^(1,2)
 - 11 = PCM/DSP mode
 - 10 = Right Justified mode
 - 01 = Left Justified mode
 - $00 = I^2S \mod$
- **Note 1:** This bit can only be written when the ON bit = 0.
 - **2:** This bit is only valid for AUDEN = 1.

REGISTER 21-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

- bit 5-2 WAITM<3:0>: Data Read/Write Strobe Wait States bits⁽¹⁾
 - 1111 = Wait of 16 Трв • •
 - 0001 = Wait of 2 Трв 0000 = Wait of 1 Трв (default)
- bit 1-0 WAITE<1:0>: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾
 - 11 = Wait of 4 TPB 10 = Wait of 3 TPB 01 = Wait of 2 TPB
 - 00 = Wait of 1 Трв (default)

For Read operations: 11 = Wait of 3 TPB 10 = Wait of 2 TPB 01 = Wait of 1 TPB 00 = Wait of 0 TPB (default)

- **Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPB cycle for a write operation; WAITB = 1 TPB cycle, WAITE = 0 TPB cycles for a read operation.
 - 2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.
 - **3:** These pins are active when MODE16 = 1 (16-bit mode).

25.1 Control Register

TABLE 25-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	50									Bits									ú
	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
0000		31:16	_	_	-	—	-	_	_	—	—	_	—	_	_	—	_	_	0000
9000	CVRCON	15:0	ON	_	—	_	—	_	—	_	_	CVROE	CVRR	CVRSS		CVR<	3:0>		0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

- bit 10 EDGSEQEN: Edge Sequence Enable bit 1 = Edge 1 must occur before Edge 2 can occur 0 = No edge sequence is needed bit 9 **IDISSEN:** Analog Current Source Control bit⁽²⁾ 1 = Analog current source output is grounded 0 = Analog current source output is not grounded CTTRIG: Trigger Control bit bit 8 1 = Trigger output is enabled 0 = Trigger output is disabled bit 7-2 ITRIM<5:0>: Current Source Trim bits 011111 = Maximum positive change from nominal current 011110 000001 = Minimum positive change from nominal current 000000 = Nominal current output specified by IRNG<1:0> 1111111 = Minimum negative change from nominal current 100010 100001 = Maximum negative change from nominal current IRNG<1:0>: Current Range Select bits⁽³⁾ bit 1-0 11 = 100 times base current 10 = 10 times base current 01 = Base current level 00 = 1000 times base current⁽⁴⁾
- Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 31-42) in Section 31.0 "Electrical Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	—	—	—	—	—	FPLLODIV<2:0>		
15:8	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	UPLLEN ⁽¹⁾	—	—	—	—	UPLLIDIV<2:0> ⁽¹⁾		
7:0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
	—	FPLLMUL<2:0>			—	FPLLIDIV<2:0>		

DEVCFG2: DEVICE CONFIGURATION WORD 2 REGISTER 28-3:

Legend:	r = Reserved bit	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-19 Reserved: Write '1'

bit 15

bit 7

bit 18-16 FPLLODIV<2:0>: Default PLL Output Divisor bits

- 111 = PLL output divided by 256 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2 000 = PLL output divided by 1 UPLLEN: USB PLL Enable bit⁽¹⁾ 1 = Disable and bypass USB PLL 0 = Enable USB PLL bit 14-11 Reserved: Write '1' bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits⁽¹⁾ 111 = 12x divider 110 = 10x divider 101 = 6x divider100 = 5x divider 011 = 4x divider 010 = 3x divider 001 = 2x divider 000 = 1x dividerReserved: Write '1' bit 6-4 FPLLMUL<2:0>: PLL Multiplier bits 111 = 24x multiplier 110 = 21x multiplier 101 = 20x multiplier 100 = 19x multiplier 011 = 18x multiplier 010 = 17x multiplier 001 = 16x multiplier 000 = 15x multiplier
- bit 3 Reserved: Write '1'

Note 1: This bit is available on PIC32MX4XX devices only.

30.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

30.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent[®] and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika[®]

DC CHARACTERISTICS			Standard Oper (unless otherw Operating temp	$\begin{array}{l} \textbf{nditions: 2.3V to 3.6V} \\ \textbf{ad)} \\ 0^\circ C \leq TA \leq +70^\circ C \text{ for Commercial} \\ -40^\circ C \leq TA \leq +85^\circ C \text{ for Industrial} \\ -40^\circ C \leq TA \leq +105^\circ C \text{ for V-temp} \end{array}$			
Param. No.	Symb.	Characteristics	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions
DI60b	Іісн	Input High Injection Current	0	_	+5 ^(8,9,10)	mA	Pins with Analog functions. Exceptions: [SOSCI, SOSCO, OSC1, D+, D-] = 0 mA max. Digital 5V tolerant desig- nated pins (VIH < $5.5V$) ⁽⁹⁾ . Exceptions: [All] = 0 mA max. Digital non-5V tolerant desig- nated pins. Exceptions: [N/A] = 0 mA max.
DI60c	∑lict	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽¹¹⁾	_	+20 ⁽¹¹⁾	mA	Absolute instantaneous sum of all \pm input injection cur- rents from all I/O pins (IICL + IICH) $\leq \sum$ IICT

TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: See the "Device Pin Tables" section for the 5V tolerant pins.
- 6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the userselectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.
- 7: VIL source < (Vss 0.3). Characterized but not tested.
- 8: VIH source > (VDD + 0.3) for non-5V tolerant pins only.
- **9:** Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.
- **10:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS 0.3)).
- 11: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If Note 7, IICL = (((Vss 0.3) VIL source) / Rs). If Note 8, IICH = ((IICH source (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (Vss 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

TABLE 31-18: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)					
			$\begin{array}{ll} Operating \ temperature & 0^{\circ}C \leq TA \leq +70^{\circ}C \ for \ Commercial \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \ for \ Industrial \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \ for \ V\text{-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions	
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	_	50 50	MHz MHz	EC (Note 4) ECPLL (Note 3)	
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT (Note 4)	
OS12			4		10	MHz	XTPLL (Notes 3,4)	
OS13			10	—	25	MHz	HS (Note 4)	
OS14			10		25	MHz	HSPLL (Notes 3,4)	
OS15			32	32.768	100	kHz	Sosc (Note 4)	
OS20	Tosc	Tosc = 1/Fosc = Tcy (Note 2)	_	—	_	_	See parameter OS10 for Fosc value	
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.45 x Tosc	—	—	ns	EC (Note 4)	
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	_	—	0.05 x Tosc	ns	EC (Note 4)	
OS40	Tost	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	_	1024	_	Tosc	(Note 4)	
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 4)	
OS42	Gм	External Oscillator Transconductance (Primary Oscillator only)	_	12		mA/V	VDD = 3.3V, TA = +25°C (Note 4)	

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

- 2: Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.
- **3:** PLL input requirements: 4 MHz \leq FPLLIN \leq 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 4: This parameter is characterized, but not tested in manufacturing.