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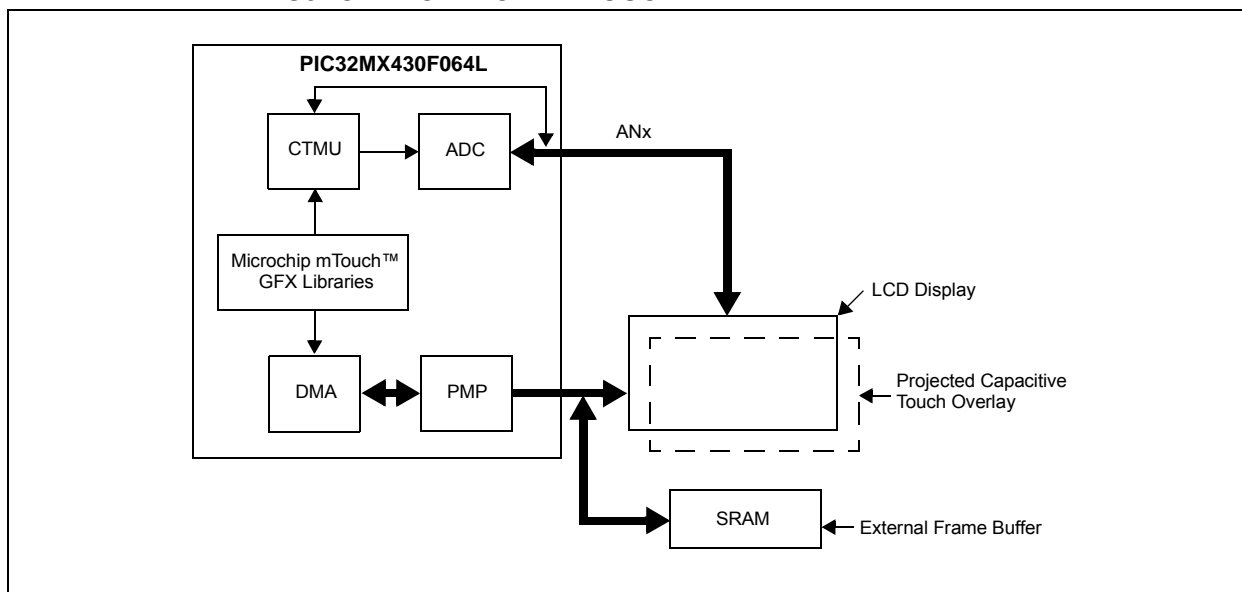
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx450f256l-v-pf

PIC32MX330/350/370/430/450/470

FIGURE 2-8: LOW-COST CONTROLLERLESS (LCC) GRAPHICS APPLICATION WITH PROJECTED CAPACITIVE TOUCH



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REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDKPBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDKPBA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits

When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** Read-Only bits

Value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

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REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SRIPL<2:0> ⁽¹⁾		
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	VEC<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits⁽¹⁾

11111-00000 = The interrupt vector that is presented to the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits

Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

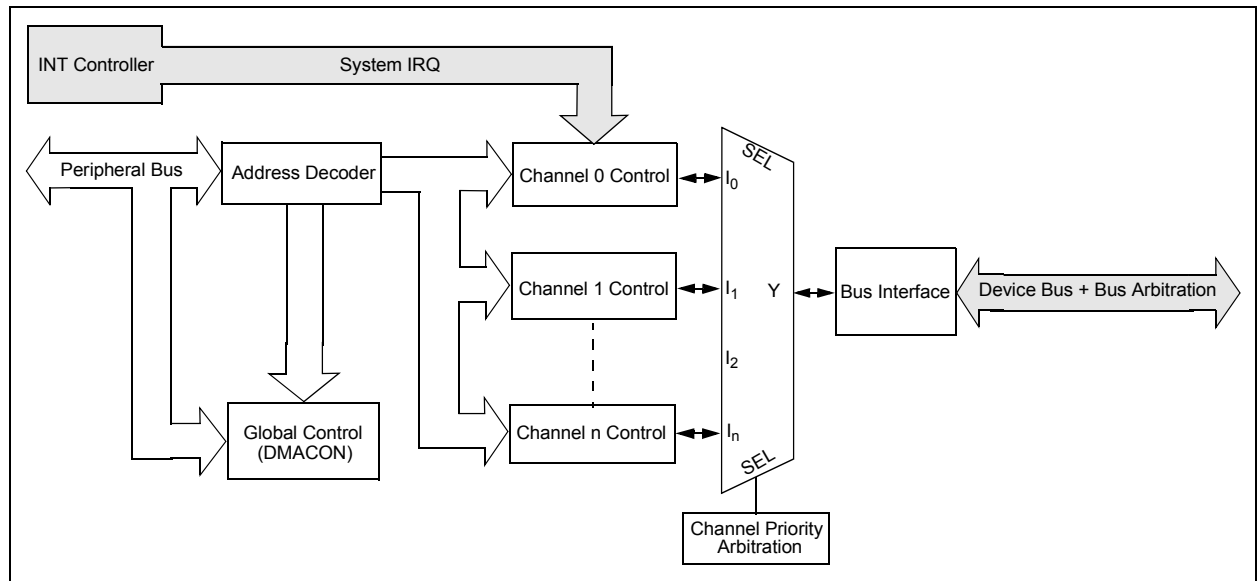
The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, etc.) or memory itself.

Following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
 - Auto-increment source and destination address registers
 - Source and destination pointers
 - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
 - Transfer granularity, down to byte level
 - Bytes need not be word-aligned at source and destination

- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- Flexible DMA requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA debug support features:
 - Most recent address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- CRC Generation module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



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REGISTER 10-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0> ⁽¹⁾							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0> ⁽¹⁾							
7:0	S-0 CFORCE	S-0 CABORT	R/W-0 PATEN	R/W-0 SIRQEN	R/W-0 AIRQEN	U-0 —	U-0 —	U-0 —

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>**: Channel Transfer Abort IRQ bits⁽¹⁾

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•
•
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>**: Channel Transfer Start IRQ bits⁽¹⁾

11111111 = Interrupt 255 will initiate a DMA transfer

•
•
•

00000001 = Interrupt 1 will initiate a DMA transfer

00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE**: DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 **CABORT**: DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 **PATEN**: Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 **SIRQEN**: Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN**: Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

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REGISTER 11-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS
	BTSEF	BMXEF	DMAEF ⁽¹⁾	BTOEF ⁽²⁾	DFN8EF	CRC16EF	CRC5EF ⁽⁴⁾ EOFEF ^(3,5)	PIDEF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit

- 1 = Packet is rejected due to bit stuff error
- 0 = Packet is accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit

- 1 = The base address, of the BDT, or the address of an individual buffer pointed to by a BDT entry, is invalid.
- 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit⁽¹⁾

- 1 = USB DMA error condition detected
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit⁽²⁾

- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit

- 1 = Data field received is not an integral number of bytes
- 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit

- 1 = Data packet rejected due to CRC16 error
- 0 = Data packet accepted

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

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TABLE 12-1: INPUT PIN SELECTION

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPN Pin Selection
INT3	INT3R	INT3R<3:0>	0000 = RPD2 0001 = RPG8 0010 = RPF4 0011 = RPD10 0100 = RPF1 0101 = RPB9 0110 = RPB10 0111 = RPC14 1000 = RPB5 1001 = Reserved 1010 = RPC1 ⁽³⁾ 1011 = RPD14 ⁽³⁾ 1100 = RPG1 ⁽³⁾ 1101 = RPA14 ⁽³⁾ 1110 = Reserved 1111 = RPF2 ⁽¹⁾
T2CK	T2CKR	T2CKR<3:0>	
IC3	IC3R	IC3R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	
U2RX	U2RXR	U2RXR<3:0>	
$\overline{\text{U5CTS}}$	U5CTSR ⁽³⁾	U5CTSR<3:0>	
REFCLKI	REFCLKIR	REFCLKIR<3:0>	
INT4	INT4R	INT4R<3:0>	0000 = RPD3 0001 = RPG7 0010 = RPF5 0011 = RPD11 0100 = RPF0 0101 = RPB1 0110 = RPE5 0111 = RPC13 1000 = RPB3 1001 = Reserved 1010 = RPC4 ⁽³⁾ 1011 = RPD15 ⁽³⁾ 1100 = RPG0 ⁽³⁾ 1101 = RPA15 ⁽³⁾ 1110 = RPF2 ⁽¹⁾ 1111 = RPF7 ⁽²⁾
T5CK	T5CKR	T5CKR<3:0>	
IC4	IC4R	IC4R<3:0>	
U3RX	U3RXR	U3RXR<3:0>	
$\overline{\text{U4CTS}}$	U4CTSR	U4CTSR<3:0>	
SDI1	SDI1R	SDI1R<3:0>	
SDI2	SDI2R	SDI2R<3:0>	
INT2	INT2R	INT2R<3:0>	0000 = RPD9 0001 = RPG6 0010 = RPB8 0011 = RPB15 0100 = RPD4 0101 = RPB0 0110 = RPE3 0111 = RPB7 1000 = Reserved 1001 = RPF12 ⁽³⁾ 1010 = RPD12 ⁽³⁾ 1011 = RPF8 ⁽³⁾ 1100 = RPC3 ⁽³⁾ 1101 = RPE9 ⁽³⁾ 1110 = Reserved 1111 = RPB2
T4CK	T4CKR	T4CKR<3:0>	
IC2	IC2R	IC2R<3:0>	
IC5	IC5R	IC5R<3:0>	
$\overline{\text{U1CTS}}$	U1CTSR	U1CTSR<3:0>	
$\overline{\text{U2CTS}}$	U2CTSR	U2CTSR<3:0>	
$\overline{\text{SS1}}$	SS1R	SS1R<3:0>	

Note 1: This selection is not available on 64-pin USB devices.

2: This selection is only available on 100-pin General Purpose devices.

3: This selection is not available on 64-pin USB and General Purpose devices.

4: This selection is only available on General Purpose devices.

TABLE 12-7: PORTD REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, PIC32MX370F512L, PIC32MX430F064L, PIC32MX450F128L, PIC32MX450F256L, AND PIC32MX470F512L DEVICES ONLY

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	ANSELD3	ANSELD2	ANSELD1	—	000E
6310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	xxxx
5320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
6330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
6340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	xxxx
6350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	xxxx
6360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	xxxx
6370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	xxxx
6390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	CN STATD8	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	xxxx

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 12-11: PORTF REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, AND PIC32MX370F512L DEVICES ONLY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	xxxx
6520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	xxxx
6550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPUF13	CNPUF12	—	—	—	CNPUF8	CNPUF7	CNPUF6	CNPUF5	CNPUF4	CNPDF3	CNPUF2	CNPUF1	CNPUF0	xxxx
6560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPDF13	CNPDF12	—	—	—	CNPDF8	CNPDF7	CNPDF6	CNPDF5	CNPDF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	xxxx
6570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNIEF13	CNIEF12	—	—	—	CNIEF8	CNIEF7	—	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	xxxx
6590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CN STATF13	CN STATF12	—	—	—	CN STATF8	CN STATF7	—	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	xxxx

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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REGISTER 19-2: I2CxSTAT: I²C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R-0, HSC ACKSTAT	R-0, HSC TRSTAT	U-0 —	U-0 —	U-0 —	R/C-0, HS BCL	R-0, HSC GCSTAT	R-0, HSC ADD10
7:0	R/C-0, HS IWCOL	R/C-0, HS I2COV	R-0, HSC D_A	R/C-0, HSC P	R/C-0, HSC S	R-0, HSC R_W	R-0, HSC RBF	R-0, HSC TBF

Legend:	HS = Set in hardware	HSC = Hardware set/cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I²C master, applicable to master transmit operation)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 8 **TRMT**: Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer
- bit 7-6 **URXISEL<1:0>**: Receive Interrupt Mode Selection bit
11 = Reserved; do not use
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)
- bit 5 **ADDEN**: Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE**: Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received
- bit 3 **PERR**: Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected
- bit 2 **FERR**: Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected
- bit 1 **OERR**: Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed
- bit 0 **URXDA**: Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

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20.2 Timing Diagrams

Figure 20-2 and Figure 20-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 20-2: UART RECEPTION

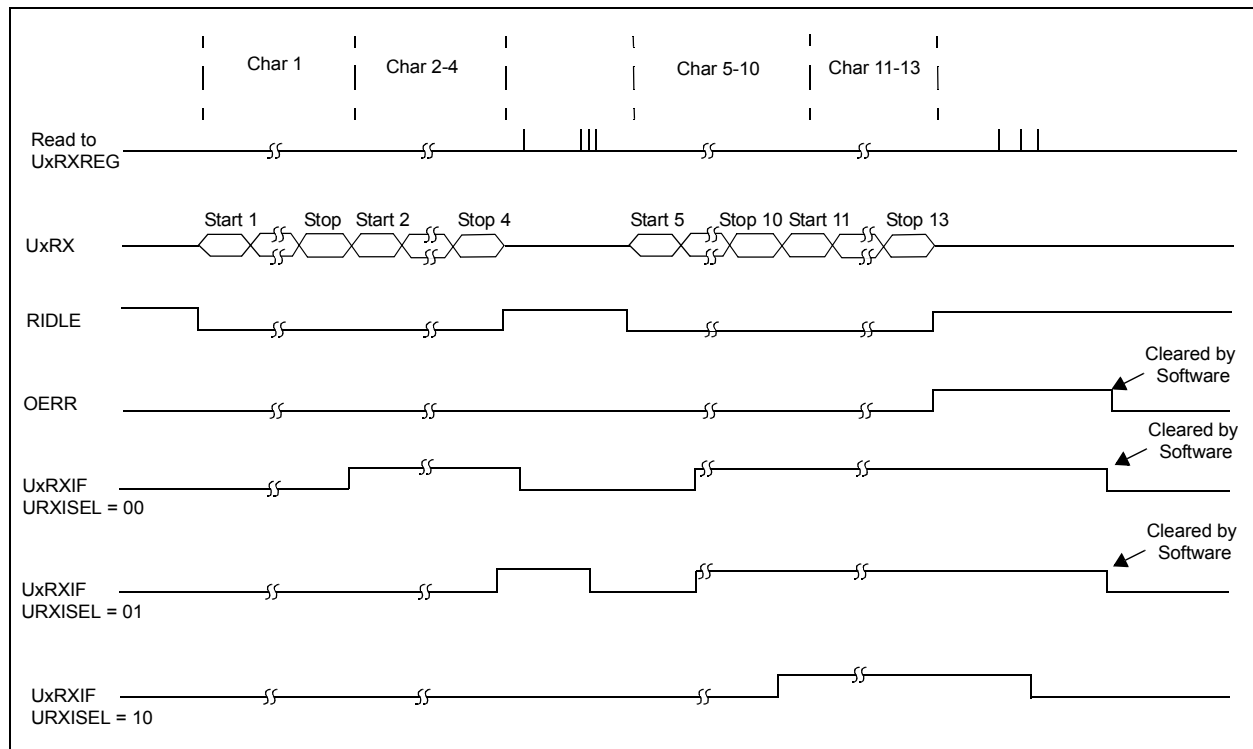
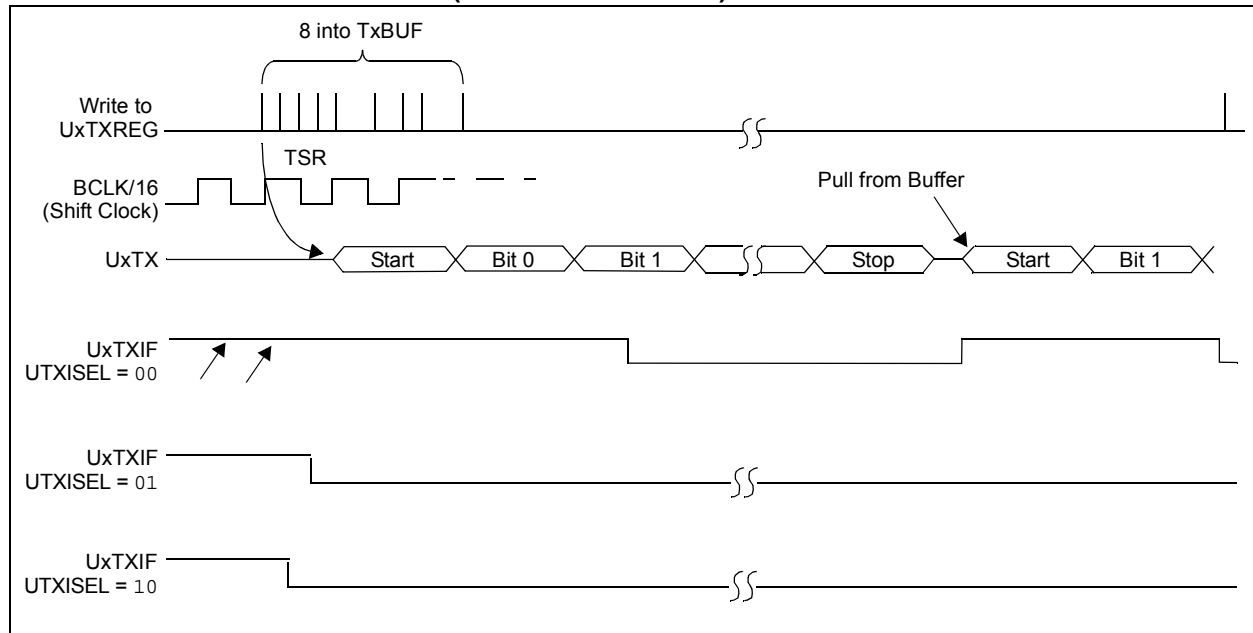


FIGURE 20-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



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REGISTER 23-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	—	CSCNA	—	—
7:0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFS	—	SMPI<3:0>				BUFM	ALTS

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	AVss
001	External VREF+ pin	AVss
010	AVDD	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVss

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the sample and hold amplifier are connected to VREFL

0 = Disable Offset Calibration mode

The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit

1 = Scan inputs

0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1.

1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7

0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence

1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence

.

.

.

0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence

0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADC1BUF8

0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples

0 = Always use Sample A input multiplexer settings

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REGISTER 28-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

- bit 11-5 **Reserved:** Write '1'
- bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits
- 11 = PGEC1/PGED1 pair is used
 - 10 = PGEC2/PGED2 pair is used
 - 01 = PGEC3/PGED3 pair is used
 - 00 = Reserved
- bit 2 **JTAGEN:** JTAG Enable bit⁽¹⁾
- 1 = JTAG is enabled
 - 0 = JTAG is disabled
- bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
- 1x = Debugger is disabled
 - 0x = Debugger is enabled

Note 1: This bit sets the value for the JTAGEN bit in the CFGCON register.

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28.2 On-Chip Voltage Regulator

All PIC32MX330/350/370/430/450/470 devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX330/350/370/430/450/470 family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 28-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 31.1 “DC Characteristics”**.

Note: It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

28.2.1 HIGH VOLTAGE DETECT (HVD)

The HVD module monitors the core voltage at the VCAP pin. If a voltage above the required level is detected on VCAP, the I/O pins are disabled and the device is held in Reset as long as the HVD condition persists. See parameter HV10 (VHVD) in Table 31-11 in **Section 31.1 “DC Characteristics”** for more information.

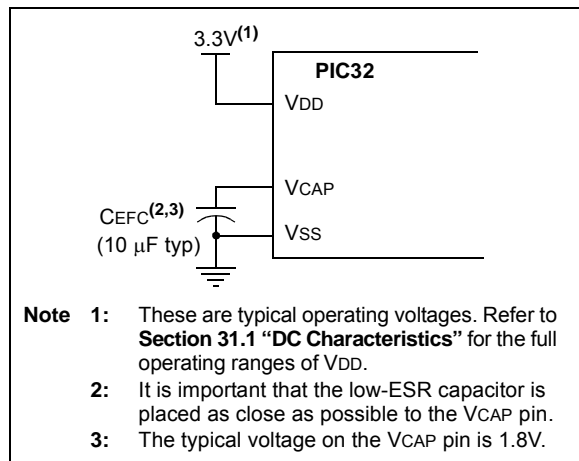
28.2.2 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

28.2.3 ON-CHIP REGULATOR AND BOR

PIC32MX330/350/370/430/450/470 devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 31.1 “DC Characteristics”**.

FIGURE 28-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



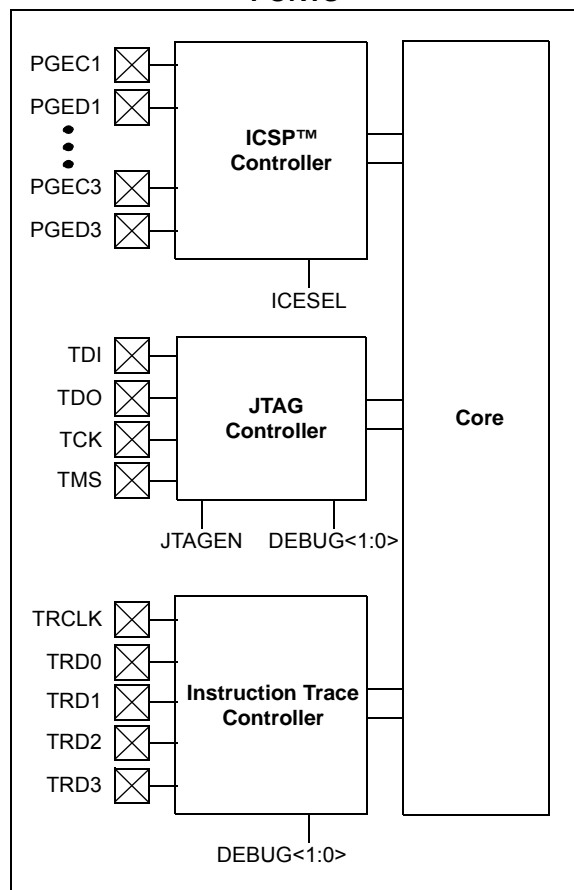
28.3 Programming and Diagnostics

PIC32MX330/350/370/430/450/470 devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 28-2: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS



PIC32MX330/350/370/430/450/470

TABLE 31-12: DC CHARACTERISTICS: PROGRAM MEMORY⁽³⁾

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
D138	TWW	Word Write Cycle Time ⁽⁴⁾	44	—	59	μs	—
D136	TRW	Row Write Cycle Time ^(2,4)	2.8	3.3	3.8	ms	—
D137	TPE	Page Erase Cycle Time ⁽⁴⁾	22	—	29	ms	—
D139	TCE	Chip Erase Cycle Time ⁽⁴⁾	86	—	116	ms	—

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

- 2:** The minimum SYSCLK for row programming is 8 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).
- 3:** Refer to the “PIC32 Flash Programming Specification” (DS60001145) for operating conditions during programming and erase cycles.
- 4:** This parameter depends on the FRC accuracy (see Table 31-20) and the FRC tuning values (see Register 8-2).

TABLE 31-13: DC CHARACTERISTICS: PROGRAM FLASH MEMORY WAIT STATE

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp	
Required Flash Wait States	SYSCLK	Units	Conditions
0 Wait State	0-40	MHz	-40°C to +85°C
	0-30	MHz	-40°C to +105°C
1 Wait State	41-80	MHz	-40°C to +85°C
	31-60	MHz	-40°C to +105°C
2 Wait States	81-100	MHz	-40°C to +85°C
	61-80	MHz	-40°C to +105°C
3 Wait States	101-120	MHz	0°C to +70°C

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TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	ns	—
			400 kHz mode	TPB * (BRG + 2)	—	ns	
			1 MHz mode (Note 2)	TPB * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode (Note 2)	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode (Note 2)	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	—
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See Note 3

Note 1: BRG is the value of the I²C Baud Rate Generator.

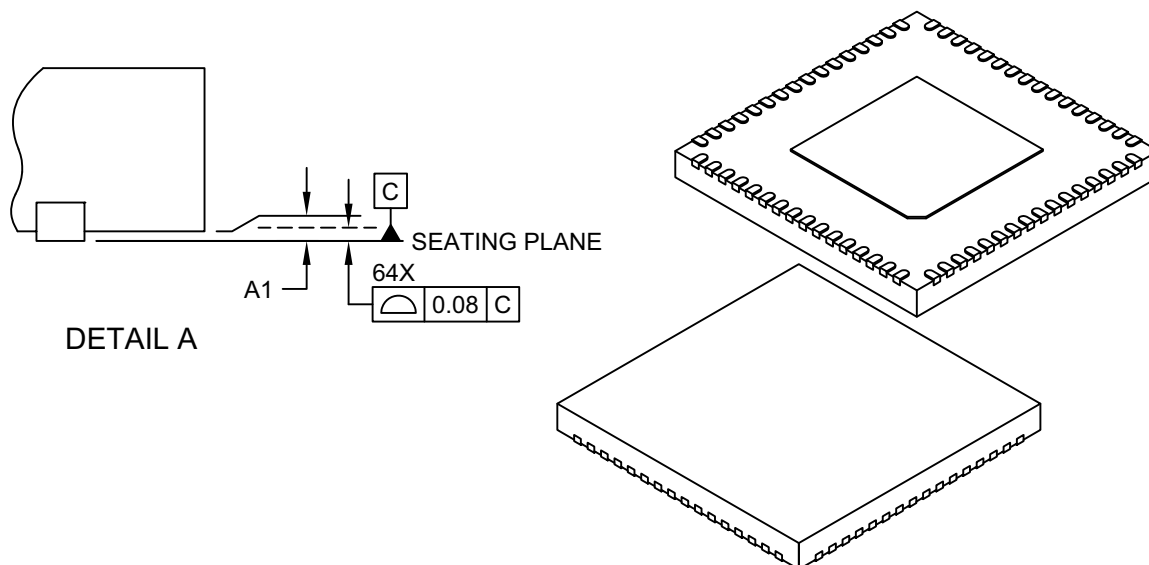
2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

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64-Terminal Plastic Quad Flat Pack, No Lead (RG) 9x9x0.9 mm Body [QFN] Saw Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Terminals	N		64		
Pitch	e		0.50 BSC		
Overall Height	A		0.80	0.85	0.90
Standoff	A1		0.00	0.02	0.05
Standoff	A3		0.20 REF		
Overall Width	E		9.00 BSC		
Exposed Pad Width	E2		4.60	4.70	4.80
Overall Length	D		9.00 BSC		
Exposed Pad Length	D2		4.60	4.70	4.80
Terminal Width	b		0.15	0.20	0.25
Terminal Length	L		0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		1.755 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

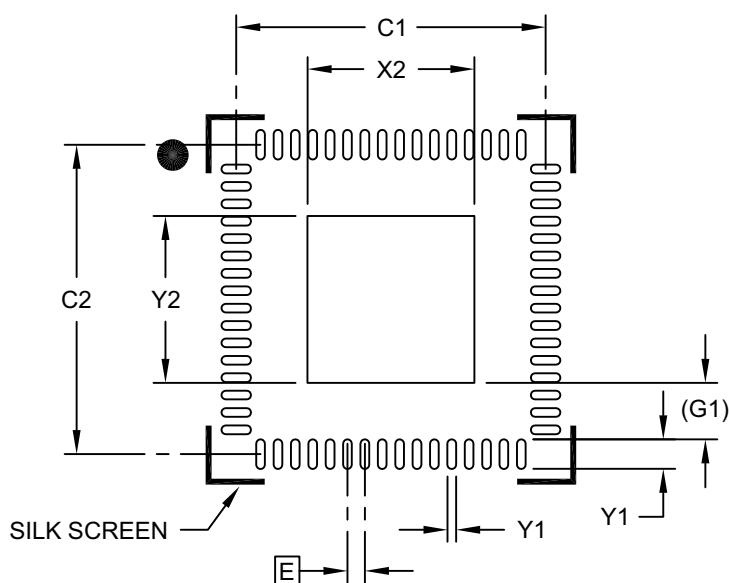
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-260A Sheet 2 of 2

PIC32MX330/350/370/430/450/470

64-Lead Very Thin Plastic Quad Flat, No Lead Package (RG) - 9x9x1.0 mm Body [QFN] 4.7x4.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			4.80
Optional Center Pad Length	Y2			4.80
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.25
Contact Pad Length (X64)	Y1			0.85
Contact Pad to Center Pad (X64)	G1	1.625 REF		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2260A

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ALRMDATE (Alarm Date Value)	232
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DCHxDAT (DMA Channel x Pattern Data)	111
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DCHxDSA (DMA Channel x Destination Start Address)	107
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