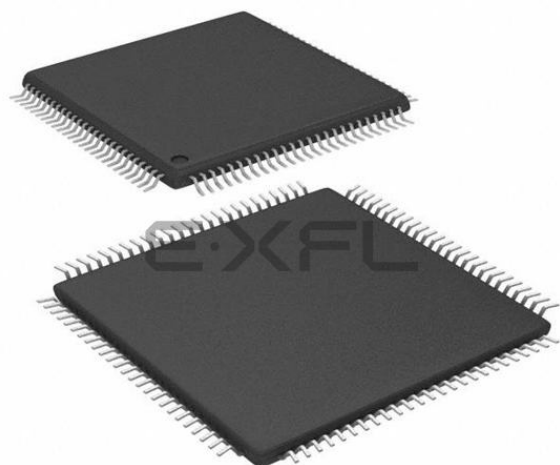




Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                                   |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                            |
| Core Processor             | MIPS32® M4K™                                                                                                                                                                      |
| Core Size                  | 32-Bit Single-Core                                                                                                                                                                |
| Speed                      | 120MHz                                                                                                                                                                            |
| Connectivity               | I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG                                                                                                                     |
| Peripherals                | Brown-out Detect/Reset, DMA, POR, PWM, WDT                                                                                                                                        |
| Number of I/O              | 81                                                                                                                                                                                |
| Program Memory Size        | 256KB (256K x 8)                                                                                                                                                                  |
| Program Memory Type        | FLASH                                                                                                                                                                             |
| EEPROM Size                | -                                                                                                                                                                                 |
| RAM Size                   | 64K x 8                                                                                                                                                                           |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V                                                                                                                                                                       |
| Data Converters            | A/D 28x10b                                                                                                                                                                        |
| Oscillator Type            | Internal                                                                                                                                                                          |
| Operating Temperature      | 0°C ~ 70°C (TA)                                                                                                                                                                   |
| Mounting Type              | Surface Mount                                                                                                                                                                     |
| Package / Case             | 100-TQFP                                                                                                                                                                          |
| Supplier Device Package    | 100-TQFP (12x12)                                                                                                                                                                  |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx450f256lt-120-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx450f256lt-120-pt</a> |

# PIC32MX330/350/370/430/450/470

**TABLE 5: PIN NAMES FOR 100-PIN DEVICES**

| 100-PIN TQFP (TOP VIEW) <sup>(1,2)</sup>                                                             |                                       |       |                                 |
|------------------------------------------------------------------------------------------------------|---------------------------------------|-------|---------------------------------|
| <b>PIC32MX430F064L</b><br><b>PIC32MX450F128L</b><br><b>PIC32MX450F256L</b><br><b>PIC32MX470F512L</b> |                                       | 100   | 1                               |
| Pin #                                                                                                | Full Pin Name                         | Pin # | Full Pin Name                   |
| 1                                                                                                    | RG15                                  | 36    | VSS                             |
| 2                                                                                                    | VDD                                   | 37    | VDD                             |
| 3                                                                                                    | AN22/RPE5/PMD5/RE5                    | 38    | TCK/CTED2/RA1                   |
| 4                                                                                                    | AN23/PMD6/RE6                         | 39    | RPF13/RF13                      |
| 5                                                                                                    | AN27/PMD7/RE7                         | 40    | RPF12/RF12                      |
| 6                                                                                                    | RPC1/RC1                              | 41    | AN12/PMA11/RB12                 |
| 7                                                                                                    | RPC2/RC2                              | 42    | AN13/PMA10/RB13                 |
| 8                                                                                                    | RPC3/RC3                              | 43    | AN14/RPB14/CTED5/PMA1/RB14      |
| 9                                                                                                    | RPC4/CTED7/RC4                        | 44    | AN15/RPB15/OCFB/CTED6/PMA0/RB15 |
| 10                                                                                                   | AN16/C1IND/RPG6/SCK2/PMA5/RG6         | 45    | VSS                             |
| 11                                                                                                   | AN17/C1INC/RPG7/PMA4/RG7              | 46    | VDD                             |
| 12                                                                                                   | AN18/C2IND/RPG8/PMA3/RG8              | 47    | RPD14/RD14                      |
| 13                                                                                                   | MCLR                                  | 48    | RPD15/RD15                      |
| 14                                                                                                   | AN19/C2INC/RPG9/PMA2/RG9              | 49    | RPF4/PMA9/RF4                   |
| 15                                                                                                   | VSS                                   | 50    | RPF5/PMA8/RF5                   |
| 16                                                                                                   | VDD                                   | 51    | USBID/RF3                       |
| 17                                                                                                   | TMS/CTED1/RA0                         | 52    | RPF2/RF2                        |
| 18                                                                                                   | RPE8/RE8                              | 53    | RPF8/RF8                        |
| 19                                                                                                   | RPE9/RE9                              | 54    | VBUS                            |
| 20                                                                                                   | AN5/C1INA/RPB5/VBUSON/RB5             | 55    | VUSB3V3                         |
| 21                                                                                                   | AN4/C1INB/RB4                         | 56    | D-                              |
| 22                                                                                                   | PGED3/AN3/C2INA/RPB3/RB3              | 57    | D+                              |
| 23                                                                                                   | PGEC3/AN2/C2INB/RPB2/CTED13/RB2       | 58    | SCL2/RA2                        |
| 24                                                                                                   | PGEC1/AN1/RPB1/CTED12/RB1             | 59    | SDA2/RA3                        |
| 25                                                                                                   | PGED1/AN0/RPB0/RB0                    | 60    | TDI/CTED9/RA4                   |
| 26                                                                                                   | PGEC2/AN6/RPB6/RB6                    | 61    | TDO/RA5                         |
| 27                                                                                                   | PGED2/AN7/RPB7/CTED3/RB7              | 62    | VDD                             |
| 28                                                                                                   | VREF-/CVREF-/PMA7/RA9                 | 63    | OSC1/CLKI/RC12                  |
| 29                                                                                                   | VREF+/CVREF+/PMA6/RA10                | 64    | OSC2/CLKO/RC15                  |
| 30                                                                                                   | AVDD                                  | 65    | VSS                             |
| 31                                                                                                   | AVSS                                  | 66    | SCL1/RPA14/RA14                 |
| 32                                                                                                   | AN8/RPB8/CTED10/RB8                   | 67    | SDA1/RPA15/RA15                 |
| 33                                                                                                   | AN9/RPB9/CTED4/RB9                    | 68    | RPD8/RTCC/RD8                   |
| 34                                                                                                   | CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10 | 69    | RPD9/RD9                        |
| 35                                                                                                   | AN11/PMA12/RB11                       | 70    | RPD10/SCK1/PMCS2/RD10           |

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 “Peripheral Pin Select”** for restrictions.
  - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 “I/O Ports”** for more information.

## Referenced Sources

This device data sheet is based on the following individual sections of the “PIC32 Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note:** To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 website: <http://www.microchip.com/pic32>.

- **Section 1. “Introduction”** (DS60001127)
- **Section 2. “CPU”** (DS60001113)
- **Section 3. “Memory Organization”** (DS60001115)
- **Section 4. “Prefetch Cache”** (DS60001119)
- **Section 5. “Flash Program Memory”** (DS60001121)
- **Section 6. “Oscillator Configuration”** (DS60001112)
- **Section 7. “Resets”** (DS60001118)
- **Section 8. “Interrupt Controller”** (DS60001108)
- **Section 9. “Watchdog Timer and Power-up Timer”** (DS60001114)
- **Section 10. “Power-Saving Features”** (DS60001130)
- **Section 12. “I/O Ports”** (DS60001120)
- **Section 13. “Parallel Master Port (PMP)”** (DS60001128)
- **Section 14. “Timers”** (DS60001105)
- **Section 15. “Input Capture”** (DS60001122)
- **Section 16. “Output Compare”** (DS60001111)
- **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104)
- **Section 19. “Comparator”** (DS60001110)
- **Section 20. “Comparator Voltage Reference (CVREF)”** (DS60001109)
- **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107)
- **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106)
- **Section 24. “Inter-Integrated Circuit (I<sup>2</sup>C)”** (DS60001116)
- **Section 27. “USB On-The-Go (OTG)”** (DS60001126)
- **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125)
- **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117)
- **Section 32. “Configuration”** (DS60001124)
- **Section 33. “Programming and Diagnostics”** (DS60001129)
- **Section 37. “Charge Time Measurement Unit (CTMU)”** (DS60001167)

# PIC32MX330/350/370/430/450/470

**REGISTER 9-2: CHEACC: CACHE ACCESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | R/W-0          | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | CHEWEN         | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | U-0            | U-0            | U-0            | U-0            | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | —              | —              | —              | —              | CHEIDX<3:0>    |                |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **CHEWEN:** Cache Access Enable bits for registers CHETAG, CHEMSK, CHEW0, CHEW1, CHEW2, and CHEW3

1 = The cache line selected by CHEIDX<3:0> is writeable

0 = The cache line selected by CHEIDX<3:0> is not writeable

bit 30-4 **Unimplemented:** Write '0'; ignore read

bit 3-0 **CHEIDX<3:0>:** Cache Line Index bits

The value selects the cache line for reading or writing.

# PIC32MX330/350/370/430/450/470

---

NOTES:

# PIC32MX330/350/370/430/450/470

## REGISTER 11-12: U1ADDR: USB ADDRESS REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | LSPDEN         | DEVADDR<6:0>   |                |                |                |                |               |               |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low Speed Enable Indicator bit

1 = Next token command to be executed at Low Speed

0 = Next token command to be executed at Full Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

## REGISTER 11-13: U1FRML: USB FRAME NUMBER LOW REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | R-0            | R-0            | R-0            | R-0            | R-0            | R-0            | R-0           | R-0           |
|           | FRML<7:0>      |                |                |                |                |                |               |               |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

**TABLE 12-11: PORTF REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, AND PIC32MX370F512L DEVICES ONLY**

| Virtual Address<br>(BF88_#) | Register<br>Name(s) | Bit Range | Bits  |       |               |               |       |       |      |              |              |        |              |              |              |              |              |              | All<br>Resets |
|-----------------------------|---------------------|-----------|-------|-------|---------------|---------------|-------|-------|------|--------------|--------------|--------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|
|                             |                     |           | 31/15 | 30/14 | 29/13         | 28/12         | 27/11 | 26/10 | 25/9 | 24/8         | 23/7         | 22/6   | 21/5         | 20/4         | 19/3         | 18/2         | 17/1         | 16/0         |               |
| 6510                        | TRISF               | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | —     | —     | TRISF13       | TRISF12       | —     | —     | —    | TRISF8       | TRISF7       | TRISF6 | TRISF5       | TRISF4       | TRISF3       | TRISF2       | TRISF1       | TRISF0       | xxxx          |
| 6520                        | PORTF               | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | —     | —     | RF13          | RF12          | —     | —     | —    | RF8          | RF7          | RF6    | RF5          | RF4          | RF3          | RF2          | RF1          | RF0          | xxxx          |
| 6530                        | LATF                | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | —     | —     | LATF13        | LATF12        | —     | —     | —    | LATF8        | LATF7        | LATF6  | LATF5        | LATF4        | LATF3        | LATF2        | LATF1        | LATF0        | xxxx          |
| 6540                        | ODCF                | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | —     | —     | ODCF13        | ODCF12        | —     | —     | —    | ODCF8        | ODCF7        | ODCF6  | ODCF5        | ODCF4        | ODCF3        | ODCF2        | ODCF1        | ODCF0        | xxxx          |
| 6550                        | CNPUF               | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | —     | —     | CNPUF13       | CNPUF12       | —     | —     | —    | CNPUF8       | CNPUF7       | CNPUF6 | CNPUF5       | CNPUF4       | CNPDF3       | CNPUF2       | CNPUF1       | CNPUF0       | xxxx          |
| 6560                        | CNPDF               | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | —     | —     | CNPDF13       | CNPDF12       | —     | —     | —    | CNPDF8       | CNPDF7       | CNPDF6 | CNPDF5       | CNPDF4       | CNPDF3       | CNPDF2       | CNPDF1       | CNPDF0       | xxxx          |
| 6570                        | CNCONF              | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | ON    | —     | SIDL          | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
| 6580                        | CNENF               | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | —     | —     | CNIEF13       | CNIEF12       | —     | —     | —    | CNIEF8       | CNIEF7       | —      | CNIEF5       | CNIEF4       | CNIEF3       | CNIEF2       | CNIEF1       | CNIEF0       | xxxx          |
| 6590                        | CNSTATF             | 31:16     | —     | —     | —             | —             | —     | —     | —    | —            | —            | —      | —            | —            | —            | —            | —            | —            | 0000          |
|                             |                     | 15:0      | —     | —     | CN<br>STATF13 | CN<br>STATF12 | —     | —     | —    | CN<br>STATF8 | CN<br>STATF7 | —      | CN<br>STATF5 | CN<br>STATF4 | CN<br>STATF3 | CN<br>STATF2 | CN<br>STATF1 | CN<br>STATF0 | xxxx          |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

## 16.0 INPUT CAPTURE

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Input Capture”** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
  - Capture timer value on every falling edge of input at ICx pin
  - Capture timer value on every rising edge of input at ICx pin
  - Capture timer value on every edge (rising and falling)
  - Capture timer value on every edge (rising and falling), specified edge first.

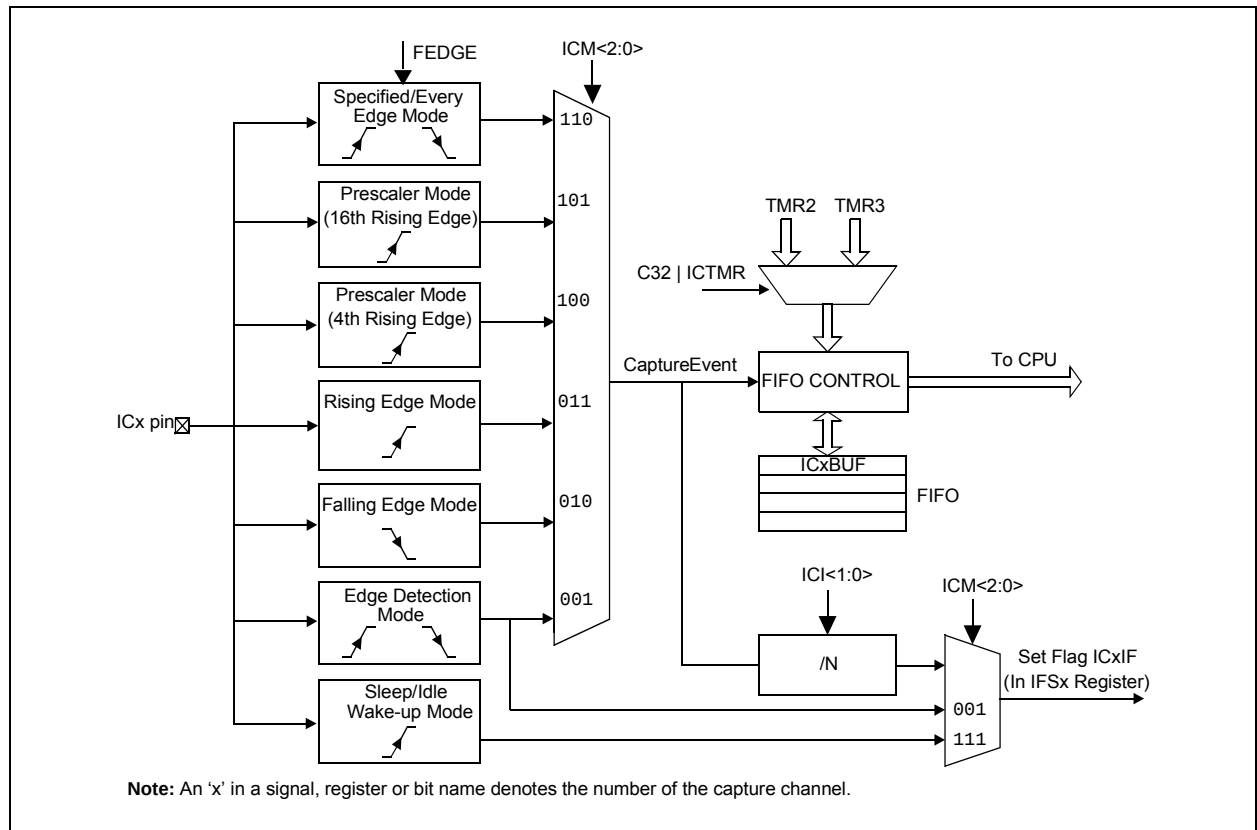
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values  
Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

**FIGURE 16-1: INPUT CAPTURE BLOCK DIAGRAM**



## REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

bit 2-0      **ICM<2:0>**: Input Capture Mode Select bits

- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode – every sixteenth rising edge
- 100 = Prescaled Capture Event mode – every fourth rising edge
- 011 = Simple Capture Event mode – every rising edge
- 010 = Simple Capture Event mode – every falling edge
- 001 = Edge Detect mode – every edge (rising and falling)
- 000 = Input Capture module is disabled

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

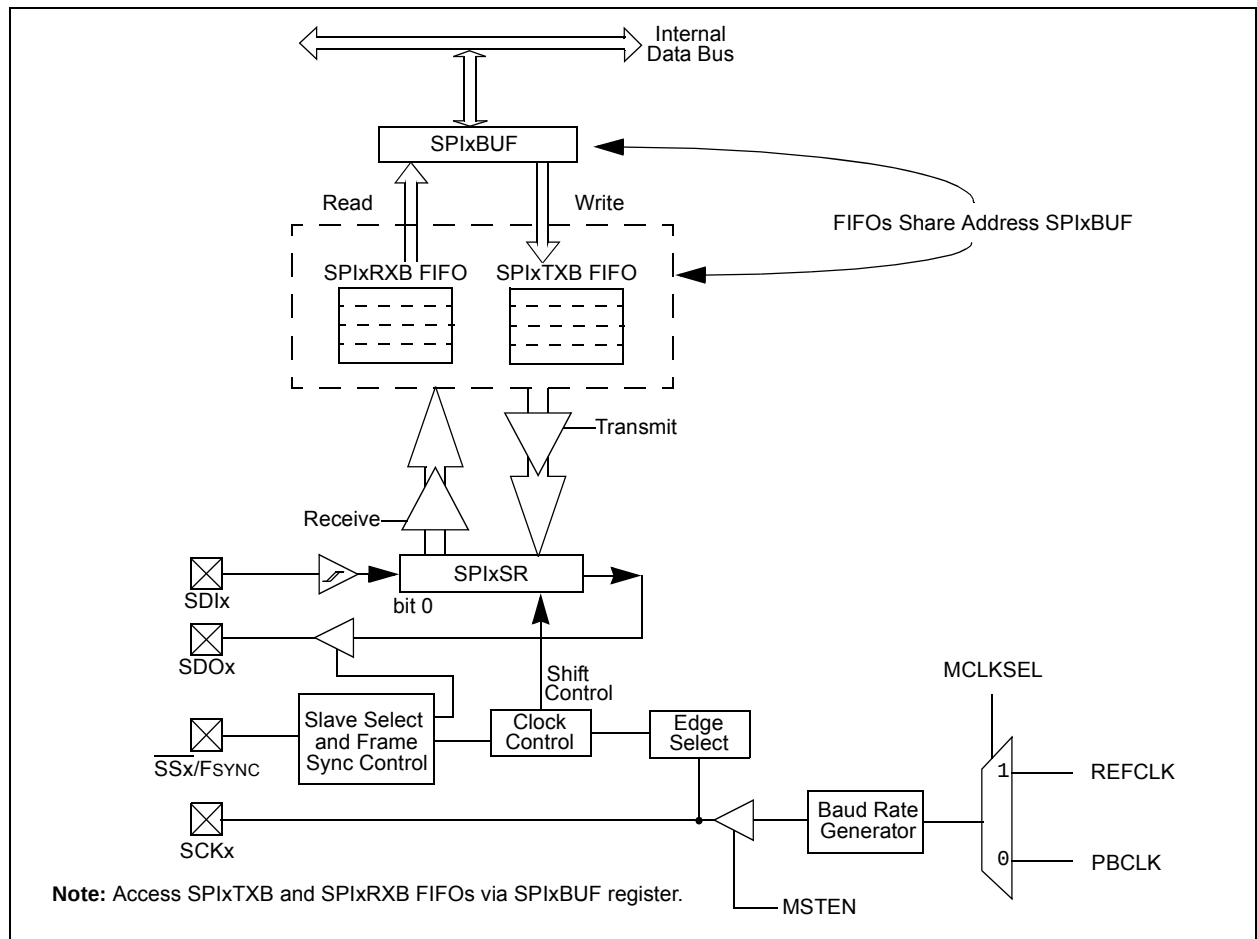
**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), etc. The PIC32 SPI module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during CPU Sleep and Idle mode
- Audio Codec Support:
  - I<sup>2</sup>S protocol
  - Left-justified
  - Right-justified
  - PCM

**FIGURE 18-1: SPI MODULE BLOCK DIAGRAM**



## 20.1 Control Registers

**TABLE 20-1: UART1 THROUGH UART5 REGISTER MAP**

| Virtual Address<br>(BF80-#) | Register Name         | Bit Range | Bits                          |       |        |       |        |       |          |        |                   |        |       |       |      |            |      |       | All Resets |
|-----------------------------|-----------------------|-----------|-------------------------------|-------|--------|-------|--------|-------|----------|--------|-------------------|--------|-------|-------|------|------------|------|-------|------------|
|                             |                       |           | 31/15                         | 30/14 | 29/13  | 28/12 | 27/11  | 26/10 | 25/9     | 24/8   | 23/7              | 22/6   | 21/5  | 20/4  | 19/3 | 18/2       | 17/1 | 16/0  |            |
| 6000                        | U1MODE <sup>(1)</sup> | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | ON                            | —     | SIDL   | IREN  | RTSMD  | —     | UEN<1:0> |        | WAKE              | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> |      | STSEL | 0000       |
| 6010                        | U1STA <sup>(1)</sup>  | 31:16     | —                             | —     | —      | —     | —      | —     | —        | ADM_EN | ADDR<7:0>         |        |       |       |      |            |      |       | 0000       |
|                             |                       | 15:0      | UTXISEL<1:0>                  |       | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF    | TRMT   | URXISEL<1:0>      |        | ADDEN | RIDLE | PERR | FERR       | OERR | URXDA | FFFF       |
| 6020                        | U1TXREG               | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | —                             | —     | —      | —     | —      | —     | —        | TX8    | Transmit Register |        |       |       |      |            |      |       | 0000       |
| 6030                        | U1RXREG               | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | —                             | —     | —      | —     | —      | —     | —        | RX8    | Receive Register  |        |       |       |      |            |      |       | 0000       |
| 6040                        | U1BRG <sup>(1)</sup>  | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | Baud Rate Generator Prescaler |       |        |       |        |       |          |        |                   |        |       |       |      |            |      |       | 0000       |
| 6200                        | U2MODE <sup>(1)</sup> | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | ON                            | —     | SIDL   | IREN  | RTSMD  | —     | UEN<1:0> |        | WAKE              | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> |      | STSEL | 0000       |
| 6210                        | U2STA <sup>(1)</sup>  | 31:16     | —                             | —     | —      | —     | —      | —     | —        | ADM_EN | ADDR<7:0>         |        |       |       |      |            |      |       | 0000       |
|                             |                       | 15:0      | UTXISEL<1:0>                  |       | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF    | TRMT   | URXISEL<1:0>      |        | ADDEN | RIDLE | PERR | FERR       | OERR | URXDA | FFFF       |
| 6220                        | U2TXREG               | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | —                             | —     | —      | —     | —      | —     | —        | TX8    | Transmit Register |        |       |       |      |            |      |       | 0000       |
| 6230                        | U2RXREG               | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | —                             | —     | —      | —     | —      | —     | —        | RX8    | Receive Register  |        |       |       |      |            |      |       | 0000       |
| 6240                        | U2BRG <sup>(1)</sup>  | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | Baud Rate Generator Prescaler |       |        |       |        |       |          |        |                   |        |       |       |      |            |      |       | 0000       |
| 6400                        | U3MODE <sup>(1)</sup> | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | ON                            | —     | SIDL   | IREN  | RTSMD  | —     | UEN<1:0> |        | WAKE              | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> |      | STSEL | 0000       |
| 6410                        | U3STA <sup>(1)</sup>  | 31:16     | —                             | —     | —      | —     | —      | —     | —        | ADM_EN | ADDR<7:0>         |        |       |       |      |            |      |       | 0000       |
|                             |                       | 15:0      | UTXISEL<1:0>                  |       | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF    | TRMT   | URXISEL<1:0>      |        | ADDEN | RIDLE | PERR | FERR       | OERR | URXDA | FFFF       |
| 6420                        | U3TXREG               | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | —                             | —     | —      | —     | —      | —     | —        | TX8    | Transmit Register |        |       |       |      |            |      |       | 0000       |
| 6430                        | U3RXREG               | 31:16     | —                             | —     | —      | —     | —      | —     | —        | —      | —                 | —      | —     | —     | —    | —          | —    | 0000  |            |
|                             |                       | 15:0      | —                             | —     | —      | —     | —      | —     | —        | RX8    | Receive Register  |        |       |       |      |            |      |       | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

# PIC32MX330/350/370/430/450/470

---

## REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>**: Alarm Repeat Counter Value bits<sup>(3)</sup>

11111111 = Alarm will trigger 256 times

.  
.  
.

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
- 2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
- 3:** This assumes a CPU read will execute in less than 32 PBCLKs.

|                                                                     |
|---------------------------------------------------------------------|
| <b>Note:</b> This register is reset only on a Power-on Reset (POR). |
|---------------------------------------------------------------------|

# PIC32MX330/350/370/430/450/470

**REGISTER 22-4: RTCDATE: RTC DATE VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x         | R/W-x         |
|           | YEAR10<3:0>    |                |                |                | YEAR01<3:0>    |                |               |               |
| 23:16     | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x         | R/W-x         |
|           | MONTH10<3:0>   |                |                |                | MONTH01<3:0>   |                |               |               |
| 15:8      | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x         | R/W-x         |
|           | DAY10<3:0>     |                |                |                | DAY01<3:0>     |                |               |               |
| 7:0       | U-0            | U-0            | U-0            | U-0            | R/W-x          | R/W-x          | R/W-x         | R/W-x         |
|           | —              | —              | —              | —              | WDAY01<3:0>    |                |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **YEAR10<3:0>**: Binary-Coded Decimal Value of Years bits, 10s place digits

bit 27-24 **YEAR01<3:0>**: Binary-Coded Decimal Value of Years bits, 1s place digit

bit 23-20 **MONTH10<3:0>**: Binary-Coded Decimal Value of Months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>**: Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>**: Binary-Coded Decimal Value of Days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>**: Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **WDAY01<3:0>**: Binary-Coded Decimal Value of Weekdays bits, 1s place digit; contains a value from 0 to 6

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).

# PIC32MX330/350/370/430/450/470

**TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

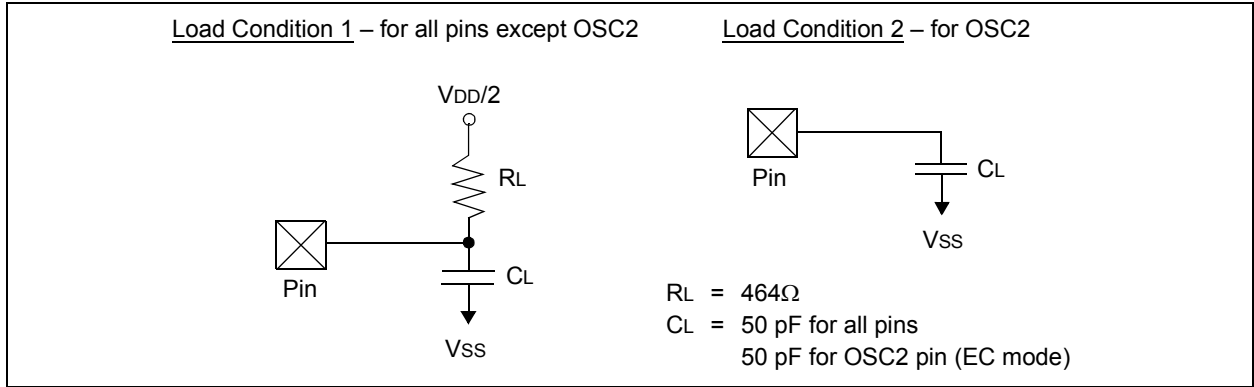
| DC CHARACTERISTICS |                  |                                                                 | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for Commercial<br>$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial<br>$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp |                     |                        |       |                                                                                                                                         |
|--------------------|------------------|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Param. No.         | Symb.            | Characteristics                                                 | Min.                                                                                                                                                                                                                                                                                                                    | Typ. <sup>(1)</sup> | Max.                   | Units | Conditions                                                                                                                              |
| DI60b              | I <sub>ICH</sub> | Input High Injection Current                                    | 0                                                                                                                                                                                                                                                                                                                       | —                   | +5 <sup>(8,9,10)</sup> | mA    | Pins with Analog functions. Exceptions: [SOSCI, SOSCO, OSC1, D+, D-] = 0 mA max.                                                        |
|                    |                  |                                                                 |                                                                                                                                                                                                                                                                                                                         |                     |                        |       | Digital 5V tolerant designated pins ( $V_{IH} < 5.5\text{V}$ ) <sup>(9)</sup> . Exceptions: [All] = 0 mA max.                           |
|                    |                  |                                                                 |                                                                                                                                                                                                                                                                                                                         |                     |                        |       | Digital non-5V tolerant designated pins. Exceptions: [N/A] = 0 mA max.                                                                  |
| DI60c              | $\Sigma I_{ICT}$ | Total Input Injection Current (sum of all I/O and control pins) | -20 <sup>(11)</sup>                                                                                                                                                                                                                                                                                                     | —                   | +20 <sup>(11)</sup>    | mA    | Absolute instantaneous sum of all $\pm$ input injection currents from all I/O pins<br>( $ I_{ICL}  +  I_{ICH} $ ) $\leq \Sigma I_{ICT}$ |

- Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** The leakage current on the  $\overline{\text{MCLR}}$  pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** This parameter is characterized, but not tested in manufacturing.
- 5:** See the “**Device Pin Tables**” section for the 5V tolerant pins.
- 6:** The  $V_{IH}$  specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic “high” internally to the PIC32 device, provided that the external load does not exceed the minimum value of  $I_{CNPV}$ . For External “input” logic inputs that require a pull-up source, to guarantee the minimum  $V_{IH}$  of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.
- 7:**  $V_{IL}$  source  $< (V_{SS} - 0.3)$ . Characterized but not tested.
- 8:**  $V_{IH}$  source  $> (V_{DD} + 0.3)$  for non-5V tolerant pins only.
- 9:** Digital 5V tolerant pins do not have an internal high side diode to  $V_{DD}$ , and therefore, cannot tolerate any “positive” input injection current.
- 10:** Injection currents  $> |0|$  can affect the ADC results by approximately 4 to 6 counts (i.e.,  $V_{IH}$  Source  $> (V_{DD} + 0.3)$  or  $V_{IL}$  source  $< (V_{SS} - 0.3)$ ).
- 11:** Any number and/or combination of I/O pins not excluded under  $I_{ICL}$  or  $I_{ICH}$  conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**,  $I_{ICL} = ((V_{SS} - 0.3) - V_{IL} \text{ source}) / R_S$ . If **Note 8**,  $I_{ICH} = ((I_{ICH} \text{ source} - (V_{DD} + 0.3)) / R_S)$ .  $R_S$  = Resistance between input source voltage and device pin. If  $(V_{SS} - 0.3) \leq V_{SOURCE} \leq (V_{DD} + 0.3)$ , injection current = 0.

## 31.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX330/350/370/430/450/470 AC characteristics and timing parameters.

**FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

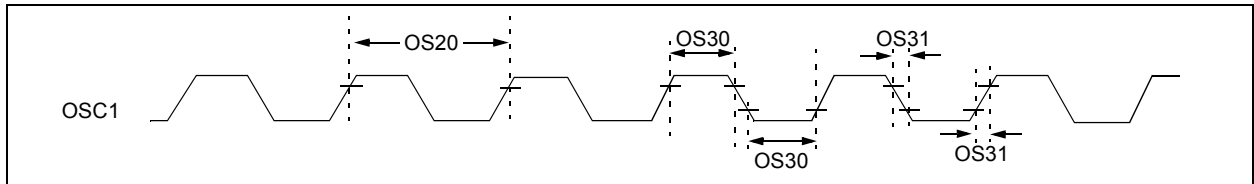


**TABLE 31-17: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

| AC CHARACTERISTICS |        |                       | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for Commercial<br>$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for Industrial<br>$-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ for V-temp |                        |      |       |                                                                   |
|--------------------|--------|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------|-------|-------------------------------------------------------------------|
| Param. No.         | Symbol | Characteristics       | Min.                                                                                                                                                                                                                                                                                                        | Typical <sup>(1)</sup> | Max. | Units | Conditions                                                        |
| DO50               | Cosco  | OSC2 pin              | —                                                                                                                                                                                                                                                                                                           | —                      | 15   | pF    | In XT and HS modes when an external crystal is used to drive OSC1 |
| DO56               | Cio    | All I/O pins and OSC2 | —                                                                                                                                                                                                                                                                                                           | —                      | 50   | pF    | EC mode                                                           |
| DO58               | Cb     | SCLx, SDAx            | —                                                                                                                                                                                                                                                                                                           | —                      | 400  | pF    | In I <sup>2</sup> C mode                                          |

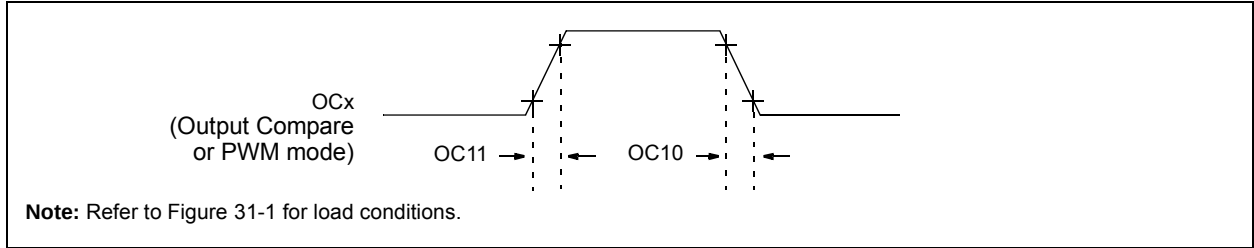
**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 31-2: EXTERNAL CLOCK TIMING**



# PIC32MX330/350/370/430/450/470

**FIGURE 31-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS**



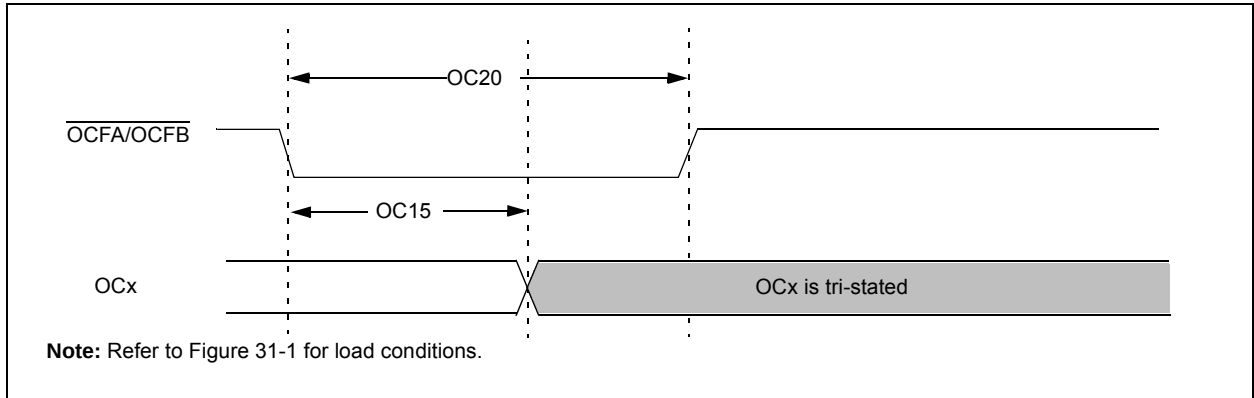
**TABLE 31-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS |        |                                | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |                        |      |       |                    |
|--------------------|--------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------|-------|--------------------|
| Param. No.         | Symbol | Characteristics <sup>(1)</sup> | Min.                                                                                                                                                                                                     | Typical <sup>(2)</sup> | Max. | Units | Conditions         |
| OC10               | TccF   | OCx Output Fall Time           | —                                                                                                                                                                                                        | —                      | —    | ns    | See parameter DO32 |
| OC11               | TccR   | OCx Output Rise Time           | —                                                                                                                                                                                                        | —                      | —    | ns    | See parameter DO31 |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 31-9: OCx/PWM MODULE TIMING CHARACTERISTICS**



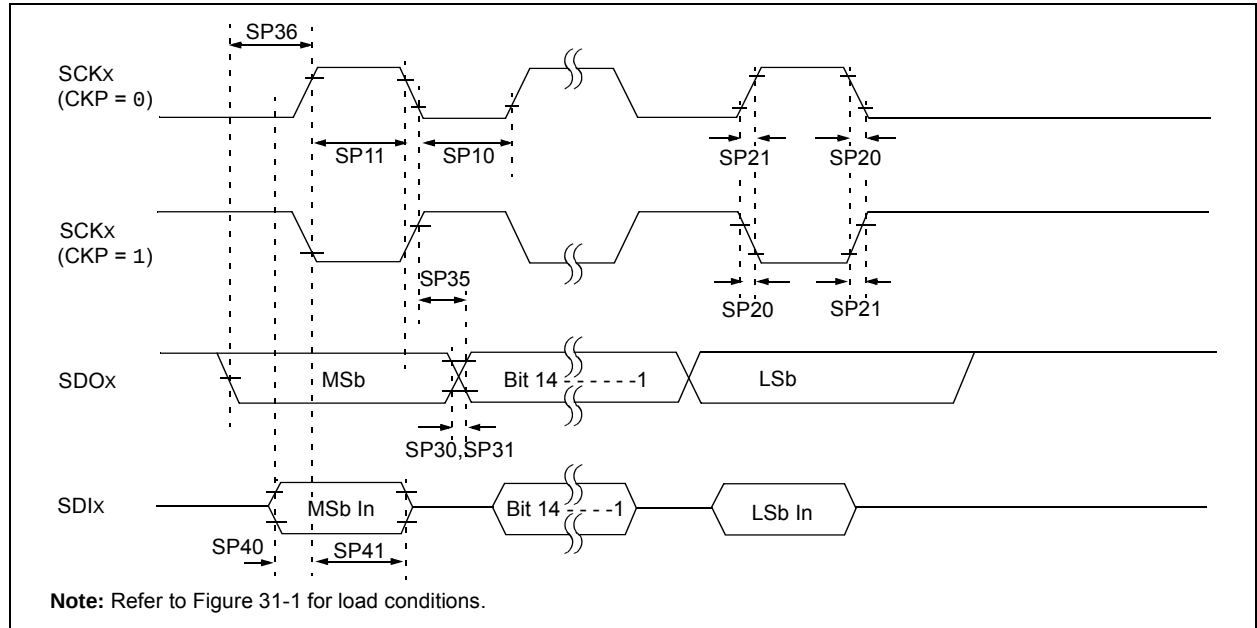
**TABLE 31-28: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS**

| AC CHARACTERISTICS |        |                                | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |                        |     |       |            |
|--------------------|--------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-----|-------|------------|
| Param No.          | Symbol | Characteristics <sup>(1)</sup> | Min                                                                                                                                                                                                      | Typical <sup>(2)</sup> | Max | Units | Conditions |
| OC15               | TfD    | Fault Input to PWM I/O Change  | —                                                                                                                                                                                                        | —                      | 50  | ns    | —          |
| OC20               | TFLT   | Fault Input Pulse Width        | 50                                                                                                                                                                                                       | —                      | —   | ns    | —          |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 31-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS**



**TABLE 31-30: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS |                       |                                            |        | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |      |       |                    |
|--------------------|-----------------------|--------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|--------------------|
| Param. No.         | Symbol                | Characteristics <sup>(1)</sup>             | Min.   | Typ. <sup>(2)</sup>                                                                                                                                                                                      | Max. | Units | Conditions         |
| SP10               | TsCL                  | SCKx Output Low Time <b>(Note 3)</b>       | TsCK/2 | —                                                                                                                                                                                                        | —    | ns    | —                  |
| SP11               | TsCH                  | SCKx Output High Time <b>(Note 3)</b>      | TsCK/2 | —                                                                                                                                                                                                        | —    | ns    | —                  |
| SP20               | TsCF                  | SCKx Output Fall Time <b>(Note 4)</b>      | —      | —                                                                                                                                                                                                        | —    | ns    | See parameter DO32 |
| SP21               | TsCR                  | SCKx Output Rise Time <b>(Note 4)</b>      | —      | —                                                                                                                                                                                                        | —    | ns    | See parameter DO32 |
| SP30               | TDoF                  | SDOx Data Output Fall Time <b>(Note 4)</b> | —      | —                                                                                                                                                                                                        | —    | ns    | See parameter DO32 |
| SP31               | TDoR                  | SDOx Data Output Rise Time <b>(Note 4)</b> | —      | —                                                                                                                                                                                                        | —    | ns    | See parameter DO31 |
| SP35               | TsCH2DoV,<br>TsCL2DoV | SDOx Data Output Valid after SCKx Edge     | —      | —                                                                                                                                                                                                        | 15   | ns    | VDD > 2.7V         |
|                    |                       |                                            | —      | —                                                                                                                                                                                                        | 20   | ns    | VDD < 2.7V         |
| SP36               | TDoV2sc,<br>TDoV2scL  | SDOx Data Output Setup to First SCKx Edge  | 15     | —                                                                                                                                                                                                        | —    | ns    | —                  |
| SP40               | TDiV2sch,<br>TDiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 15     | —                                                                                                                                                                                                        | —    | ns    | VDD > 2.7V         |
|                    |                       |                                            | 20     | —                                                                                                                                                                                                        | —    | ns    | VDD < 2.7V         |
| SP41               | TsCH2DiL,<br>TsCL2DiL | Hold Time of SDIx Data Input to SCKx Edge  | 15     | —                                                                                                                                                                                                        | —    | ns    | VDD > 2.7V         |
|                    |                       |                                            | 20     | —                                                                                                                                                                                                        | —    | ns    | VDD < 2.7V         |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**Note 2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**Note 3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

**Note 4:** Assumes 50 pF load on all SPIx pins.

# PIC32MX330/350/370/430/450/470

**TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

| AC CHARACTERISTICS |         |                            |                        | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |      |       |                                                       |
|--------------------|---------|----------------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|-------------------------------------------------------|
| Param. No.         | Symbol  | Characteristics            |                        | Min. <sup>(1)</sup>                                                                                                                                                                                      | Max. | Units | Conditions                                            |
| IM10               | TLO:SCL | Clock Low Time             | 100 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | —                                                     |
|                    |         |                            | 400 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | —                                                     |
|                    |         |                            | 1 MHz mode<br>(Note 2) | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | —                                                     |
| IM11               | THI:SCL | Clock High Time            | 100 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | —                                                     |
|                    |         |                            | 400 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | —                                                     |
|                    |         |                            | 1 MHz mode<br>(Note 2) | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | —                                                     |
| IM20               | TF:SCL  | SDAx and SCLx Fall Time    | 100 kHz mode           | —                                                                                                                                                                                                        | 300  | ns    | Cb is specified to be from 10 to 400 pF               |
|                    |         |                            | 400 kHz mode           | 20 + 0.1 Cb                                                                                                                                                                                              | 300  | ns    |                                                       |
|                    |         |                            | 1 MHz mode<br>(Note 2) | —                                                                                                                                                                                                        | 100  | ns    |                                                       |
| IM21               | Tr:SCL  | SDAx and SCLx Rise Time    | 100 kHz mode           | —                                                                                                                                                                                                        | 1000 | ns    | Cb is specified to be from 10 to 400 pF               |
|                    |         |                            | 400 kHz mode           | 20 + 0.1 Cb                                                                                                                                                                                              | 300  | ns    |                                                       |
|                    |         |                            | 1 MHz mode<br>(Note 2) | —                                                                                                                                                                                                        | 300  | ns    |                                                       |
| IM25               | TSU:DAT | Data Input Setup Time      | 100 kHz mode           | 250                                                                                                                                                                                                      | —    | ns    | —                                                     |
|                    |         |                            | 400 kHz mode           | 100                                                                                                                                                                                                      | —    | ns    |                                                       |
|                    |         |                            | 1 MHz mode<br>(Note 2) | 100                                                                                                                                                                                                      | —    | ns    |                                                       |
| IM26               | THD:DAT | Data Input Hold Time       | 100 kHz mode           | 0                                                                                                                                                                                                        | —    | μs    | —                                                     |
|                    |         |                            | 400 kHz mode           | 0                                                                                                                                                                                                        | 0.9  | μs    |                                                       |
|                    |         |                            | 1 MHz mode<br>(Note 2) | 0                                                                                                                                                                                                        | 0.3  | μs    |                                                       |
| IM30               | TSU:STA | Start Condition Setup Time | 100 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | Only relevant for Repeated Start condition            |
|                    |         |                            | 400 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    |                                                       |
|                    |         |                            | 1 MHz mode<br>(Note 2) | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    |                                                       |
| IM31               | THD:STA | Start Condition Hold Time  | 100 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | After this period, the first clock pulse is generated |
|                    |         |                            | 400 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    |                                                       |
|                    |         |                            | 1 MHz mode<br>(Note 2) | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    |                                                       |
| IM33               | TSU:STO | Stop Condition Setup Time  | 100 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    | —                                                     |
|                    |         |                            | 400 kHz mode           | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    |                                                       |
|                    |         |                            | 1 MHz mode<br>(Note 2) | TPB * (BRG + 2)                                                                                                                                                                                          | —    | μs    |                                                       |

**Note 1:** BRG is the value of the I<sup>2</sup>C Baud Rate Generator.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

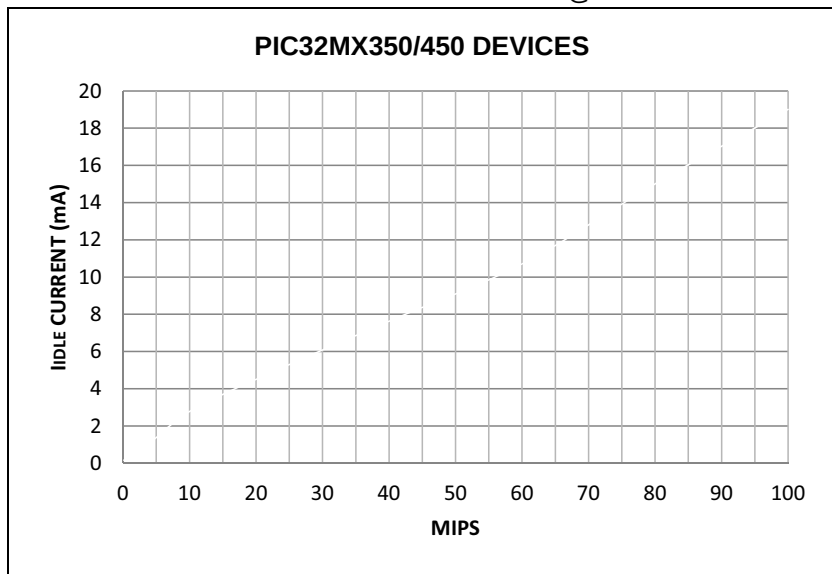
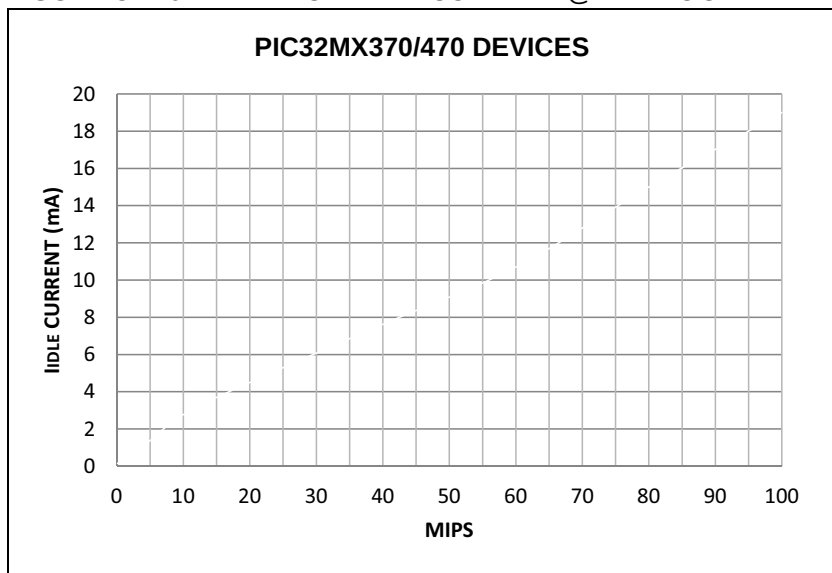
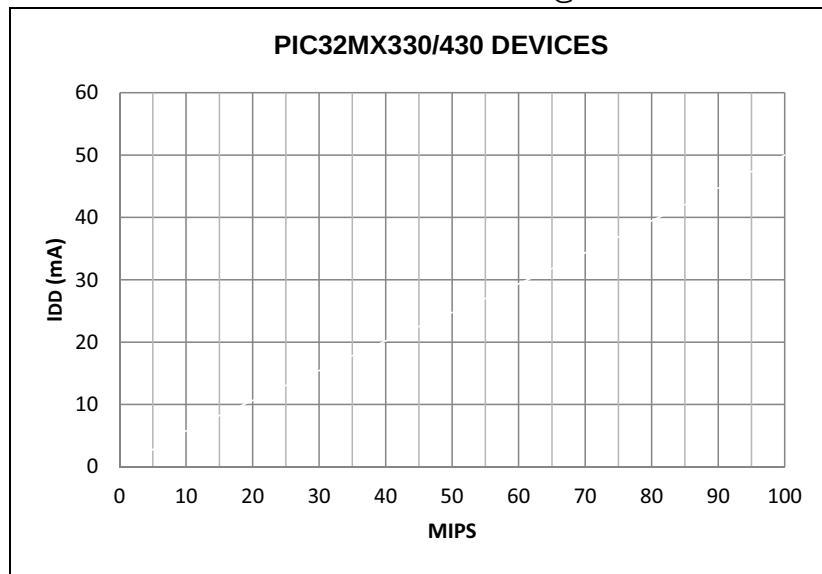
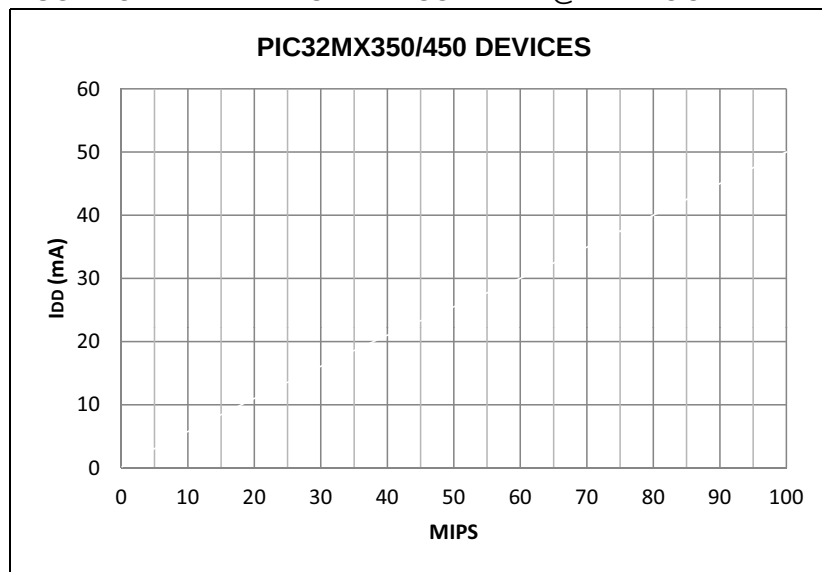
**3:** The typical value for this parameter is 104 ns.

# PIC32MX330/350/370/430/450/470

**TABLE 31-41: OTG ELECTRICAL SPECIFICATIONS**

| AC CHARACTERISTICS |         |                                   | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |      |      |       |                                                                          |
|--------------------|---------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------|--------------------------------------------------------------------------|
| Param. No.         | Symbol  | Characteristics <sup>(1)</sup>    | Min.                                                                                                                                                                                                     | Typ. | Max. | Units | Conditions                                                               |
| USB313             | VUSB3V3 | USB Voltage                       | 3.0                                                                                                                                                                                                      | —    | 3.6  | V     | Voltage on VUSB3V3 must be in this range for proper USB operation        |
| USB315             | VILUSB  | Input Low Voltage for USB Buffer  | —                                                                                                                                                                                                        | —    | 0.8  | V     | —                                                                        |
| USB316             | VIHUSB  | Input High Voltage for USB Buffer | 2.0                                                                                                                                                                                                      | —    | —    | V     | —                                                                        |
| USB318             | VDIFS   | Differential Input Sensitivity    | —                                                                                                                                                                                                        | —    | 0.2  | V     | The difference between D+ and D- must exceed this value while VCM is met |
| USB319             | VCM     | Differential Common Mode Range    | 0.8                                                                                                                                                                                                      | —    | 2.5  | V     | —                                                                        |
| USB320             | ZOUT    | Driver Output Impedance           | 28.0                                                                                                                                                                                                     | —    | 44.0 | Ω     | —                                                                        |
| USB321             | VOL     | Voltage Output Low                | 0.0                                                                                                                                                                                                      | —    | 0.3  | V     | 1.425 kΩ load connected to VUSB3V3                                       |
| USB322             | VOH     | Voltage Output High               | 2.8                                                                                                                                                                                                      | —    | 3.6  | V     | 14.25 kΩ load connected to ground                                        |

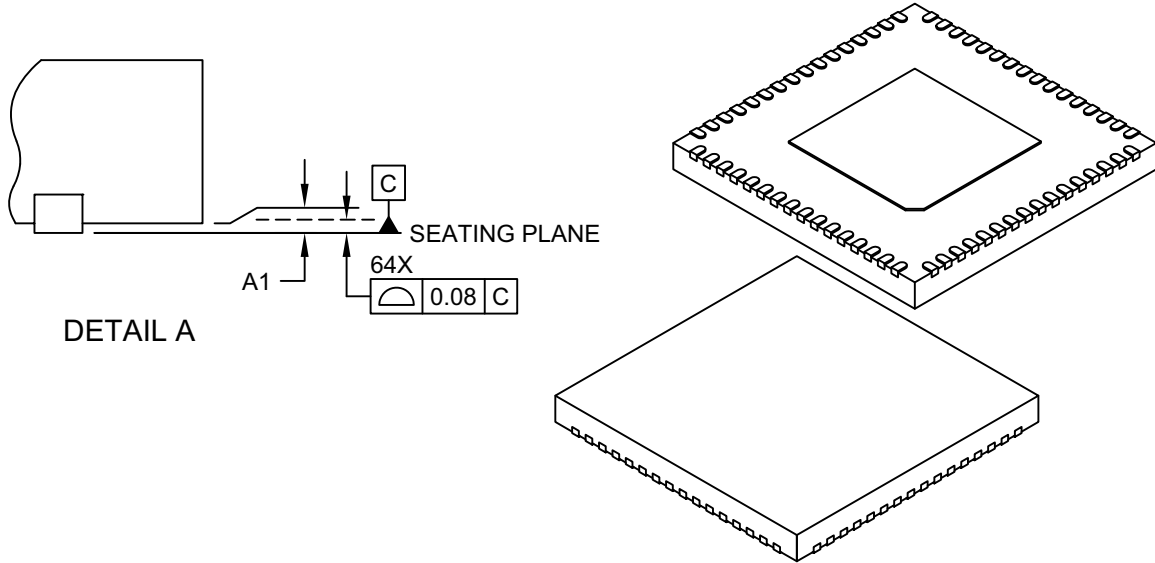
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-9: TYPICAL  $I_{IDLE}$  CURRENT @  $V_{DD} = 3.3V$** **FIGURE 32-10: TYPICAL  $I_{IDLE}$  CURRENT @  $V_{DD} = 3.3V$** **FIGURE 32-11: TYPICAL  $I_{DD}$  CURRENT @  $V_{DD} = 3.3V$** **FIGURE 32-12: TYPICAL  $I_{DD}$  CURRENT @  $V_{DD} = 3.3V$** 

# PIC32MX330/350/370/430/450/470

## 64-Terminal Plastic Quad Flat Pack, No Lead (RG) 9x9x0.9 mm Body [QFN] Saw Singulated

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



|                         |    | Units     | MILLIMETERS |      |     |
|-------------------------|----|-----------|-------------|------|-----|
| Dimension Limits        |    |           | MIN         | NOM  | MAX |
| Number of Terminals     | N  | 64        |             |      |     |
| Pitch                   | e  | 0.50 BSC  |             |      |     |
| Overall Height          | A  | 0.80      | 0.85        | 0.90 |     |
| Standoff                | A1 | 0.00      | 0.02        | 0.05 |     |
| Standoff                | A3 | 0.20 REF  |             |      |     |
| Overall Width           | E  | 9.00 BSC  |             |      |     |
| Exposed Pad Width       | E2 | 4.60      | 4.70        | 4.80 |     |
| Overall Length          | D  | 9.00 BSC  |             |      |     |
| Exposed Pad Length      | D2 | 4.60      | 4.70        | 4.80 |     |
| Terminal Width          | b  | 0.15      | 0.20        | 0.25 |     |
| Terminal Length         | L  | 0.30      | 0.40        | 0.50 |     |
| Terminal-to-Exposed-Pad | K  | 1.755 REF |             |      |     |

### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-260A Sheet 2 of 2