What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	49
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx470f512h-120-mr

PIC32MX330/350/370/430/450/470

TABLE 1: PIC32MX330/350/370/430/450/470 CONTROLLER FAMILY FEATURES

Device	Pins	Packages	Program Memory (KB)[1]	Data Memory (KB)	Remappable Pins	Timers/Capture/Compare[2]	UART	SPI/I²S	External Interrupts[3]	10-bit 1 Msps ADC (Channels)	Analog Comparators	USB On-The-Go (OTG)	CTMU	I²C	PMP	RTCC	DMA Channels (Programmable/Dedicated)	I/O Pins	JTAG	Trace
PIC32MX330F064H	64	QFN, TQFP	64+12	16	37	5/5/5	4	2/2	5	28	2	N	Y	2	Y	Y	4/0	53	Y	N
PIC32MX330F064L	100 / 124	TQFP / VTLA	64+12	16	54	5/5/5	5	2/2	5	28	2	N	Y	2	Y	Y	4/0	85	Y	Y
PIC32MX350F128H	64	QFN, TQFP	128+12	32	37	5/5/5	4	2/2	5	28	2	N	Y	2	Y	Y	4/0	53	Y	N
PIC32MX350F128L	100 / 124	TQFP / VTLA	128+12	32	54	5/5/5	5	2/2	5	28	2	N	Y	2	Y	Y	4/0	85	Y	Y
PIC32MX350F256H	64	QFN, TQFP	256+12	64	37	5/5/5	4	2/2	5	28	2	N	Y	2	Y	Y	4/0	53	Y	N
PIC32MX350F256L	100 / 124	TQFP / VTLA	256+12	64	54	5/5/5	5	2/2	5	28	2	N	Y	2	Y	Y	4/0	85	Y	Y
PIC32MX370F512H	64	QFN, TQFP	512+12	128	37	5/5/5	4	2/2	5	28	2	N	Y	2	Y	Y	4/0	53	Y	N
PIC32MX370F512L	100 / 124	TQFP / VTLA	512+12	128	54	5/5/5	5	2/2	5	28	2	N	Y	2	Y	Y	4/0	85	Y	Y
PIC32MX430F064H	64	QFN, TQFP	64+12	16	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX430F064L	100 / 124	TQFP / VTLA	64+12	16	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
PIC32MX450F128H	64	QFN, TQFP	128+12	32	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX450F128HB (see **Note 4**)	64	QFN, TQFP	128+12	32	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX450F128L	100 / 124	TQFP / VTLA	128+12	32	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
PIC32MX450F256H	64	QFN, TQFP	256+12	64	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX450F256L	100 / 124	TQFP / VTLA	256+12	64	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
PIC32MX470F512H	64	QFN, TQFP	512+12	128	34	5/5/5	4	2/2	5	28	2	Y	Y	2	Y	Y	4/2	49	Y	N
PIC32MX470F512L	100 / 124	TQFP / VTLA	512+12	128	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y
PIC32MX470F512LB (see **Note 4**)	100 / 124	TQFP / VTLA	512+12	128	51	5/5/5	5	2/2	5	28	2	Y	Y	2	Y	Y	4/2	81	Y	Y

Note 1: All devices feature 12 KB of Boot Flash memory.
2: Four out of five timers are remappable.
3: Four out of five external interrupts are remappable.
4: This PIC32 device is targeted to specific audio software packages that are tracked for licensing royalty purposes. All peripherals and electrical characteristics are identical to their corresponding base part numbers

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PIC32MX330/350/370/430/450/470

3.2 Architecture Overview

The MIPS32® M4K® processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e® Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32® M4K® processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32® M4K® processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.
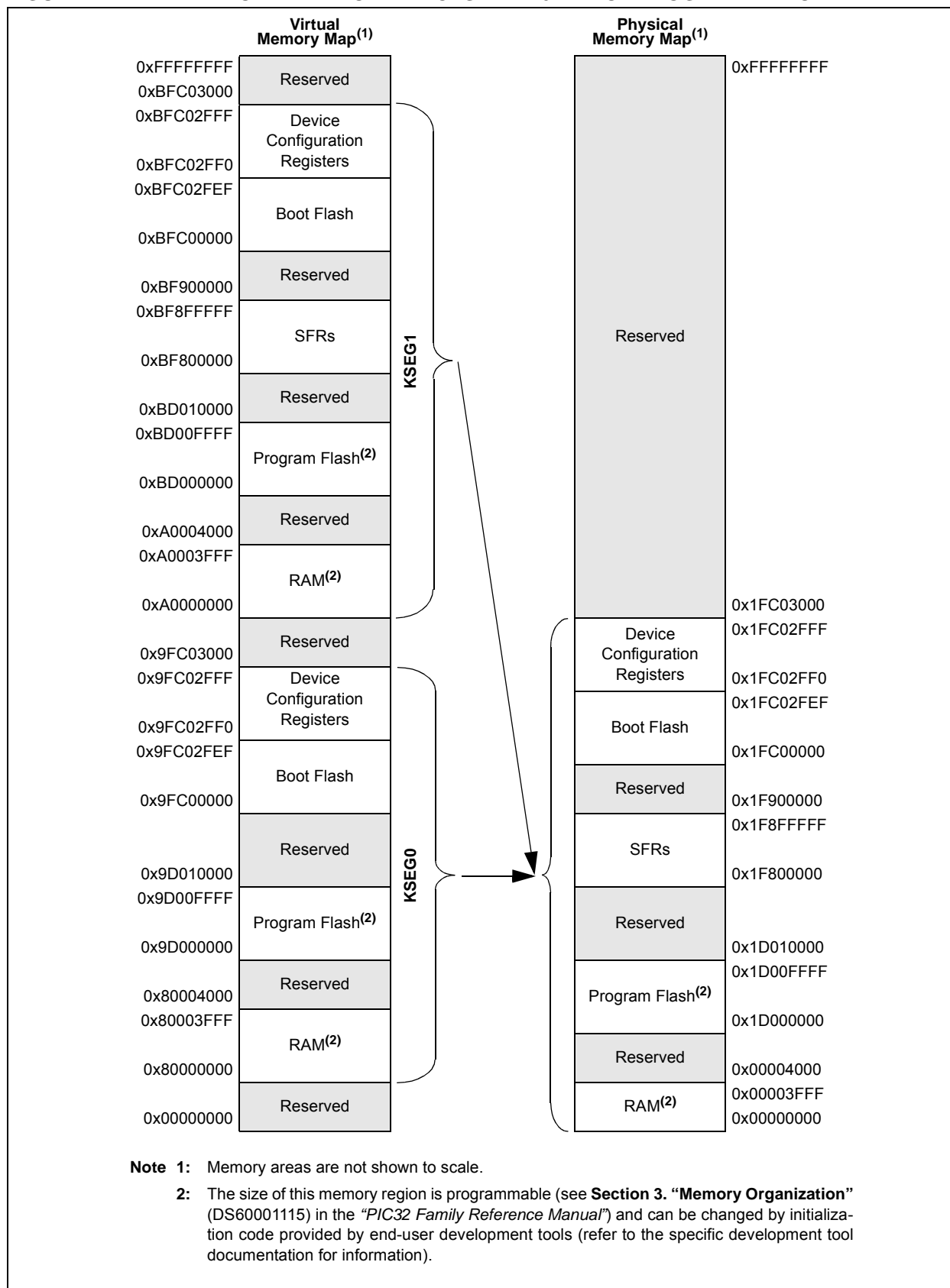
Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS32® M4K® PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/ DIVIDE UNIT LATENCIES AND REPEAT RATES

Op code	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU, MSUB/MSUBU	16 bits	1	1
	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

FIGURE 4-1: **MEMORY MAP FOR DEVICES WITH 64 KB OF PROGRAM MEMORY**

Virtual Memory Map[1]

Address	Region
0xFFFFFFFF	Reserved
0xBFC03000	
0xBFC02FFF	Device Configuration Registers
0xBFC02FF0	
0xBFC02FEF	Boot Flash
0xBFC00000	
0xBF900000	Reserved
0xBF8FFFFF	SFRs
0xBF800000	
0xBD010000	Reserved
0xBD00FFFF	Program Flash[2]
0xBD000000	
0xA0004000	Reserved
0xA0003FFF	RAM[2]
0xA0000000	
0x9FC03000	Reserved
0x9FC02FFF	Device Configuration Registers
0x9FC02FF0	
0x9FC02FEF	Boot Flash
0x9FC00000	
0x9D010000	Reserved
0x9D00FFFF	Program Flash[2]
0x9D000000	
0x80004000	Reserved
0x80003FFF	RAM[2]
0x80000000	
0x00000000	Reserved

KSEG1, KSEG0

Physical Memory Map[1]

Address	Region
0xFFFFFFFF	Reserved
0x1FC03000	Device Configuration Registers
0x1FC02FFF	
0x1FC02FF0	
0x1FC02FEF	Boot Flash
0x1FC00000	
0x1F900000	Reserved
0x1F8FFFFF	SFRs
0x1F800000	
0x1D010000	Reserved
0x1D00FFFF	Program Flash[2]
0x1D000000	
0x00004000	Reserved
0x00003FFF	RAM[2]
0x00000000	

Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

PIC32MX330/350/370/430/450/470

7.0 INTERRUPT CONTROLLER

> **Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX330/350/370/430/450/470 devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX330/350/370/430/450/470 interrupt module includes the following features:

- Up to 76 interrupt sources
- Up to 46 interrupt vectors
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Dedicated shadow set configurable for any priority level (see the FSRSSEL<2:0> bits (DEVCFG3<18:16>) in **28.0 "Special Features"** for more information)
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

FIGURE 7-1: INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM
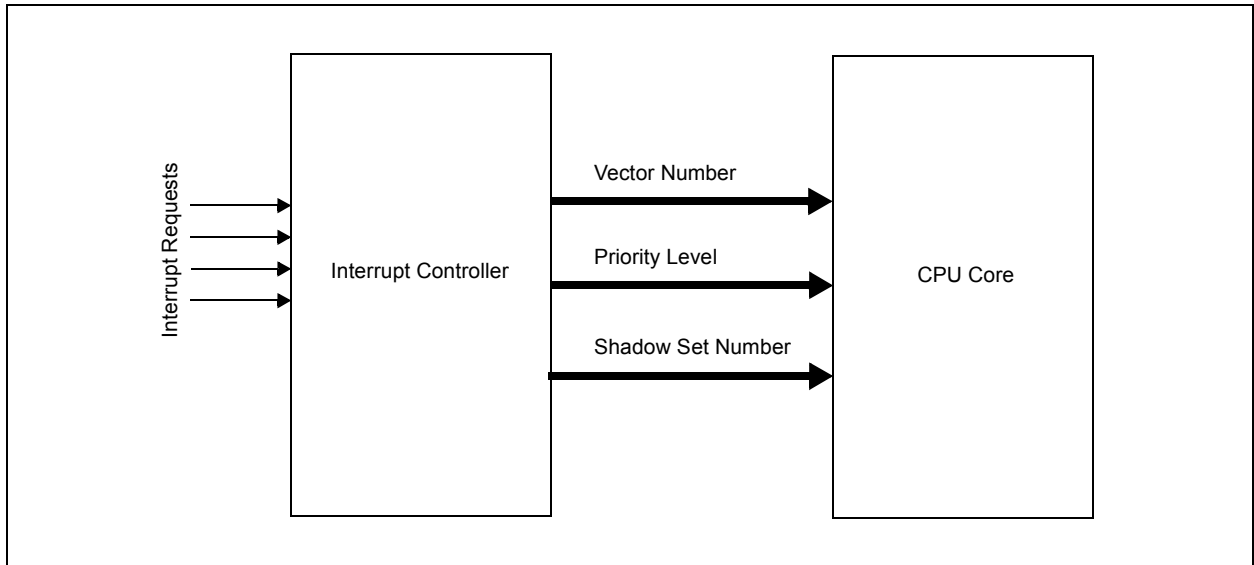
REGISTER 11-11:   U1CON: USB CONTROL REGISTER (CONTINUED)

bit 1   **PPBRST:** Ping-Pong Buffers Reset bit

1 = Reset all Even/Odd buffer pointers to the EVEN BD banks
0 = Even/Odd buffer pointers not being Reset

bit 0   **USBEN:** USB Module Enable bit[4]

1 = USB module and supporting circuitry is enabled
0 = USB module and supporting circuitry is disabled

SOFEN: SOF Enable bit[5]

1 = SOF token sent every 1 ms
0 = SOF token is disabled

Note 1:   Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).

2:   All host control logic is reset any time that the value of this bit is toggled.

3:   Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.

4:   Device mode.

5:   Host mode.

REGISTER 12-1: [*pin name*]R: PERIPHERAL PIN SELECT INPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	[*pin name*]R<3:0>			

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-4   **Unimplemented:** Read as '0'

bit 3-0   **[*pin name*]R<3:0>:** Peripheral Pin Select Input bits
Where [*pin name*] refers to the pins that are used to configure peripheral input mapping. See Table 12-1 for input pin selection values.

> **Note:**   Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

REGISTER 12-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RPnR<3:0>			

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-4   **Unimplemented:** Read as '0'

bit 3-0   **RPnR<3:0>:** Peripheral Pin Select Output bits
See Table 12-2 for output pin selection values.

> **Note:**   Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

14.2 Control Register

TABLE 14-1: TIMER2 THROUGH TIMER5 REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0800	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	—	TCKPS<2:0>		T32	—	TCS	—	0000
0810	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0820	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0A00	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	—	TCKPS<2:0>		—	—	TCS	—	0000
0A10	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0A20	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0C00	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	—	TCKPS<2:0>		T32	—	TCS	—	0000
0C10	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0C20	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0E00	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	—	TCKPS<2:0>		—	—	TCS	—	0000
0E10	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0E20	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

NOTES:

REGISTER 17-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON[1]	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT[2]	OCTSEL	OCM<2:0>		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit[1]

    1 = Output Compare peripheral is enabled
    0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

    1 = Discontinue operation when CPU enters Idle mode
    0 = Continue operation in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit

    1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisions to the 32-bit timer source
    0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit[2]

    1 = PWM Fault condition has occurred (cleared in HW only)
    0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit

    1 = Timer3 is the clock source for this Output Compare module
    0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits

    111 = PWM mode on OCx; Fault pin is enabled
    110 = PWM mode on OCx; Fault pin is disabled
    101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
    100 = Initialize OCx pin low; generate single output pulse on OCx pin
    011 = Compare event toggles OCx pin
    010 = Initialize OCx pin high; compare event forces OCx pin low
    001 = Initialize OCx pin low; compare event forces OCx pin high
    000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
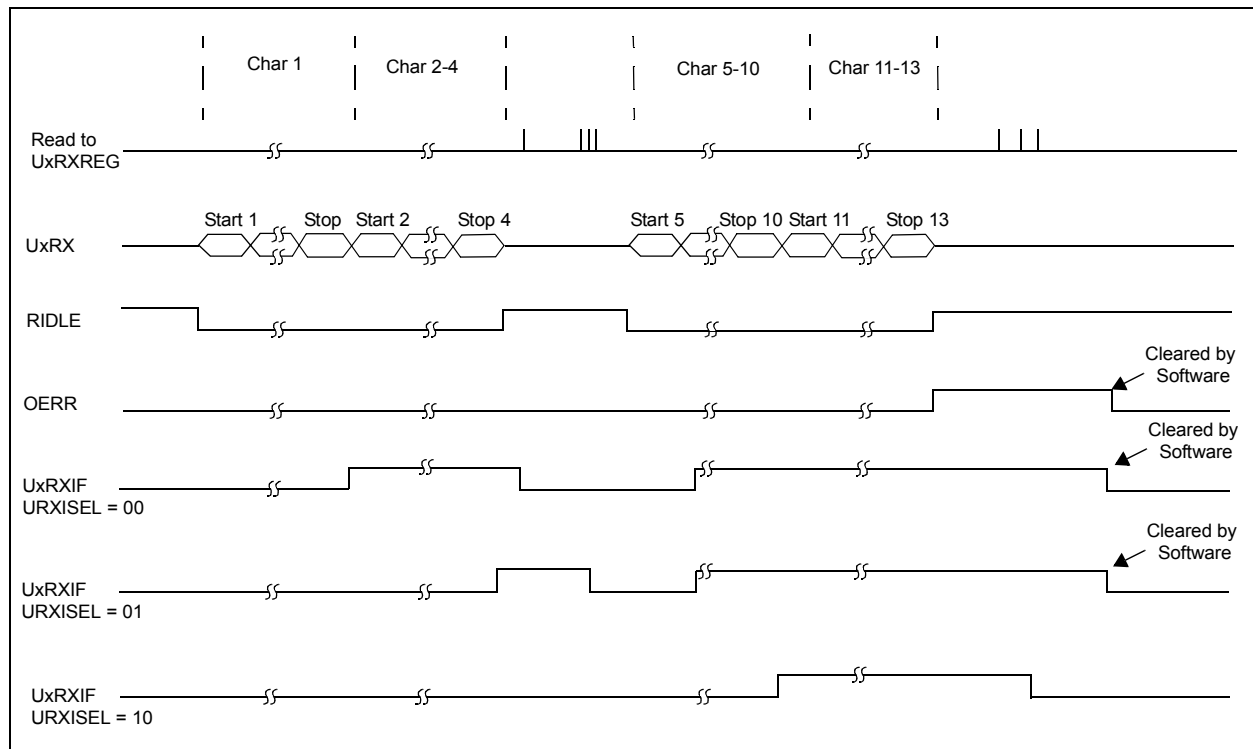
    2: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.
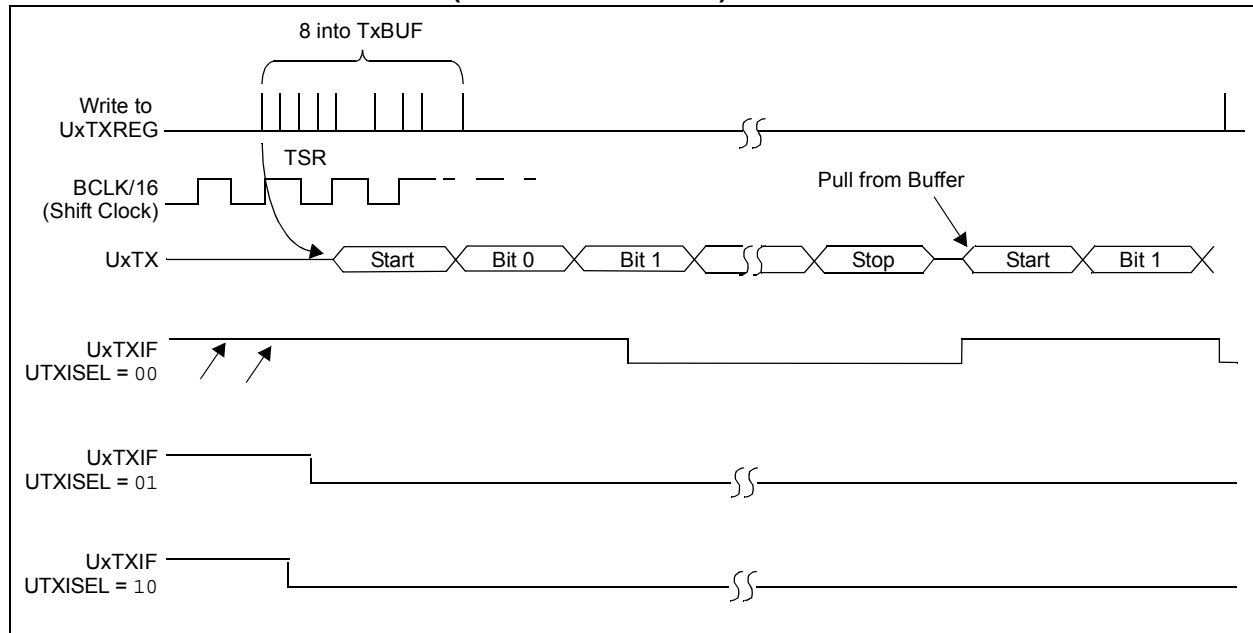
20.2   Timing Diagrams

Figure 20-2 and Figure 20-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 20-2:   UART RECEPTION

FIGURE 20-3:   TRANSMISSION (8-BIT OR 9-BIT DATA)

REGISTER 23-1:   AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 4   **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)
> 1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
> 0 = Normal operation, buffer contents will be overwritten by the next conversion sequence

bit 3   **Unimplemented:** Read as '0'

bit 2   **ASAM:** ADC Sample Auto-Start bit
> 1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.
> 0 = Sampling begins when SAMP bit is set

bit 1   **SAMP:** ADC Sample Enable bit[2]
> 1 = The ADC sample and hold amplifier is sampling
> 0 = The ADC sample/hold amplifier is holding
> When ASAM = 0, writing '1' to this bit starts sampling.
> When SSRC = 000, writing '0' to this bit will end sampling and start conversion.

bit 0   **DONE:** Analog-to-Digital Conversion Status bit[3]
> 1 = Analog-to-digital conversion is done
> 0 = Analog-to-digital conversion is not done or has not started
> Clearing this bit will not affect any operation in progress.

Note 1:   When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2:   If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ 0, this bit is automatically cleared by hardware to end sampling and start conversion.

3:   This bit is automatically set by hardware when ADC is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	C2OUT	C1OUT

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-14   **Unimplemented:** Read as '0'

bit 13   **SIDL:** Stop in IDLE Control bit

1 = All Comparator modules are disabled in IDLE mode
0 = All Comparator modules continue to operate in the IDLE mode

bit 12-2   **Unimplemented:** Read as '0'

bit 1   **C2OUT:** Comparator Output bit

1 = Output of Comparator 2 is a '1'
0 = Output of Comparator 2 is a '0'

bit 0   **C1OUT:** Comparator Output bit

1 = Output of Comparator 1 is a '1'
0 = Output of Comparator 1 is a '0'

REGISTER 26-1:   CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 24   **EDG1STAT:** Edge 1 Status bit

Indicates the status of Edge 1 and can be written to control edge source

1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 23   **EDG2MOD:** Edge 2 Edge Sampling Select bit

1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 22   **EDG2POL:** Edge 2 Polarity Select bit

1 = Edge 2 programmed for a positive edge response
0 = Edge 2 programmed for a negative edge response

bit 21-18 **EDG2SEL<3:0>:** Edge 2 Source Select bits

1111 = Reserved
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = PBCLK clock is selected
1011 = IC3 Capture Event is selected
1010 = IC2 Capture Event is selected
1001 = IC1 Capture Event is selected
1000 = CTED13 pin is selected
0111 = CTED12 pin is selected
0110 = CTED11 pin is selected
0101 = CTED10 pin is selected
0100 = CTED9 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 17-16 **Unimplemented:** Read as '0'

bit 15   **ON:** ON Enable bit

1 = Module is enabled
0 = Module is disabled

bit 14   **Unimplemented:** Read as '0'

bit 13   **CTMUSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12   **TGEN:** Time Generation Enable bit[1]

1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11   **EDGEN:** Edge Enable bit

1 = Edges are not blocked
0 = Edges are blocked

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 31-42) in **Section 31.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

28.0 SPECIAL FEATURES

> **Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129), which are available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MX330/350/370/430/450/470 family of devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

28.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- CFGCON: Configuration Control Register

In addition, the DEVID register (Register 28-6) provides device and revision information.

PIC32MX330/350/370/430/450/470

TABLE 31-5: DC CHARACTERISTICS: OPERATING CURRENT (I$_{DD}$)

DC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $0°C \leq T_A \leq +70°C$ for Commercial $-40°C \leq T_A \leq +85°C$ for Industrial $-40°C \leq T_A \leq +105°C$ for V-temp	
Parameter No.	Typical[3]	Maximum	Units	Conditions	
Operating Current (I$_{DD}$)[1,2]					
DC20	2.5	4	mA	4 MHz	
DC21	6	9	mA	10 MHz **(Note 4)**	
DC22	11	17	mA	20 MHz **(Note 4)**	
DC23	21	32	mA	40 MHz **(Note 4)**	
DC24	30	45	mA	60 MHz **(Note 4)**	
DC25	40	60	mA	80 MHz	
DC25a	50	75	mA	100 MHz, $-40°C \leq T_A \leq +85°C$	
DC25c	72	84	mA	120 MHz, $0°C \leq T_A \leq +70°C$	
DC26	100	—	µA	+25ºC, 3.3V	LPRC (31 kHz) **(Note 4)**

Note 1: A device's I$_{DD}$ supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for I$_{DD}$ measurements are as follows:
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 7, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating (ON bit = 0), but the associated PMD bit is clear
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V$_{SS}$
- $\overline{MCLR}$ = V$_{DD}$
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: This parameter is characterized, but not tested in manufacturing.

TABLE 31-19:   PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp					
Param. No.	Symbol	Characteristics[1]	Min.	Typical	Max.	Units	Conditions	
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	3.92	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes	
OS51a	FSYS	On-Chip VCO System Frequency	60	—	120	MHz	Commercial devices	
OS51b			60	—	100	MHz	Industrial devices	
OS51c			60	—	80	MHz	V-temp devices	
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	—	
OS53	DCLK	CLKO Stability[2] (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\dfrac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 40 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\dfrac{40}{20}}} = \frac{D_{CLK}}{1.41}$$

TABLE 31-20:   INTERNAL FRC ACCURACY

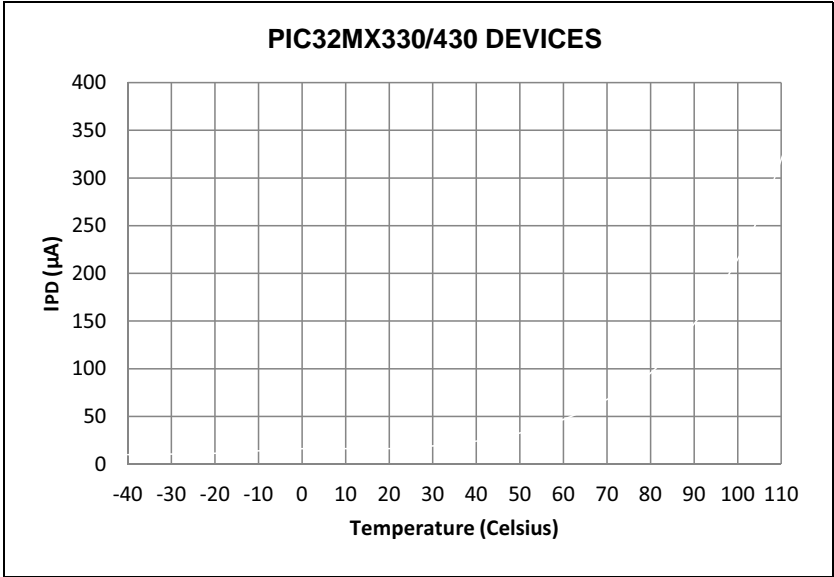| AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal FRC Accuracy @ 8.00 MHz[1]						
F20b	FRC	-0.9	—	+0.9	%	—

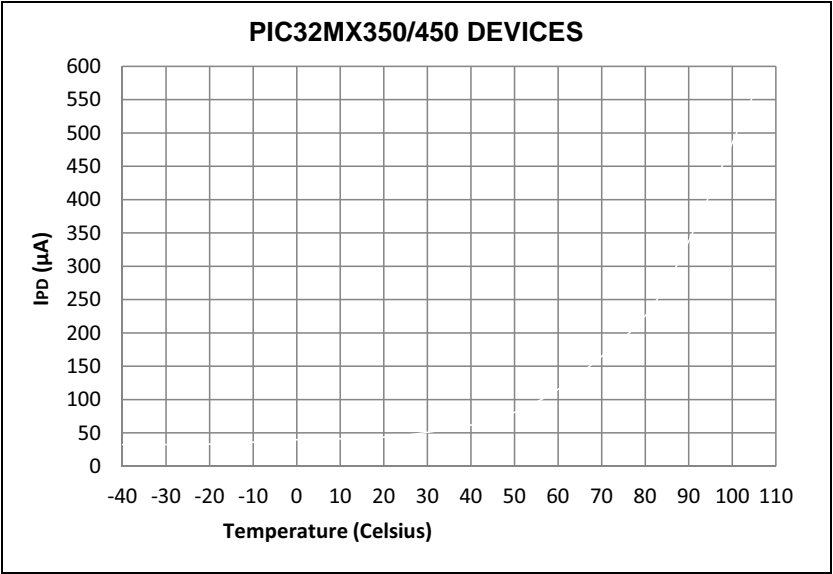**Note 1:** Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

NOTES:

FIGURE 32-5: TYPICAL IPD CURRENT @ VDD = 3.3V
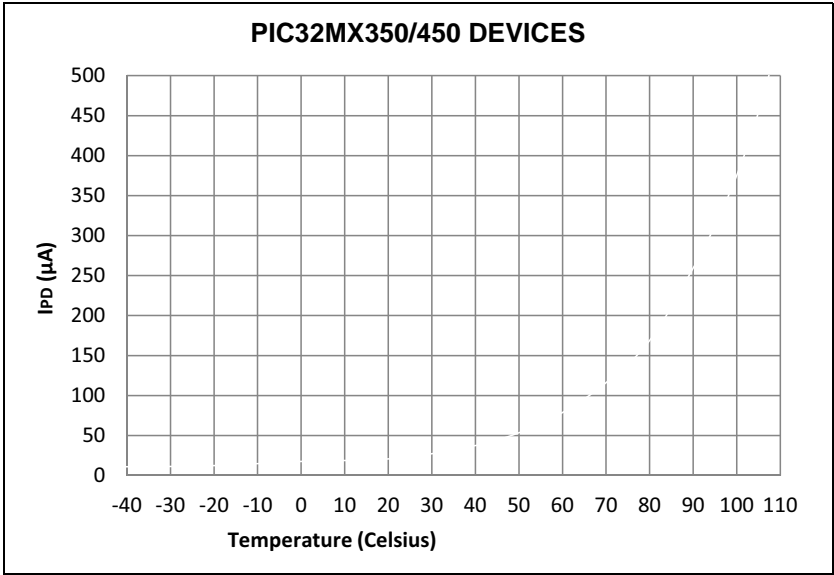
PIC32MX330/430 DEVICES

FIGURE 32-6: TYPICAL IPD CURRENT @ VDD = 3.3V

PIC32MX350/450 DEVICES

FIGURE 32-7: TYPICAL IPD CURRENT @ VDD = 3.3V

PIC32MX350/450 DEVICES
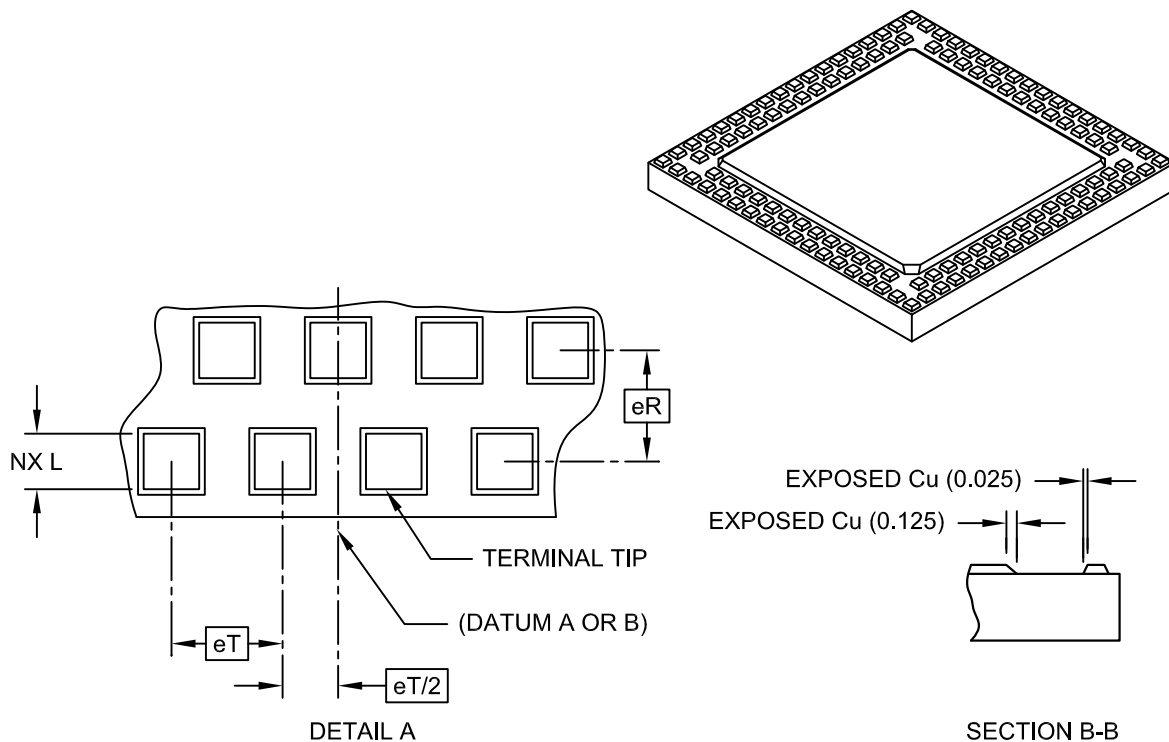
FIGURE 32-8: TYPICAL IIDLE CURRENT @ VDD = 3.3V

PIC32MX330/430 DEVICES
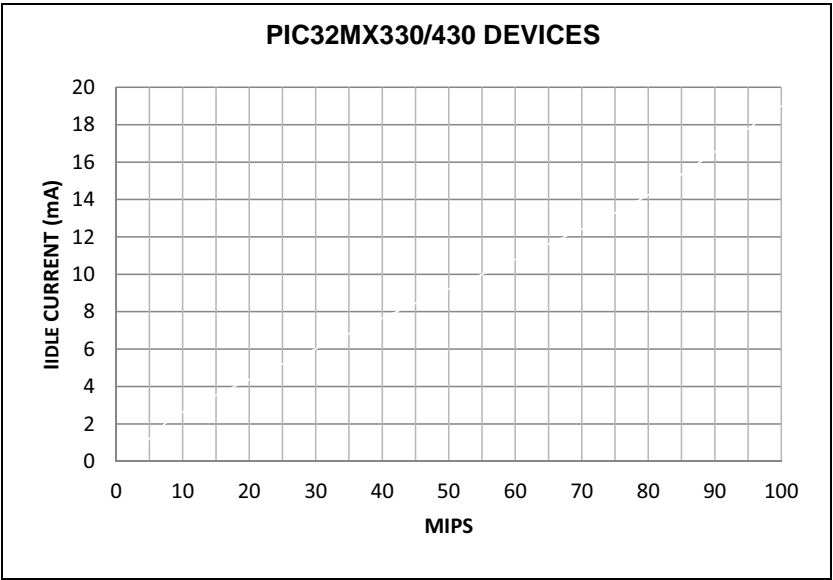
124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging	

NX L

eR

TERMINAL TIP

(DATUM A OR B)

eT

eT/2

DETAIL A

EXPOSED Cu (0.025)

EXPOSED Cu (0.125)

SECTION B-B

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		124	
Pitch	eT		0.50 BSC	
Pitch (Inner to outer terminal ring)	eR		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	-	0.05
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	6.40	6.55	6.70
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	6.40	6.55	6.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2