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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx470f512l-i-pf

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC32MX330/350/370/430/450/470

		Pin Numb	er			
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	Pin Type	Buffer Type	Description
RE0	60	93	B52	I/O	ST	
RE1	61	94	A64	I/O	ST	
RE2	62	98	A66	I/O	ST	
RE3	63	99	B56	I/O	ST	
RE4	64	100	A67	I/O	ST	PORTE is a hidiractional I/O part
RE5	1	3	B2	I/O	ST	PORTE IS a bidirectional i/O port
RE6	2	4	A4	I/O	ST	
RE7	3	5	B3	I/O	ST	
RE8	_	18	A11	I/O	ST	
RE9	_	19	B10	I/O	ST	
RF0	58	87	B49	I/O	ST	
RF1	59	88	A60	I/O	ST	
RF2	34(1)	52	A36	I/O	ST	
RF3	33	51	A35	I/O	ST	
RF4	31	49	B27	I/O	ST	
RF5	32	50	A32	I/O	ST	PORTF is a bidirectional I/O port
RF6	35(1)	55(1)	B30 ⁽¹⁾	I/O	ST	
RF7	_	54 ⁽¹⁾	A37 ⁽¹⁾	I/O	ST	
RF8	_	53	B29	I/O	ST	
RF12	_	40	A27	I/O	ST	
RF13	_	39	B22	I/O	ST	
RG0	_	90	A61	I/O	ST	
RG1	_	89	B50	I/O	ST	
RG2	37 ⁽¹⁾	57 ⁽¹⁾	B31	I/O	ST	
RG3	36(1)	56 ⁽¹⁾	A38	I/O	ST	
RG6	4	10	A7	I/O	ST	
RG7	5	11	B6	I/O	ST	
RG8	6	12	A8	I/O	ST	PORTG is a bidirectional 1/0 port
RG9	8	14	A9	I/O	ST	
RG12		96	A65	I/O	ST	
RG13	_	97	B55	I/O	ST	
RG14	_	95	B54	I/O	ST	
RG15	_	1	A2	I/O	ST	
T1CK	48	74	B40	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	PPS	I	ST	Timer5 External Clock Input
Legend:	CMOS = C	MOS compati	tible input or o	output	Ar	alog = Analog input P = Power

TABLE 1-1-PINOLIT I/O DESCRIPTIONS (CONTINUED)

ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer

Output

Input

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices.



6.1 Reset Control Registers

TABLE 6-1: SYSTEM CONTROL REGISTER MAP

ess	Register Name ⁽¹⁾										Bits								ú
Virtual Addr (BF80_#)		Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
E600	RCON	31:16	—	—	HVDR	—	—	—	—	—	_	_	—	—	—	—	—	—	0000
FOUU		15:0	_	—	_	_	_	_	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	xxxx ⁽²⁾
F610	DOMIDET	31:16	_	—	_	_	_	_	_	_	—	_	—	_	—	_	_	—	0000
	RSWRST	15:0	_	_	_	_	_	_	_	_	_	-	_	_	_	_	_	SWRST	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

Intermed Course(1)	100 #	Vector		Interru	upt Bit Location		Persistent
Interrupt Source 7	IRQ #	#	Flag	Enable	Priority	Sub-priority	Interrupt
CNB – PORTB Input Change Interrupt	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>	Yes
CNC – PORTC Input Change Interrupt	46	33	IFS1<14>	IEC1<14>	IPC8<12:10>	IPC8<9:8>	Yes
CND – PORTD Input Change Interrupt	47	33	IFS1<15>	IEC1<15>	IPC8<12:10>	IPC8<9:8>	Yes
CNE – PORTE Input Change Interrupt	48	33	IFS1<16>	IEC1<16>	IPC8<12:10>	IPC8<9:8>	Yes
CNF – PORTF Input Change Interrupt	49	33	IFS1<17>	IEC1<17>	IPC8<12:10>	IPC8<9:8>	Yes
CNG – PORTG Input Change Interrupt	50	33	IFS1<18>	IEC1<18>	IPC8<12:10>	IPC8<9:8>	Yes
PMP – Parallel Master Port	51	34	IFS1<19>	IEC1<19>	IPC8<20:18>	IPC8<17:16>	Yes
PMPE – Parallel Master Port Error	52	34	IFS1<20>	IEC1<20>	IPC8<20:18>	IPC8<17:16>	Yes
SPI2E – SPI2 Fault	53	35	IFS1<21>	IEC1<21>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2RX – SPI2 Receive Done	54	35	IFS1<22>	IEC1<22>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2TX – SPI2 Transfer Done	55	35	IFS1<23>	IEC1<23>	IPC8<28:26>	IPC8<25:24>	Yes
U2E – UART2 Error	56	36	IFS1<24>	IEC1<24>	IPC9<4:2>	IPC9<1:0>	Yes
U2RX – UART2 Receiver	57	36	IFS1<25>	IEC1<25>	IPC9<4:2>	IPC9<1:0>	Yes
U2TX – UART2 Transmitter	58	36	IFS1<26>	IEC1<26>	IPC9<4:2>	IPC9<1:0>	Yes
I2C2B – I2C2 Bus Collision Event	59	37	IFS1<27>	IEC1<27>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2S – I2C2 Slave Event	60	37	IFS1<28>	IEC1<28>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2M – I2C2 Master Event	61	37	IFS1<29>	IEC1<29>	IPC9<12:10>	IPC9<9:8>	Yes
U3E – UART3 Error	62	38	IFS1<30>	IEC1<30>	IPC9<20:18>	IPC9<17:16>	Yes
U3RX – UART3 Receiver	63	38	IFS1<31>	IEC1<31>	IPC9<20:18>	IPC9<17:16>	Yes
U3TX – UART3 Transmitter	64	38	IFS2<0>	IEC2<0>	IPC9<20:18>	IPC9<17:16>	Yes
U4E – UART4 Error	65	39	IFS2<1>	IEC2<1>	IPC9<28:26>	IPC9<25:24>	Yes
U4RX – UART4 Receiver	66	39	IFS2<2>	IEC2<2>	IPC9<28:26>	IPC9<25:24>	Yes
U4TX – UART4 Transmitter	67	39	IFS2<3>	IEC2<3>	IPC9<28:26>	IPC9<25:24>	Yes
U5E – UART5 Error	68	40	IFS2<4>	IEC2<4>	IPC10<4:2>	IPC10<1:0>	Yes
U5RX – UART5 Receiver	69	40	IFS2<5>	IEC2<5>	IPC10<4:2>	IPC10<1:0>	Yes
U5TX – UART5 Transmitter	70	40	IFS2<6>	IEC2<6>	IPC10<4:2>	IPC10<1:0>	Yes
CTMU – CTMU Event	71	41	IFS2<7>	IEC2<7>	IPC10<12:10>	IPC10<9:8>	Yes
DMA0 – DMA Channel 0	72	42	IFS2<8>	IEC2<8>	IPC10<20:18>	IPC10<17:16>	No
DMA1 – DMA Channel 1	73	43	IFS2<9>	IEC2<9>	IPC10<28:26>	IPC10<25:24>	No
DMA2 – DMA Channel 2	74	44	IFS2<10>	IEC2<10>	IPC11<4:2>	IPC11<1:0>	No
DMA3 – DMA Channel 3	75	45	IFS2<11>	IEC2<11>	IPC11<12:10>	IPC11<9:8>	No
		Lowe	st Natural Or	der Priority			

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX330/350/370/430/450/470 Controller Family Features" for the list of available peripherals.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0						
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
31:24	ROTRIM<8:1>													
00.40	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0						
23:10	ROTRIM<0>	—	—	—	—	—	—	—						
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0						
15:8	—	_	—	—	—	_	—	—						
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0						
7:0	_	_	_	_	—	_	_	_						

REGISTER 8-4: REFOTRIM: REFERENCE OSCILLATOR TRIM REGISTER

Legend:	y = Value set from Configuration bits on POR							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'						
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					

bit 31-23 ROTRIM<8:0>: Reference Oscillator Trim bits

Note: While the ON bit (REFOCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

11.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 27. "USB On-The-Go (OTG)" (DS60001126), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module. The PIC32 USB module includes the following features:

- USB full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- · Transaction handshaking performed by hardware
- · Endpoint buffering anywhere in system RAM
- · Integrated DMA to access system RAM and Flash
- The implementation and use of the USB Note: specifications, and other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0 U-0		U-0
31.24	—	—	—	—		—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0			—	—	—	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

REGISTER 11-4: U10TGCON: USB OTG CONTROL REGISTER

Legend:

- J			
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 DPPULUP: D+ Pull-Up Enable bit	
---	--

- 1 = D+ data line pull-up resistor is enabled
- 0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

- 1 = D- data line pull-up resistor is enabled
- 0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit

- 1 = D+ data line pull-down resistor is enabled
- 0 = D+ data line pull-down resistor is disabled

bit 4 DMPULDWN: D- Pull-Down Enable bit

- 1 = D- data line pull-down resistor is enabled
- 0 = D- data line pull-down resistor is disabled
- bit 3 **VBUSON:** VBUS Power-on bit
 - 1 = VBUS line is powered
 - 0 = VBUS line is not powered
- bit 2 OTGEN: OTG Functionality Enable bit
 - 1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
 - 0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 VBUSCHG: VBUS Charge Enable bit

- 1 = VBUS line is charged through a pull-up resistor
- 0 = VBUS line is not charged through a resistor

bit 0 VBUSDIS: VBUS Discharge Enable bit

- 1 = VBUS line is discharged through a pull-down resistor
- 0 = VBUS line is not discharged through a resistor

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
15:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0		SEO	PKTDIS ⁽⁴⁾	HEBDET		DESIME(3)	DDDDCT	USBEN ⁽⁴⁾
	JUNE	320	TOKBUSY ^(1,5)	USBROI	HOSTEN,	RESUMEN	FFDROI	SOFEN ⁽⁵⁾

REGISTER 11-11: U1CON: USB CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-8 Unimplemented: Read as '0'

- bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit 1 = JSTATE detected on the USB
 - 0 = No JSTATE detected
- bit 6 SE0: Live Single-Ended Zero flag bit
 1 = Single Ended Zero detected on the USB
 0 = No Single Ended Zero detected
- bit 5 **PKTDIS:** Packet Transfer Disable bit⁽⁴⁾
 - 1 = Token and packet processing disabled (set upon SETUP token received)
 - 0 = Token and packet processing enabled
 - TOKBUSY: Token Busy Indicator bit^(1,5)
 - 1 = Token being executed by the USB module
 - 0 = No token being executed

bit 4 USBRST: Module Reset bit⁽⁵⁾

- 1 = USB reset is generated
- 0 = USB reset is terminated

bit 3 HOSTEN: Host Mode Enable bit⁽²⁾

- 1 = USB host capability is enabled
- 0 = USB host capability is disabled

bit 2 RESUME: RESUME Signaling Enable bit⁽³⁾

- 1 = RESUME signaling is activated
- 0 = RESUME signaling is disabled
- **Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).
 - 2: All host control logic is reset any time that the value of this bit is toggled.
 - **3:** Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
 - 4: Device mode.
 - 5: Host mode.

13.2 Control Registers

TABLE 13-1: TIMER1 REGISTER MAP

ess		0								В	its								6
Virtual Addı (BF80_#	Registe Name ⁽¹⁾	Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000		31:16	_	—	_	-	—	—	—	—	-	—	—	—	—	-	-	—	0000
0000	TICON	15:0	ON	—	SIDL	TWDIS	TWIP	_	_	—	TGATE	—	TCKP	S<1:0>	—	TSYNC	TCS	—	0000
0610		31:16		—	_	—	_	_	_	—	—	—	_	_	—	—	—	—	0000
0010		15:0								TMR1	<15:0>								0000
0620	DD1	31:16	_	_	_	_	_	_	_	_	_	_		_	_	_	_	_	0000
0020	FKI	15:0								PR1<	<15:0>								FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0			
	—	—	—	RXBUFELM<4:0>							
00.40	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0			
23.10	—	—	—	TXBUFELM<4:0>							
45.0	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0			
15:8	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR			
7.0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0			
7:0	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF			

REGISTER 18-3: SPIxSTAT: SPI STATUS REGISTER

Legend:	C = Clearable bit	HS = Set in hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 31-29 Unimplemented: Read as '0'
- bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 23-21 Unimplemented: Read as '0'
- bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 15-13 Unimplemented: Read as '0'
- bit 12 **FRMERR:** SPI Frame Error status bit
 - 1 = Frame error is detected
 - 0 = No Frame error is detected
 - This bit is only valid when FRMEN = 1.
- bit 11 SPIBUSY: SPI Activity Status bit
 - 1 = SPI peripheral is currently busy with some transactions
 - 0 = SPI peripheral is currently idle
- bit 10-9 Unimplemented: Read as '0'
- bit 8 SPITUR: Transmit Under Run bit
 - 1 = Transmit buffer has encountered an underrun condition
 - 0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.

- bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
 - 1 = When SPI module shift register is empty
 - 0 = When SPI module shift register is not empty
- bit 6 SPIROV: Receive Overflow Flag bit
 - 1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
 - 0 = No overflow has occurred

This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.

- bit 5 SPIRBE: RX FIFO Empty bit (valid only when ENHBUF = 1) 1 = RX FIFO is empty (CRPTR = SWPTR)
 - 0 = RX FIFO is not empty (CRPTR \neq SWPTR)
- bit 4 Unimplemented: Read as '0'

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
51.24	_	_	_	—	—	_	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
45.0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
15.8	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC ⁽³⁾		AMASK	<3:0> ⁽³⁾		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	ARPT<7:0> ⁽³⁾								

REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ALRMEN: Alarm Enable bit^(1,2)
 - 1 = Alarm is enabled
 - 0 = Alarm is disabled

bit 14 CHIME: Chime Enable bit⁽²⁾

- 1 = Chime is enabled ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse. When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 ALRMSYNC: Alarm Sync bit⁽³⁾

- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 AMASK<3:0>: Alarm Mask Configuration bits⁽³⁾

- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved; do not use
- 1011 = Reserved; do not use
- 11xx = Reserved; do not use
- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

23.1 **Control Registers**

TABLE 23-1: ADC REGISTER MAP

SSS										Bi	its								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
		31:16		_	_	_		_	_	_	_	_	_	_	_	_	_	_	0000
9000	AD1CON1"	15:0	ON	_	SIDL	_	_		FORM<2:0	>		SSRC<2:0>	>	CLRASAM	—	ASAM	SAMP	DONE	0000
0040		31:16	_	_	—	—	_	—	_	—	-	—	—	_	—	—	-	_	0000
9010	AD1CON2"	15:0		VCFG<2:0>	>	OFFCAL		CSCNA		—	BUFS	_		SMPI	<3:0>	•	BUFM	ALTS	0000
0020		31:16	_	—	—	—	_	_	_	_	_	_	—	—	_	_	_	_	0000
9020	AD ICONS.	15:0	ADRC	—	—			SAMC<4:0>	>					ADCS	\$<7:0>				0000
0040		31:16	CH0NB	_	—		(CH0SB<4:0	>		CH0NA	_	_		(CH0SA<4:0	>		0000
5040	ADICIIS.	15:0	-	_	-	_		—	—	—		—	—	-	—	—		—	0000
0050		31:16	_	CSSL30	CSSL29	CSSL28	CSSL27	CSSL26	CSSL25	CSSL24	CSSL23	CSSL22	CSSL21	CSSL20	CSSL19	CSSL18	CSSL17	CSSL16	0000
9030	ADTOSSL	15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
0070									0000										
9070	ADCIDOIO	15:0							ADC Ne		(ADC ID0I	0<31.02)							0000
9080		31:16								sult Word 1		1<31.0>)							0000
3000	ADCIDOI I	15:0							ADC Net			1501.02)							0000
9090		31:16								sult Word 2		2<31.0>)							0000
3030		15:0							ADC Ne.			2 ~ 3 1.02)							0000
9040		31:16								sult Word 3		3<31.0>)							0000
3070	ADC IDOI 3	15:0							ADC Ne.			3531.02)							0000
90B0	ADC1BUE4	31:16							ADC Res	sult Word 4	(ADC1BUE	4<31.0>)							0000
0000	1.0010011	15:0							7120110		(7.201201	1.01.07							0000
9000	ADC1BUE5	31:16							ADC Res	sult Word 5	(ADC1BUE	5<31.0>)							0000
0000	12012010	15:0							71201100		(7.201201	0.01.07							0000
9000	ADC1BUE6	31:16							ADC Res	sult Word 6	(ADC1BUE	6<31.0>)							0000
0020		15:0							1.201.00		(,	• • • • • •							0000
90E0	ADC1BUF7	31:16							ADC Res	sult Word 7	(ADC1BUF	7<31:0>)							0000
		15:0									(, ,							0000
90F0	ADC1BUF8	31:16							ADC Res	sult Word 8	(ADC1BUF	8<31:0>)							0000
		15:0							1.001.00		(,								0000
9100	ADC1BUF9	31:16							ADC Res	sult Word 9	(ADC1BUF	9<31:0>)							0000
0.00		15:0							1.2 0 1.00										0000
Leger	nd: x = u	nknowr	n value on l	Reset: =	unimpleme	nted, read a	s '0'. Rese	t values are	shown in h	exadecimal									

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for details. Note 1:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
51.24	EDG1MOD	EDG1POL		EDG1S	EDG2STAT	EDG1STAT			
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	
23.10	EDG2MOD	EDG2POL		EDG2S	—	—			
15.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15.0	ON	—	CTMUSIDL	TGEN ⁽¹⁾	EDGEN	EDGSEQEN	IDISSEN ⁽²⁾	CTTRIG	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7.0			ITRIM	1<5:0>			IRNG<1:0>		

REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 EDG1MOD: Edge 1 Edge Sampling Select bit

1 = Input is edge-sensitive

0 = Input is level-sensitive

bit 30 EDG1POL: Edge 1 Polarity Select bit

1 = Edge 1 programmed for a positive edge response

0 = Edge 1 programmed for a negative edge response

bit 29-26 EDG1SEL<3:0>: Edge 1 Source Select bits

1111 = Reserved

1110 = C2OUT pin is selected

- 1101 = C1OUT pin is selected
- 1100 = IC3 Capture Event is selected
- 1011 = IC2 Capture Event is selected
- 1010 = IC1 Capture Event is selected
- 1001 = CTED8 pin is selected
- 1000 = CTED7 pin is selected
- 0111 = CTED6 pin is selected
- 0110 = CTED5 pin is selected
- 0101 = CTED4 pin is selected
- 0100 = CTED3 pin is selected
- 0011 = CTED1 pin is selected
- 0010 = CTED2 pin is selected
- 0001 = OC1 Compare Event is selected

0000 = Timer1 Event is selected

bit 25 EDG2STAT: Edge 2 Status bit

Indicates the status of Edge 2 and can be written to control edge source

- 1 = Edge 2 has occurred
- 0 = Edge 2 has not occurred
- **Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 31-42) in Section 31.0 "Electrical Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

REGISIC	ER 20-1: CIMUCON: CIMU CONTROL REGISTER (CONTINUE
bit 24	EDG1STAT: Edge 1 Status bit
	Indicates the status of Edge 1 and can be written to control edge source
	1 = Edge 1 has occurred
	0 = Edge 1 has not occurred
bit 23	EDG2MOD: Edge 2 Edge Sampling Select bit
	1 = Input is edge-sensitive
h:+ 00	0 = Input is level-sensitive
DIT 22	EDG2POL: Edge 2 Polarity Select bit
	1 = Edge 2 programmed for a positive edge response
h:+ 04 40	0 = Euge z programmed for a negative euge response
DIL 21-18	
	1111 = Reserved
	1110 = C2OOT pin is selected 1101 = C1OUT pin is selected
	1100 = PBCLK clock is selected
	1011 = IC3 Capture Event is selected
	1010 = IC2 Capture Event is selected
	1001 = IC1 Capture Event is selected
	1000 = CTED13 pin is selected
	0111 = CTED12 pin is selected
	0110 = CTED10 pin is selected
	0100 = CTED9 pin is selected
	0011 = CTED1 pin is selected
	0010 = CTED2 pin is selected
	0001 = OC1 Compare Event is selected
	0000 = Timer1 Event is selected
bit 17-16	Unimplemented: Read as '0'
bit 15	ON: ON Enable bit
	1 = Module is enabled
	0 = Module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	CTMUSIDL: Stop in Idle Mode bit
	1 = Discontinue module operation when device enters Idle mode
	0 = Continue module operation in Idle mode
bit 12	TGEN: Time Generation Enable bit ⁽¹⁾
	1 = Enables edge delay generation
1.11.4.4	0 = Disables edge delay generation
dit 11	EDGEN: Edge Enable bit
	1 = Edges are not blocked
	$U = \Box OOES ALE DIOCKEO$

- **Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 31-42) in Section 31.0 "Electrical Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

27.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid. To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 27-1 for more information.

Note: Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TARI E 27-1·	PERIPHERAL MODULE DISABLE BITS AND LOCATIONS
IADLE ZI-I.	FERIFIERAL MODULE DISABLE DITS AND LOCATIONS

Peripheral ⁽¹⁾	PMDx bit Name ⁽¹⁾	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
СТМИ	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
I2C1	I2C1MD	PMD5<16>
12C2	I2C2MD	PMD5<17>
USB ⁽²⁾	USBMD	PMD5<24>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

Note 1: Not all modules and associated PMDx bits are available on all devices. See TABLE 1: "PIC32MX330/350/ 370/430/450/470 Controller Family Features" for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

NOTES:

TABLE 31-15: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHA		STICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments		
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time.	_	_	10	μs	See Note 1		
D313	DACREFH	CVREF Input Voltage Reference Range	AVss	—	AVdd	V	CVRSRC with CVRSS = 0		
			VREF-	_	VREF+	V	CVRSRC with CVRSS = 1		
D314	DVREF	CVREF Programmable Output Range	0	_	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size		
			0.25 x DACREFH	_	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/ 32 step size		
D315	DACRES	Resolution	_	_	DACREFH/24		CVRCON <cvrr> = 1</cvrr>		
			—	—	DACREFH/32		CVRCON <cvrr> = 0</cvrr>		
D316	DACACC	Absolute Accuracy ⁽²⁾	—	—	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>		
			—	—	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>		

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 31-16: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Param. No. Symbol Characteristics			Typical	Max.	Units	Comments		
D321	Cefc	External Filter Capacitor Value	8	10		μF	Capacitor must be low series resistance (3 ohm). Typical voltage on the VCAP pin is 1.8V.		



TABLE 31-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^\circ C \leq TA \leq +70^\circ C \mbox{ for Commercial} \\ & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics ⁽²⁾		-	Min.	Typical	Max.	Units	Conditions	
TA10	ТтхН	TxCK High Time	Synchronous, with prescaler		[(12.5 ns or 1 TPB)/N] — + 25 ns		—	ns	Must also meet parameter TA15	
			Asynchronous, with prescaler		10	_		ns		
TA11	ΤτxL	TxCK Low Time	Synchronous, with prescaler		[(12.5 ns or 1 Трв)/N] + 25 ns	(12.5 ns or 1 TPB)/N]		ns	Must also meet parameter TA15	
			Asynchronous, with prescaler		10 —			ns	—	
TA15	ΤτχΡ	TxCK Input Period	Synchronous, with prescaler		[(Greater of 25 ns or 2 Трв)/N] + 30 ns	_		ns	VDD > 2.7V	
					[(Greater of 25 ns or 2 Трв)/N] + 50 ns	_		ns	VDD < 2.7V	
			Asynchronous, with prescaler		20	_	_	ns	VDD > 2.7V (Note 3)	
					50	_		ns	VDD < 2.7V (Note 3)	
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by set TCS bit (T1CON<1>))			32	_	100	kHz	_	
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment			_		1	Трв	—	

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).



FIGURE 31-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

TABLE 31-30: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHA	ARACTERIS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions	
SP10	TscL	SCKx Output Low Time (Note 3)	Tsck/2	—	_	ns	—	
SP11	TscH	SCKx Output High Time (Note 3)	Tsck/2	_	_	ns	—	
SP20	TscF	SCKx Output Fall Time (Note 4)	—	_		ns	See parameter DO32	
SP21	TscR	SCKx Output Rise Time (Note 4)	—	—	_	ns	See parameter DO32	
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	—	_		ns	See parameter DO32	
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	—	—		ns	See parameter DO31	
SP35	TscH2doV,	SDOx Data Output Valid after SCKx Edge	—	_	15	ns	VDD > 2.7V	
	TscL2doV		—		20	ns	VDD < 2.7V	
SP36	TDOV2sc, TDOV2scL	SDOx Data Output Setup to First SCKx Edge	15	—		ns	_	
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	15	—		ns	VDD > 2.7V	
			20	—	_	ns	VDD < 2.7V	
SP41	TscH2DIL,	Hold Time of SDIx Data Input	15	_	_	ns	VDD > 2.7V	
	TscL2DIL	to SCKx Edge	20	_	_	ns	VDD < 2.7V	

Note 1: These parameters are characterized, but not tested in manufacturing.

- Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only 2: and are not tested.
- The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not 3: violate this specification.
- Assumes 50 pF load on all SPIx pins. 4:

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Number of Pins	Ν	124				
Pitch	eT	0.50 BSC				
Pitch (Inner to outer terminal ring)	eR	0.50 BSC				
Overall Height	A	0.80	0.85	0.90		
Standoff	A1	0.00	-	0.05		
Overall Width	E	9.00 BSC				
Exposed Pad Width	E2	6.40	6.55	6.70		
Overall Length	D	9.00 BSC				
Exposed Pad Length	D2	6.40	6.55	6.70		
Contact Width	b	0.20	0.25	0.30		
Contact Length	L	0.20	0.25	0.30		
Contact-to-Exposed Pad	K	0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2