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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx470f512l-v-pf

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The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32<sup>®</sup> architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

# 3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e<sup>®</sup>, is also available by accessing the CP0 registers, listed in Table 3-2.

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX330/350/370/430/450/470 family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers.
8	BadVAddr <sup>(1)</sup>	Reports the address for the most recent address-related exception.
9	Count <sup>(1)</sup>	Processor cycle count.
10	Reserved	Reserved in the PIC32MX330/350/370/430/450/470 family core.
11	Compare <sup>(1)</sup>	Timer interrupt control.
12	Status <sup>(1)</sup>	Processor status and control.
12	IntCtl <sup>(1)</sup>	Interrupt system status and control.
12	SRSCtl <sup>(1)</sup>	Shadow register set status and control.
12	SRSMap <sup>(1)</sup>	Provides mapping from vectored interrupt to a shadow set.
13	Cause <sup>(1)</sup>	Cause of last general exception.
14	EPC <sup>(1)</sup>	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration register 1.
16	Config2	Configuration register 2.
16	Config3	Configuration register 3.
17-22	Reserved	Reserved in the PIC32MX330/350/370/430/450/470 family core.
23	Debug <sup>(2)</sup>	Debug control and exception status.
24	DEPC <sup>(2)</sup>	Program counter at last debug exception.
25-29	Reserved	Reserved in the PIC32MX330/350/370/430/450/470 family core.
30	ErrorEPC <sup>(1)</sup>	Program counter at last error.
31	DESAVE <sup>(2)</sup>	Debug handler scratchpad register.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Note 1: Registers used in exception processing.

**2:** Registers used during debug.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21:24	R	R	R	R	R	R	R	R		
31:24				BMXDRM	ISZ<31:24>					
22:46	R	R	R	R	R	R	R	R		
23.10	BMXDRMSZ<23:16>									
45.0	R	R	R	R	R	R	R	R		
15:8	BMXDRMSZ<15:8>									
7.0	R	R	R	R	R	R	R	R		
7:0				BMXDR	MSZ<7:0>					

#### BMXDRMSZ: DATA RAM SIZE REGISTER **REGISTER 4-5:**

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BMXDRMSZ<31:0>: Data RAM Memory (DRM) Size bits

Static value that indicates the size of the Data RAM in bytes: 0x00004000 = Device has 16 KB RAM 0x00008000 = Device has 32 KB RAM 0x00010000 = Device has 64 KB RAM 0x00020000 = Device has 128 KB RAM

#### **REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS** REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	—	—	—	—	—	—			
00.40	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:16	_	—	_	—	BMXPUPBA<19:16>						
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0			
15:8	BMXPUPBA<15:8>										
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
7:0				BMXPU	PBA<7:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 Unimplemented: Read as '0'

bit 19-11 BMXPUPBA<19:11>: Program Flash (PFM) User Program Base Address bits

## bit 10-0 BMXPUPBA<10:0>: Read-Only bits Value is always '0', which forces 2 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

2: The value in this register must be less than or equal to BMXPFMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31.24	—	—	—	—	—	—	—	—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	—	—	—	—	—	—	—	—			
45.0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
15:8	—	—	—	—	—	5	SRIPL<2:0> <sup>(1)</sup>				
7.0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0	_	_			VEC	<5:0> <sup>(1)</sup>					

#### REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 Unimplemented: Read as '0'

- bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits<sup>(1)</sup> 111-000 = The priority level of the latest interrupt presented to the CPU
- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 VEC<5:0>: Interrupt Vector bits<sup>(1)</sup> 11111-00000 = The interrupt vector that is presented to the CPU
- Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31.24		IPTMR<31:24>									
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:10	IPTMR<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	IPTMR<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0				IPTM	IR<7:0>						

#### REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Legend:						
R = Readable bit	W = Writable bit	N = Writable bit $U =$ Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

# 9.2 Control Registers

# TABLE 9-1: PREFETCH REGISTER MAP

ess										Bit	s								
Virtual Addro (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
4000		31:16	—	_	—	_	—	_	—	—	—	_	—	_	—	—	—	CHECOH	0000
4000	CHECON"	15:0	—	_	—	—	_	—	DCSZ	<1:0>	—	—	PREFE	N<1:0>	-	F	FMWS<2:0	)>	0007
4010		31:16	CHEWEN	—	—	—	_	—	—	—	—	—	—	—	—	—	—	—	0000
4010	CHEACC ?	15:0	—	—	_	—	_	—	—	—	—	_	_	_		CHEID	X<3:0>		00xx
4020		31:16	LTAGBOOT	—	_	—		—	_					LTAG<	<23:16>				xxx0
4020	CHEIAG	15:0						LTAG<	:15:4>						LVALID	LLOCK	LTYPE	_	xxx2
1030	CHEMSK(1)	31:16	—	—	_	_		_	_			_	_		—	_	—	_	0000
+030		15:0					LN	/ASK<15:5	>						—	—	—	_	xxxx
1010	CHEWO	31:16								CHEWO	<31.0>								xxxx
-0-0	CHEWO	15:0								CHEWO	ST.02								xxxx
4050	CHEW1	31:16								CHEW1	<31.0>								xxxx
4000	ONEWI	15:0								ONEWI	-01.04								xxxx
4060	CHEW2	31:16								CHEW/2	<31.0>								xxxx
4000	OTIEWZ	15:0								ONEW2	-01.04								xxxx
4070	CHEW3	31:16								CHFW3	<31.0>								xxxx
	0.12110	15:0								0.12110	0110								xxxx
4080	CHELRU	31:16	—	—	—	_	—		—				CH	ielru<24:	16>				0000
	0	15:0								CHELRU	<15:0>								0000
4090	CHEHIT	31:16								CHEHIT	<31:0>								XXXX
		15:0									XXXX								
40A0	CHEMIS	31:16								CHEMIS	<31:0>								XXXX
		15:0																	XXXX
40C0	CHEPFABT	31:16								CHEPFAE	T<31:0>								XXXX
		15:0					(1) 5 (				-								XXXX

Legend:

x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

#### REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	
31:24	—	—	BYTC	)<1:0>	WBO <sup>(1)</sup>	—	_	BITO <sup>(1)</sup>	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	_	_	—	_	_	—	
45.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	—	—	—			PLEN<4:0>			
7.0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
7:0	CRCEN	CRCAPP <sup>(1)</sup>	CRCTYP	—	_	(	CRCCH<2:0>	•	

# Legend:

Logena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-30 Unimplemented: Read as '0'

- bit 29-28 BYTO<1:0>: CRC Byte Order Selection bits
  - 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
  - 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
  - 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
  - 00 = No swapping (i.e., source byte order)
- bit 27 **WBO:** CRC Write Byte Order Selection bit<sup>(1)</sup>
  - 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
  - 0 = Source data is written to the destination unaltered
- bit 26-25 Unimplemented: Read as '0'
- bit 24 BITO: CRC Bit Order Selection bit<sup>(1)</sup>

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

### <u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode):

- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

### bit 23-13 Unimplemented: Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits<sup>(1)</sup>

<u>When CRCTYP (DCRCCON<15>) = 1</u> (CRC module is in IP Header mode): These bits are unused.

<u>When CRCTYP (DCRCCON<15>) = 0</u> (CRC module is in LFSR mode): Denotes the length of the polynomial -1.

- bit 7 CRCEN: CRC Enable bit
  - 1 = CRC module is enabled and channel transfers are routed through the CRC module
  - 0 = CRC module is disabled and channel transfers proceed normally
- Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		—	_	_	—	_	_	_
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	_	—	_	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

# REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24	Unimplemented: Read as '0'
bit 23	CHSDIE: Channel Source Done Interrupt Enable bit
	1 = Interrupt is enabled
1.11.00	
bit 22	CHSHIE: Channel Source Half Empty Interrupt Enable bit
	1 =  Interrupt is enabled 0 =  Interrupt is disabled
bit 21	CHDDIE: Channel Destination Done Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 20	CHDHIE: Channel Destination Half Full Interrupt Enable bit
	1 = Interrupt is enabled
h:+ 40	0 = Interrupt is disabled
DIT 19	
	0 = Interrupt is disabled
bit 18	CHCCIE: Channel Cell Transfer Complete Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 17	CHTAIE: Channel Transfer Abort Interrupt Enable bit
	1 = Interrupt is enabled
bit 16	0 – Interrupt is disabled
DIL TO	
	0 = Interrupt is disabled
bit 15-8	Unimplemented: Read as '0'
bit 7	CHSDIF: Channel Source Done Interrupt Flag bit
	1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
	0 = No interrupt is pending
bit 6	CHSHIF: Channel Source Half Empty Interrupt Flag bit
	<ul> <li>1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)</li> <li>0 = No interrupt is pending</li> </ul>
bit 5	CHDDIF: Channel Destination Done Interrupt Flag bit
	1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ
	0 = No interrupt is pending
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~ <u>~</u> ~ ~ ~ ~ ~ ~ U	

# 12.1 Parallel I/O (PIO) Ports

All port pins have ten registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

# 12.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the presence of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the **"Device Pin Tables"** section for the available pins and their functionality.

# 12.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

# 12.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an NOP.

# 12.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MX330/350/370/430/450/470 devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

Each I/O pin also has a weak pull-up and every I/O pin has a weak pull-down connected to it. The pullups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on change notifi							
	cation pins should always be disabled							
	when the port pin is configured as a digital							
	output. They should also be disabled on							
	5V tolerant pins when the pin voltage can							
	exceed VDD.							

An additional control register (CNCONx) is shown in Register 12-3.

# 12.2 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.



# FIGURE 14-2: TIMER2/3, 4/5 BLOCK DIAGRAM (32-BIT)<sup>(1)</sup>

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31:24		HR10	<3:0>			HR01	<3:0>		
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23:10		MIN10	<3:0>		MIN01<3:0>				
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15:8	SEC10<3:0>				SEC01<3:0>				
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
7:0	—	—	—	—	—	-	—	—	
Legend:									
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'						
-n = Value at POR '1' = Bit is set			et	'0' = Bit is cleared x = Bit is unknown					

# REGISTER 22-5: ALRMTIME: ALARM TIME VALUE REGISTER

bit 31-28 HR10<3:0>: Binary Coded Decimal value of hours bits, 10s place digits; contains a value from 0 to 2
bit 27-24 HR01<3:0>: Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9
bit 23-20 MIN10<3:0>: Binary Coded Decimal value of minutes bits, 10s place digits; contains a value from 0 to 5
bit 19-16 MIN01<3:0>: Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9
bit 15-12 SEC10<3:0>: Binary Coded Decimal value of seconds bits, 10s place digits; contains a value from 0 to 5
bit 11-8 SEC01<3:0>: Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9
bit 7-0 Unimplemented: Read as '0'

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
10.0	ON <sup>(1)</sup>	COE	CPOL <sup>(2)</sup>	—	—	—	—	COUT
7.0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
7.0	EVPOL<1:0>		_	CREF	_	_	CCH	<1:0>

#### REGISTER 24-1: CMxCON: COMPARATOR CONTROL REGISTER

# Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Comparator ON bit<sup>(1)</sup>
  - 1 = Module is enabled. Setting this bit does not affect the other bits in this register
  - 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register
- bit 14 **COE:** Comparator Output Enable bit
  - 1 = Comparator output is driven on the output CxOUT pin
  - 0 = Comparator output is not driven on the output CxOUT pin
- bit 13 **CPOL:** Comparator Output Inversion bit<sup>(2)</sup>
  - 1 = Output is inverted
  - 0 = Output is not inverted
- bit 12-9 Unimplemented: Read as '0'
- bit 8 **COUT:** Comparator Output bit
  - 1 =Output of the Comparator is a '1'
  - 0 = Output of the Comparator is a '0'
- bit 7-6 EVPOL<1:0>: Interrupt Event Polarity Select bits
  - 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
  - 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
  - 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
  - 00 = Comparator interrupt generation is disabled
- bit 5 Unimplemented: Read as '0'

### bit 4 **CREF:** Comparator Positive Input Configure bit

- 1 = Comparator non-inverting input is connected to the internal CVREF
- 0 = Comparator non-inverting input is connected to the CXINA pin

#### bit 3-2 Unimplemented: Read as '0'

- bit 1-0 CCH<1:0>: Comparator Negative Input Select bits for Comparator
  - 11 = Comparator inverting input is connected to the IVREF
  - 10 = Comparator inverting input is connected to the CxIND pin
  - 01 = Comparator inverting input is connected to the CxINC pin
  - 00 = Comparator inverting input is connected to the CxINB pin
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

# 25.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them. A block diagram of the module is illustrated in Figure 25-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/Vss or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The CVREF module has the following features:

- High and low range selection
- · Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- · Output can be connected to a pin



### FIGURE 25-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

NOTES:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
31:24	—	—	—	—	—	—	FWDTWI	NSZ<1:0>
00.40	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
23:10	FWDTEN	WINDIS	—	WDTPS<4:0>				
45.0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
15:8	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC POSCMOD<1:0		OD<1:0>
7.0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
7:0	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

### REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Legend:	r = Reserved bit P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-26 Reserved: Write '1'

bit 25-24 FWDTWINSZ<1:0>: Watchdog Timer Window Size bits

- 11 = Window size is 25%
- 10 = Window size is 37.5%
- 01 = Window size is 50%
- 00 = Window size is 75%

#### bit 23 FWDTEN: Watchdog Timer Enable bit

- 1 = Watchdog Timer is enabled and cannot be disabled by software
- 0 = Watchdog Timer is not enabled; it can be enabled in software

### bit 22 WINDIS: Watchdog Timer Window Enable bit

- 1 = Watchdog Timer is in non-Window mode
- 0 = Watchdog Timer is in Window mode

#### bit 21 Reserved: Write '1'

#### bit 20-16 WDTPS<4:0>: Watchdog Timer Postscale Select bits

•
10100 <b>= 1:1048576</b>
10011 <b>= 1:524288</b>
10010 <b>= 1:262144</b>
10001 <b>= 1:131072</b>
10000 <b>= 1:65536</b>
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 <b>= 1:4096</b>
01011 <b>= 1:2048</b>
01010 = 1:1024
01001 <b>= 1:512</b>
01000 <b>= 1:256</b>
00111 <b>= 1:128</b>
00110 <b>= 1:64</b>
00101 <b>= 1:32</b>
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

**Note 1:** Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

# 31.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX330/350/370/430/450/470 AC characteristics and timing parameters.

## FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



#### TABLE 31-17: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
DO50	Cosco	OSC2 pin	_	_	15	pF	In XT and HS modes when an external crystal is used to drive OSC1
DO56	Сю	All I/O pins and OSC2	_		50	pF	EC mode
DO58	Св	SCLx, SDAx	—		400	pF	In I <sup>2</sup> C mode

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

### FIGURE 31-2: EXTERNAL CLOCK TIMING



# TABLE 31-21: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions			
LPRC @ 31.25 kHz <sup>(1)</sup>									
F21	LPRC	-15	_	+15	%	—			

Note 1: Change of LPRC frequency as VDD changes.

# FIGURE 31-3: I/O TIMING CHARACTERISTICS



## TABLE 31-22: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param. No.	Symbol	Characteris	stics <sup>(2)</sup>	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time		_	5	15	ns	Vdd < 2.5V
				_	5	10	ns	Vdd > 2.5V
DO32	TIOF	Port Output Fall Time		—	5	15	ns	Vdd < 2.5V
				—	5	10	ns	VDD > 2.5V
DI35	TINP	INTx Pin High or Low Time		10	_	_	ns	
DI40	Trbp	CNx High or Low Tir	2	_	_	TSYSCLK	_	

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for Commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp				
Param. No. Symbol		Characteristics		Min. <sup>(1)</sup>	Max.	Units	Conditions	
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Трв * (BRG + 2)		μS	_	
			400 kHz mode	Трв * (BRG + 2)	—	μS	—	
			1 MHz mode <b>(Note 2)</b>	Трв * (BRG + 2)	—	μs	_	
IM11	THI:SCL	Clock High Time	100 kHz mode	Трв * (BRG + 2)	_	μS	—	
			400 kHz mode	Трв * (BRG + 2)	_	μS	—	
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs	_	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be	
			400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF	
			1 MHz mode <b>(Note 2)</b>	—	100	ns		
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF	
			400 kHz mode	20 + 0.1 Св	300	ns		
			1 MHz mode (Note 2)	_	300	ns		
IM25	Tsu:dat	Data Input Setup Time	100 kHz mode	250	—	ns		
			400 kHz mode	100	—	ns		
			1 MHz mode <b>(Note 2)</b>	100	—	ns		
IM26	Thd:dat	Data Input Hold Time	100 kHz mode	0	—	μS	—	
			400 kHz mode	0	0.9	μS		
			1 MHz mode <b>(Note 2)</b>	0	0.3	μs		
IM30	Tsu:sta	Start Condition Setup Time	100 kHz mode	Трв * (BRG + 2)	—	μS	Only relevant for	
			400 kHz mode	Трв * (BRG + 2)	—	μS	Repeated Start	
			1 MHz mode <b>(Note 2)</b>	Трв * (BRG + 2)	—	μs	condition	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	Трв * (BRG + 2)	_	μS	After this period, the	
			400 kHz mode	Трв * (BRG + 2)	—	μS	first clock pulse is	
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs	generated	
IM33	Tsu:sto	Stop Condition Setup Time	100 kHz mode	Трв * (BRG + 2)	—	μS	—	
			400 kHz mode	Трв * (BRG + 2)	_	μS		
			1 MHz mode (Note 2)	Трв * (BRG + 2)		μS	]	

# TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

**Note 1:** BRG is the value of the  $l^2C$  Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**3:** The typical value for this parameter is 104 ns.

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^\circ C \leq TA \leq +70^\circ C \mbox{ for Commercial} \\ & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Charact	eristics	Min.	Max.	Units	Conditions		
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	_		
			400 kHz mode	600		ns			
			1 MHz mode <b>(Note 1)</b>	250		ns			
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—		
			400 kHz mode	0	1000	ns			
			1 MHz mode <b>(Note 1)</b>	0	350	ns			
IS45	Tbf:sda	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus		
			400 kHz mode	1.3	—	μS	must be free before a new		
			1 MHz mode (Note 1)	0.5	_	μS	transmission can start		
IS50	Св	Bus Capacitive Loading			400	pF	—		

# TABLE 31-34: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).



# FIGURE 31-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)



100

NOTES: