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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx470f512l-v-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.2 Architecture Overview

The MIPS32[®] M4K[®] processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e[®] Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32[®] M4K[®] processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction
 address
- Logic for branch determination and branch target address calculation
- · Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32[®] M4K[®] processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

Op code	Operand Size (mul rt) (div rs)	Latency	Repeat Rate						
MULT/MULTU, MADD/MADDU,	16 bits	1	1						
MSUB/MSUBU	32 bits	2	2						
MUL	16 bits	2	1						
	32 bits	3	2						
DIV/DIVU	8 bits	12	11						
	16 bits	19	18						
	24 bits	26	25						
	32 bits	33	32						

TABLE 3-1: MIPS32[®] M4K[®] PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/ DIVIDE UNIT LATENCIES AND REPEAT RATES



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	
31.24				NVMKE	Y<31:24>				
00.40	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	
23:10	NVMKEY<23:16>								
45.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	
15:8	NVMKEY<15:8>								
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	
				NVMK	EY<7:0>				

REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Legend:

Legenu.				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 NVMKEY<31:0>: Unlock Register bits

These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24		NVMADDR<31:24>									
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:10	NVMADDR<23:16>										
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	NVMADDR<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0				NVMA	DDR<7:0>						

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 **NVMADDR<31:0>:** Flash Address bits Bulk/Chip/PFM Erase: Address is ignored Page Erase: Address identifies the page to erase Row Program: Address identifies the row to program Word Program: Address identifies the word to program

REGIST	ER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)
bit 9-8	IS1<1:0>: Interrupt Subpriority bits
	11 = Interrupt subpriority is 3
	10 = Interrupt subpriority is 2
	01 = Interrupt subpriority is 1
	00 = Interrupt subpriority is 0
bit 7-5	Unimplemented: Read as '0'
bit 4-2	IP0<2:0>: Interrupt Priority bits
	111 = Interrupt priority is 7
	•
	010 = Interrupt priority is 2
	001 = Interrupt priority is 1
	000 = Interrupt is disabled
bit 1-0	IS0<1:0>: Interrupt Subpriority bits
	11 = Interrupt subpriority is 3
	10 = Interrupt subpriority is 2
	01 = Interrupt subpriority is 1
	00 = Interrupt subpriority is 0
Note:	This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit
Note.	definitions.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

- bit 18-16 PLLMULT<2:0>: Phase-Locked Loop (PLL) Multiplier bits
 - 111 = Clock is multiplied by 24
 - 110 = Clock is multiplied by 21
 - 101 = Clock is multiplied by 20
 - 100 = Clock is multiplied by 19
 - 011 = Clock is multiplied by 18
 - 010 = Clock is multiplied by 17
 - 001 = Clock is multiplied by 16
 - 000 =Clock is multiplied by 15
- bit 15 Unimplemented: Read as '0'
- bit 14-12 COSC<2:0>: Current Oscillator Selection bits
 - 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC (FRC) Oscillator divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (Posc) (XT, HS or EC)
 - 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast RC (FRC) Oscillator
- bit 11 Unimplemented: Read as '0'
- bit 10-8 NOSC<2:0>: New Oscillator Selection bits
 - 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC Oscillator (FRC) divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (XT, HS or EC)
 - 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

- bit 7 CLKLOCK: Clock Selection Lock Enable bit
 - If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):
 - 1 = Clock and PLL selections are locked
 - 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x): Clock and PLL selections are never locked and may be modified.

- bit 6 ULOCK: USB PLL Lock Status bit⁽¹⁾
 - 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
 - 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled
- bit 5 SLOCK: PLL Lock Status bit
 - 1 = PLL module is in lock or PLL module start-up timer is satisfied
 - 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled
- bit 4 **SLPEN:** Sleep Mode Enable bit
 - 1 = Device will enter Sleep mode when a WAIT instruction is executed
 - 0 = Device will enter Idle mode when a WAIT instruction is executed
- bit 3 CF: Clock Fail Detect bit
 - 1 = FSCM has detected a clock failure
 - 0 = No clock failure has been detected
- **Note 1:** This bit is available on PIC32MX4XX devices only.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31:24	—	RODIV<14:8> ^(1,3)							
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	RODIV<7:0> ⁽³⁾								
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC	
15:8	ON	_	SIDL	OE	RSLP ⁽²⁾	_	DIVSWEN	ACTIVE	
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
				_	ROSEL<3:0> ⁽¹⁾				

REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

Legend: HC = Hardware Clearabl		HS = Hardware Settable		
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

- bit 31 Unimplemented: Read as '0'
- bit 30-16 **RODIV<14:0>:** Reference Clock Divider bits^(1,3) This value selects the Reference Clock Divider bits. See Figure 8-1 for more information. bit 15 **ON:** Output Enable bit 1 = Reference Oscillator Module is enabled 0 = Reference Oscillator Module is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode
- bit 12 OE: Reference Clock Output Enable bit
 - 1 = Reference clock is driven out on REFCLKO pin
 - 0 = Reference clock is not driven out on REFCLKO pin
- bit 11 RSLP: Reference Oscillator Module Run in Sleep bit⁽²⁾
 - 1 = Reference Oscillator Module output continues to run in Sleep
 - 0 = Reference Oscillator Module output is disabled in Sleep
- bit 10 Unimplemented: Read as '0'
- bit 9 DIVSWEN: Divider Switch Enable bit
 - 1 = Divider switch is in progress
 - 0 = Divider switch is complete
- bit 8 ACTIVE: Reference Clock Request Status bit
 - 1 = Reference clock request is active
 - 0 = Reference clock request is not active
- bit 7-4 Unimplemented: Read as '0'
- **Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
 - **2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
 - 3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31.24				CHEW1<	:31:24>				
00.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23:10	CHEW1<23:16>								
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15.0	CHEW1<15:8>								
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
7.0				CHEW1	<7:0>				

REGISTER 9-6: CHEW1: CACHE WORD 1

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 **CHEW1<31:0>:** Word 1 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

REGISTER 9-7: CHEW2: CACHE WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
31.24				CHEW2<	:31:24>					
22:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
23.10	CHEW2<23:16>									
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
15.0	CHEW2<15:8>									
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
				CHEW2	<7:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW2<31:0>:** Word 2 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		—	_	_	—	_	_	_
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	_	—	_	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24	Unimplemented: Read as '0'
bit 23	CHSDIE: Channel Source Done Interrupt Enable bit
	1 = Interrupt is enabled
1.11.00	
bit 22	CHSHIE: Channel Source Half Empty Interrupt Enable bit
	1 = Interrupt is enabled 0 = Interrupt is disabled
bit 21	CHDDIE: Channel Destination Done Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 20	CHDHIE: Channel Destination Half Full Interrupt Enable bit
	1 = Interrupt is enabled
h:+ 40	0 = Interrupt is disabled
DIT 19	
	0 = Interrupt is disabled
bit 18	CHCCIE: Channel Cell Transfer Complete Interrupt Enable bit
	1 = Interrupt is enabled
	0 = Interrupt is disabled
bit 17	CHTAIE: Channel Transfer Abort Interrupt Enable bit
	1 = Interrupt is enabled
bit 16	CHERIE: Channel Address Error Interrunt Enable bit
DIL TO	
	0 = Interrupt is disabled
bit 15-8	Unimplemented: Read as '0'
bit 7	CHSDIF: Channel Source Done Interrupt Flag bit
	1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
	0 = No interrupt is pending
bit 6	CHSHIF: Channel Source Half Empty Interrupt Flag bit
	 1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2) 0 = No interrupt is pending
bit 5	CHDDIF: Channel Destination Done Interrupt Flag bit
	1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ
	0 = No interrupt is pending
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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31.24	31:24 CHSSA<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23.10				CHSSA<	:23:16>						
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHSSA<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0 CHSSA<7:0>											

REGISTER 10-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

 bit 31-0
 CHSSA<31:0> Channel Source Start Address bits

 Channel source start address.

 Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24	CHDSA<31:24>										
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:10				CHDSA<	:23:16>						
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHDSA<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0	CHDSA<7:0>										

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits Channel destination start address.

 $\ensuremath{\textbf{Note:}}$ This must be the physical address of the destination.

ess										Bi	ts								
Virtual Addr (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6510	TRISE	31:16	_	_	—	—		-	-										0000
00.0		15:0	—	_	TRISF13	TRISF12	_	_	_	TRISF8	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	xxxx
6520	PORTE	31:16	—	—	-	—	-	-	—	—	-	—	—	-	—	—	—	—	0000
0020		15:0	—	—	RF13	RF12	-	-	—	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6530	LATE	31:16	—	_	_	—	_	_	_		_	—	—	—	—	_			0000
0000	2	15:0	—	_	LATF13	LATF12	—	_	_	LATF8	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6540	ODCE	31:16	—			—		_			_	—			—	—			0000
0040	000	15:0	—		ODCF13	ODCF12		_		ODCF8	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	xxxx
6550	CNPLIE	31:16	—			—		_			_	—			—	—			0000
0000		15:0	—		CNPUF13	CNPUF12		_		CNPUF8	CNPUF7	CNPUF6	CNPUF5	CNPUF4	CNPDF3	CNPUF2	CNPUF1	CNPUF0	xxxx
6560	CNPDE	31:16	—			—		_			_	—			—	—			0000
0000		15:0	—	_	CNPDF13	CNPDF12	—	—	—	CNPDF8	CNPDF7	CNPDF6	CNPDF5	CNPDF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	xxxx
6570	CNCONE	31:16	—	_	—	—	_	-	-	—	-	—	—	-	—	—	_	—	0000
0070	CINCOIN	15:0	ON	_	SIDL	—	-	_	_	—	_	—	—	_	—	—	_	—	0000
6580		31:16	_		_	_				_		_	_		_	_	_	_	0000
0300	CINLINI	15:0	_		CNIEF13	CNIEF12				CNIEF8	CNIEF7	_	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	xxxx
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6590	CNSTATF	15:0	_	_	CN STATF13	CN STATF12	_	_	_	CN STATF8	CN STATF7	_	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	xxxx

TABLE 12-11: PORTF REGISTER MAP FOR PIC32MX330F064L, PIC32MX350F128L, PIC32MX350F256L, AND PIC32MX370F512L DEVICES

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

TABLE 12-18: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

ss										В	its								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
EDOO		31:16		_	_	_	_	_	_	_	_	_	_		_	_	_	—	0000
FB90	RPC4R**	15:0	-	_	_	_	—	_	—	_	_	—	_			RPC4	<3:0>		0000
EDDA	PDC13D	31:16	_	—	—	—	—	—	—	—	—	—	—		—	—	_	_	0000
1004	KFC ISK	15:0	—			—	—			—		—				RPC1	3<3:0>	-	0000
FBB8	RPC14R	31:16	—			—	—	—		—		—	—	_	—	—	—	—	0000
I BB0	KFC14K	15:0	—	—	—	—	—	—	—	—	—	—	—	_		RPC1	4<3:0>		0000
FRCO	REDUB	31:16	—			—	—			—		—			_	—	—	—	0000
1 DC0	IN DOIN	15:0	_	—	—	—	—	—	—	—	—	—	—	_		RPDO	<3:0>		0000
EBC4		31:16	—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	—	0000
1 004	REDIK	15:0	—	—	—	—	—	—	—	—	—	—	—	_		RPD1	<3:0>		0000
ERCO		31:16	—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	—	0000
1 BC0	KF D2K	15:0	_	—	—	—	—	—	—	—	—	—	—	_		RPD2	<3:0>		0000
ERCC		31:16	_	—	—	—	—	_	—	_	—	—	_		—	—	_	_	0000
1 BCC	REDSR	15:0	_	—	—	—	—	—	—	—	—	—	—	_		RPD3	<3:0>		0000
EBDO		31:16	—	—	—	—	—	—	—	—	—	—	—	-	—	—	—	—	0000
FBDU	KFD4K	15:0	_	_	_	—	—	—	_	_	_	—	_	l		RPD4	<3:0>		0000
EDDA		31:16	_	—	—	—	—	—	_	—	—	—	—		—	_	_	_	0000
FDD4	REDSK	15:0	_	_	_	—	—	—	_	_	_	_	—			RPD	i<3:0>		0000
EDEO		31:16	_	_	_	—	—	—	_	_	_	—	_	l	_	-	_	_	0000
I BLU	REDOR	15:0	_	—	—	—	—	—	—	—	—	—	—	_		RPD8	<3:0>		0000
EDEA	BBDOB	31:16	_	_	_	—	—	—	_	_	_	_	—		_	_	_	_	0000
FDE4	RED9R	15:0	_	—	—	—	—	_	—	_	—	—	_			RPDS	<3:0>		0000
EDES		31:16	—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	_	0000
FDEO	REDIOR	15:0	_	_	_	—	—	—	_	_	_	_	—			RPD1	0<3:0>		0000
EREC		31:16	_	—	—	—	—	_	—	_	—	—	_		—	—	_	_	0000
IBLC	REDTIK	15:0		—	—	—	—	—	—	—	—	—	—	_		RPD1	1<3:0>		0000
EDEO	DD12D(1)	31:16	_	_	_	—	—	—	_	_	_	_	—		_	_	_	_	0000
FDFU	RFD12R* /	15:0	_	_	_	—	—	—	_	_	_	—	_	l		RPD1	2<3:0>		0000
EDEO		31:16	_	—	—	—	—	—	_	—	—	—	—		—	_	_	_	0000
ГБГО	KFD14K ⁽⁾	15:0	_	_	_	—	—	—	_	_	_	_	—			RPD1	4<3:0>		0000
EDEO		31:16	_	_	_	_	—	_	—		_	_	_	_	—		_		0000
FBFC	RPU15K"	15:0		_	_				_		_	_		_		RPD1	5<3:0>		0000
5000		31:16	—	—	_	—	—	_	—	_	—	—	—	_	—	_	—	—	0000
FCUC	RPESR	15:0	_	—	—	_	_	_	—	—	—	—	—	_		RPE3	<3:0>		0000

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Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is only available on devices without a USB module.

3: This register is not available on 64-pin devices with a USB module.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	_	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ^(1,2)	—	—	—	—	—	—	—
7.0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
7:0	_		WDTWINEN	WDTCLR				

REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Legend:	y = Values set from Configuration bits on POR							
R = Readable bit	W = Writable bit	U = Unimplemented bit, I	read as '0'					
-n = Value at POR	'1' = Bit is set	x = Bit is unknown						

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Watchdog Timer Enable bit^(1,2)
 - 1 = Enables the WDT if it is not enabled by the device configuration
 - 0 = Disable the WDT if it was enabled in software
- bit 14-7 Unimplemented: Read as '0'
- bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.
- bit 1 WDTWINEN: Watchdog Timer Window Enable bit
 - 1 = Enable windowed Watchdog Timer
 - 0 = Disable windowed Watchdog Timer
- bit 0 WDTCLR: Watchdog Timer Reset bit
 - 1 = Writing a '1' will clear the WDT
 - 0 = Software cannot force this bit to a '0'
- **Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
 - 2: When using the 1:1 PBCLK divisor, the user software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 16-1: ICXCON: INPUT CAPTURE 'X' CONTROL REGISTER (CONTINUED)

- bit 2-0 ICM<2:0>: Input Capture Mode Select bits
 - 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
 - 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
 - 101 = Prescaled Capture Event mode every sixteenth rising edge
 - 100 = Prescaled Capture Event mode every fourth rising edge
 - 011 = Simple Capture Event mode every rising edge
 - 010 = Simple Capture Event mode every falling edge
 - 001 = Edge Detect mode every edge (rising and falling)
 - 000 = Input Capture module is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

19.0 INTER-INTEGRATED CIRCUIT (I²C)

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 24. "Inter-Integrated Circuit (I²C)" (DS60001116), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/ pic32). The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard. Figure 19-1 illustrates the I^2C module block diagram.

Each I^2C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module offers the following key features:

- I²C interface supporting both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation; detects bus collision and arbitrates accordingly
- · Provides support for address bit masking

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REGISTER 19-1: I2CxCON: I²C CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	_	—	—	_	_	—	—
45.0	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7.0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
7:0	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:	HC = Cleared in Hardware	e	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** I²C Enable bit⁽¹⁾
 - 1 = Enables the I^2C module and configures the SDA and SCL pins as serial port pins
 - 0 = Disables the I^2 C module; all I^2 C pins are controlled by PORT functions
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when device enters Idle mode
 - 0 = Continue module operation in Idle mode
 - **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
 - 1 = Release SCLx clock

bit 12

- 0 = Hold SCLx clock low (clock stretch)
- If STREN = 1:

Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:

Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

- bit 11 STRICT: Strict I²C Reserved Address Rule Enable bit
 - 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
 - 0 = Strict I²C Reserved Address Rule is not enabled

bit 10 A10M: 10-bit Slave Address bit

- 1 = I2CxADD is a 10-bit slave address
- 0 = I2CxADD is a 7-bit slave address
- bit 9 **DISSLW:** Disable Slew Rate Control bit
 - 1 = Slew rate control is disabled
 - 0 = Slew rate control is enabled
- bit 8 SMEN: SMBus Input Levels bit
 - 1 = Enable I/O pin thresholds compliant with SMBus specification
 - 0 = Disable SMBus input thresholds
- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

21.1 Control Registers

TABLE 21-1: PARALLEL MASTER PORT REGISTER MAP

ess										Bi	its								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
7000	PMCON	31:16	_	_	—	—	—	—	—	_	_	—	—				_	—	0000
1000	FINCON	15:0	ON	_	SIDL	ADRMI	JX<1:0>	PMPTTL	PTWREN	PTRDEN	CSF	<1:0>	ALP	CS2P	CS1P	_	WRSP	RDSP	0000
7010		31:16	_	_	—	_	—	_	_		_	_	_	_	_	_	_	—	0000
7010		15:0	BUSY	IRQM<1:0>		INCM	INCM<1:0> MODE16		MODE	MODE<1:0> WAITB<1:0>		B<1:0>	WAITM<3:0>			WAIT	E<1:0>	0000	
7020		31:16	_	_	—	_	—	_	_		_	_	_	_	_	_	_	—	0000
7020	PINADUR	15:0	CS2	CS1							ADDR	<13:0>							0000
7020		31:16		000											0000				
7030	PMDOUT	15:0								DATAOU	11<31.0>								0000
7040		31:16		DATAIN (21.0)										0000					
1040 PMDIN 15:0 DATAIN<31:0>									0000										
7050		31:16	—	_	—	—	—	—	—		_	-	—	_	_	_	_	—	0000
7000 PIWAEIN 15:0 PTEN<15:0>								0000											
7060	DMOTAT	31:16	_	_	—	—	-	—	—	—	_	—	—	_	_	_	_	—	0000
1000	FINISTAL	15:0	IBF	IBOV	_	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	_	_	OB3E	OB2E	OB1E	OB0E	BFBF
Logon	and:																		

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0		
31.24	—	—	—	—	—	—	CAL<9):8>		
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	CAL<7:0>									
15.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0		
15.0	ON ^(1,2)	—	SIDL	—	—	—	—	—		
7.0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0		
7.0	RTSECSEL ⁽³⁾	RTCCLKON	_	—	RTCWREN ⁽⁴⁾	RTCSYNC	HALFSEC ⁽⁵⁾	RTCOE		

REGISTER 22-1: RTCCON: RTC CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 Unimplemented: Read as '0'

bit 25-16 CAL<9:0>: RTC Drift Calibration bits, which contain a signed 10-bit integer value 0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute 000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute 000000000 = No adjustment 1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute 100000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute ON: RTCC On bit^(1,2) bit 15 1 = RTCC module is enabled 0 = RTCC module is disabled bit 14 Unimplemented: Read as '0' bit 13 SIDL: Stop in Idle Mode bit 1 = Disables the PBCLK to the RTCC when CPU enters in Idle mode 0 = Continue normal operation in Idle mode Unimplemented: Read as '0' bit 12-8 bit 7 RTSECSEL: RTCC Seconds Clock Output Select bit⁽³⁾ 1 = RTCC Seconds Clock is selected for the RTCC pin 0 = RTCC Alarm Pulse is selected for the RTCC pin bit 6 RTCCLKON: RTCC Clock Enable Status bit 1 = RTCC Clock is actively running 0 = RTCC Clock is not running bit 5-4 Unimplemented: Read as '0' **Note 1:** The ON bit is only writable when RTCWREN = 1. 2: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit. 3: Requires RTCOE = 1 (RTCCON<0>) for the output to be active. 4: The RTCWREN bit can be set only when the write sequence is enabled. 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 ARPT<7:0>: Alarm Repeat Counter Value bits⁽³⁾ 11111111 = Alarm will trigger 256 times

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

23.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32). The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- · Up to 1 Msps conversion speed
- · Up to 28 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- · Automatic Channel Scan mode
- Selectable conversion trigger source
- · 16-word conversion result buffer
- · Selectable buffer fill modes
- · Eight conversion result format options
- · Operation during CPU Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 23-1. The 10-bit ADC has up to 28 analog input pins, designated AN0-AN27. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.



4: This selection is only used with CTMU capacitive and time measurement.

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions	
D130	Eр	Cell Endurance	20,000	—	_	E/W	—	
D131	Vpr	VDD for Read	2.3	—	3.6	V	—	
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	_	
D134	TRETD	Characteristic Retention	20	_		Year	Provided no other specifications are violated	
D135	IDDP	Supply Current during Programming	_	10		mA	_	
D138	Tww	Word Write Cycle Time ⁽⁴⁾	44	—	59	μs	—	
D136	Trw	Row Write Cycle Time ^(2,4)	2.8	3.3	3.8	ms	_	
D137	TPE	Page Erase Cycle Time ⁽⁴⁾	22	_	29	ms		
D139	TCE	Chip Erase Cycle Time ⁽⁴⁾	86	_	116	ms	_	

TABLE 31-12: DC CHARACTERISTICS: PROGRAM MEMORY⁽³⁾

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 8 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

- **3:** Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.
- 4: This parameter depends on the FRC accuracy (see Table 31-20) and the FRC tuning values (see Register 8-2).

TABLE 31-13:	DC CHARACTERISTICS:	PROGRAM FLASH MEMOR	Y WAIT STATE
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	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)						
DC CHARACTERISTICS	$\begin{array}{ll} \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Required Flash Wait States	SYSCLK	Units	Conditions				
0 Wait State	0-40	MHz	-40°C to +85°C				
	0-30	MHz	-40°C to +105°C				
1 Wait State	41-80	MHz	-40°C to +85°C				
I Wait State	31-60	MHz	-40°C to +105°C				
2 Wait States	81-100	MHz	-40°C to +85°C				
	61-80	MHz	-40°C to +105°C				
3 Wait States	101-120	MHz	0°C to +70°C				