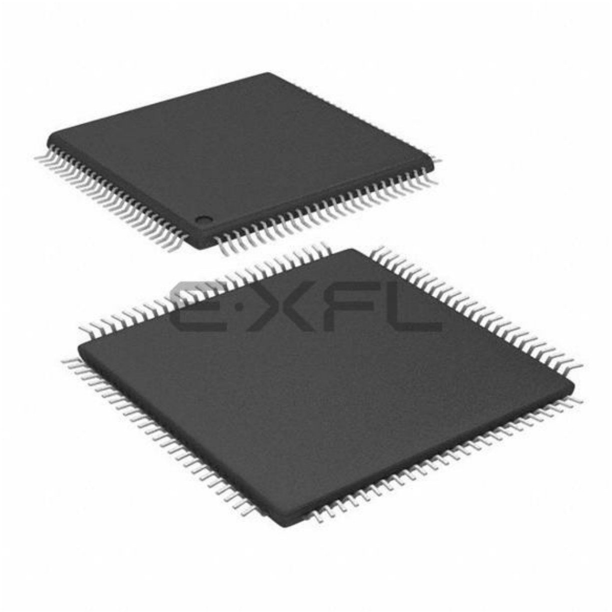
Microchip Technology - PIC32MX470F512LT-120/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx470f512lt-120-pt

Device Pin Tables

TABLE 2: PIN NAMES FOR 64-PIN DEVICES

64-PIN QFN(1,2,3,4) AND TQFP(1,2,3,4) (TOP VIEW)

PIC32MX330F064H
PIC32MX350F128H
PIC32MX350F256H
PIC32MX370F512H

64 1

QFN(4)

64 1

TQFP

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	RPF3/RF3
2	AN23/PMD6/RE6	34	RPF2/RF2
3	AN27/PMD7/RE7	35	RPF6/SCK1/INT0/RF6
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	SDA1/RG3
5	AN17/C1INC/RPG7/PMA4/RG7	37	SCL1/RG2
6	AN18/C2IND/RPG8/PMA3/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/RB5	43	RPD9/RD9
12	AN4/C1INB/RB4	44	RPD10/PMCS2/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMCS1/RD11
14	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	46	RPD0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3//RB7	50	AN25/RPD2/RD2
19	AVDD	51	AN26/RPD3/RD3
20	AVSS	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10//RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11//PMA13/RB10	55	RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/RPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31	RPF4/SDA2/PMA9/RF4	63	RPE3/CTPLS/PMD3/RE3
32	RPF5/SCL2/PMA8/RF5	64	AN21/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 “Peripheral Pin Select”** for restrictions.

2: Every I/O port pin (RBx-RGx), with the exception of RF6, can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 “I/O Ports”** for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: RPF6 (pin 35) is only available for output functions.

TABLE 3: PIN NAMES FOR 64-PIN DEVICES

64-PIN QFN(1,2) AND TQFP(1,2) (TOP VIEW)

PIC32MX430F064H
PIC32MX450F128H
PIC32MX450F256H
PIC32MX470F512H

64 1

QFN(3)

64 1

TQFP

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN22/RPE5/PMD5/RE5	33	USBID/RF3
2	AN23/PMD6/RE6	34	VBUS
3	AN27/PMD7/RE7	35	VUSB3V3
4	AN16/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN17/C1INC/RPG7/PMA4/RG7	37	D+
6	AN18/C2IND/RPG8/PMA3/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSC1/CLKI/RC12
8	AN19/C2INC/RPG9/PMA2/RG9	40	OSC2/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	RPD8/RTCC/RD8
11	AN5/C1INA/RPB5/VBUSON/RB5	43	RPD9/SDA1/RD9
12	AN4/C1INB/RB4	44	RPD10/SCL1/PMCS2/RD10
13	PGED3/AN3/C2INA/RPB3/RB3	45	RPD11/PMCS1/RD11
14	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	46	RPD0/INT0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/CTED12/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN6/RPB6/RB6	49	AN24/RPD1/RD1
18	PGED2/AN7/RPB7/CTED3//RB7	50	AN25/RPD2/SCK1/RD2
19	AVDD	51	AN26/RPD3/RD3
20	AVSS	52	RPD4/PMWR/RD4
21	AN8/RPB8/CTED10//RB8	53	RPD5/PMRD/RD5
22	AN9/RPB9/CTED4/PMA7/RB9	54	RD6
23	TMS/CVREFOUT/AN10/RPB10/CTED11//PMA13/RB10	55	RD7
24	TDO/AN11/PMA12/RB11	56	VCAP
25	VSS	57	VDD
26	VDD	58	RPF0/RF0
27	TCK/AN12/PMA11/RB12	59	RPF1/RF1
28	TDI/AN13/PMA10/RB13	60	PMD0/RE0
29	AN14/RPB14/CTED5/PMA1/RB14	61	PMD1/RE1
30	AN15/RPB15/OCFB/CTED6/PMA0/RB15	62	AN20/PMD2/RE2
31	RPF4/SDA2/PMA9/RF4	63	RPE3/CTPLS/PMD3/RE3
32	RPF5/SCL2/PMA8/RF5	64	AN21/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

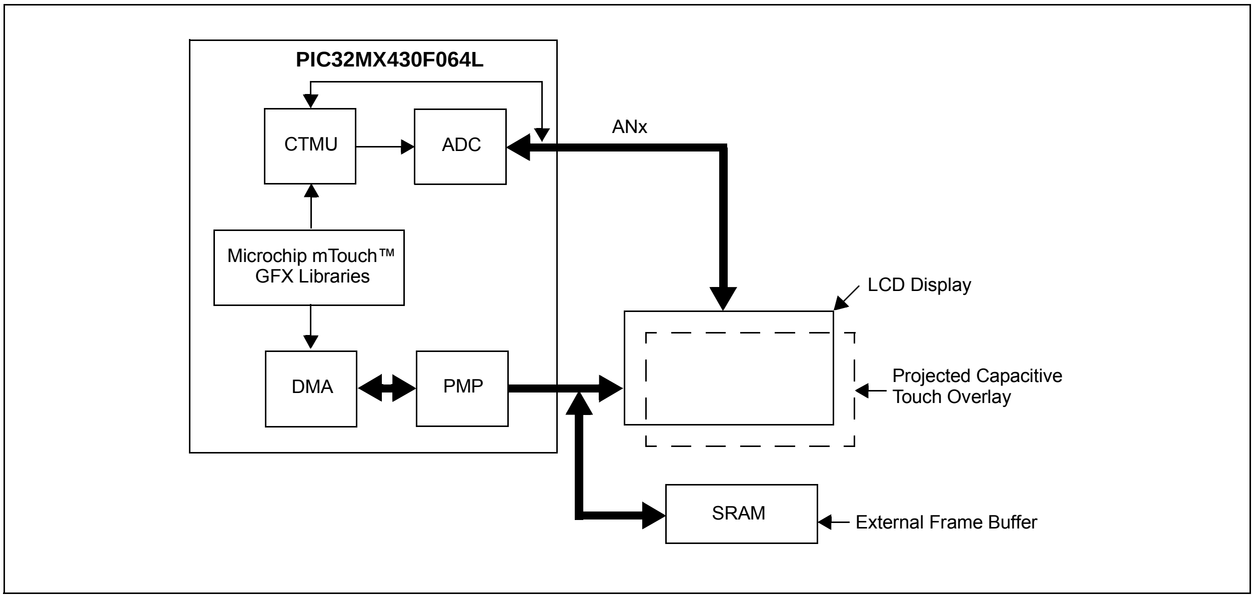
TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA			
AN0	16	25	B14	I	Analog	Analog input channels.
AN1	15	24	A15	I	Analog	
AN2	14	23	B13	I	Analog	
AN3	13	22	A13	I	Analog	
AN4	12	21	B11	I	Analog	
AN5	11	20	A12	I	Analog	
AN6	17	26	A20	I	Analog	
AN7	18	27	B16	I	Analog	
AN8	21	32	A23	I	Analog	
AN9	22	33	B19	I	Analog	
AN10	23	34	A24	I	Analog	
AN11	24	35	B20	I	Analog	
AN12	27	41	B23	I	Analog	
AN13	28	42	A28	I	Analog	
AN14	29	43	B24	I	Analog	
AN15	30	44	A29	I	Analog	
AN16	4	10	A7	I	Analog	
AN17	5	11	B6	I	Analog	
AN18	6	12	A8	I	Analog	
AN19	8	14	A9	I	Analog	
AN20	62	98	A66	I	Analog	
AN21	64	100	A67	I	Analog	
AN22	1	3	B2	I	Analog	
AN23	2	4	A4	I	Analog	
AN24	49	76	A52	I	Analog	
AN25	50	77	B42	I	Analog	
AN26	51	78	A53	I	Analog	
AN27	3	5	B3	I	Analog	
CLKI	39	63	B34	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	40	64	A42	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with the OSC2 pin function.
OSC1	39	63	B34	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	40	64	A42	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	73	A47	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	48	74	B40	O	—	32.768 kHz low-power oscillator crystal output.

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer
Analog = Analog input
O = Output
P = Power
I = Input

Note 1: This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices.

FIGURE 2-8: LOW-COST CONTROLLERLESS (LCC) GRAPHICS APPLICATION WITH PROJECTED CAPACITIVE TOUCH



4.0 MEMORY ORGANIZATION

> **Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX330/350/370/430/450/470 microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX330/350/370/430/450/470 devices to execute from data memory.

Key features include:

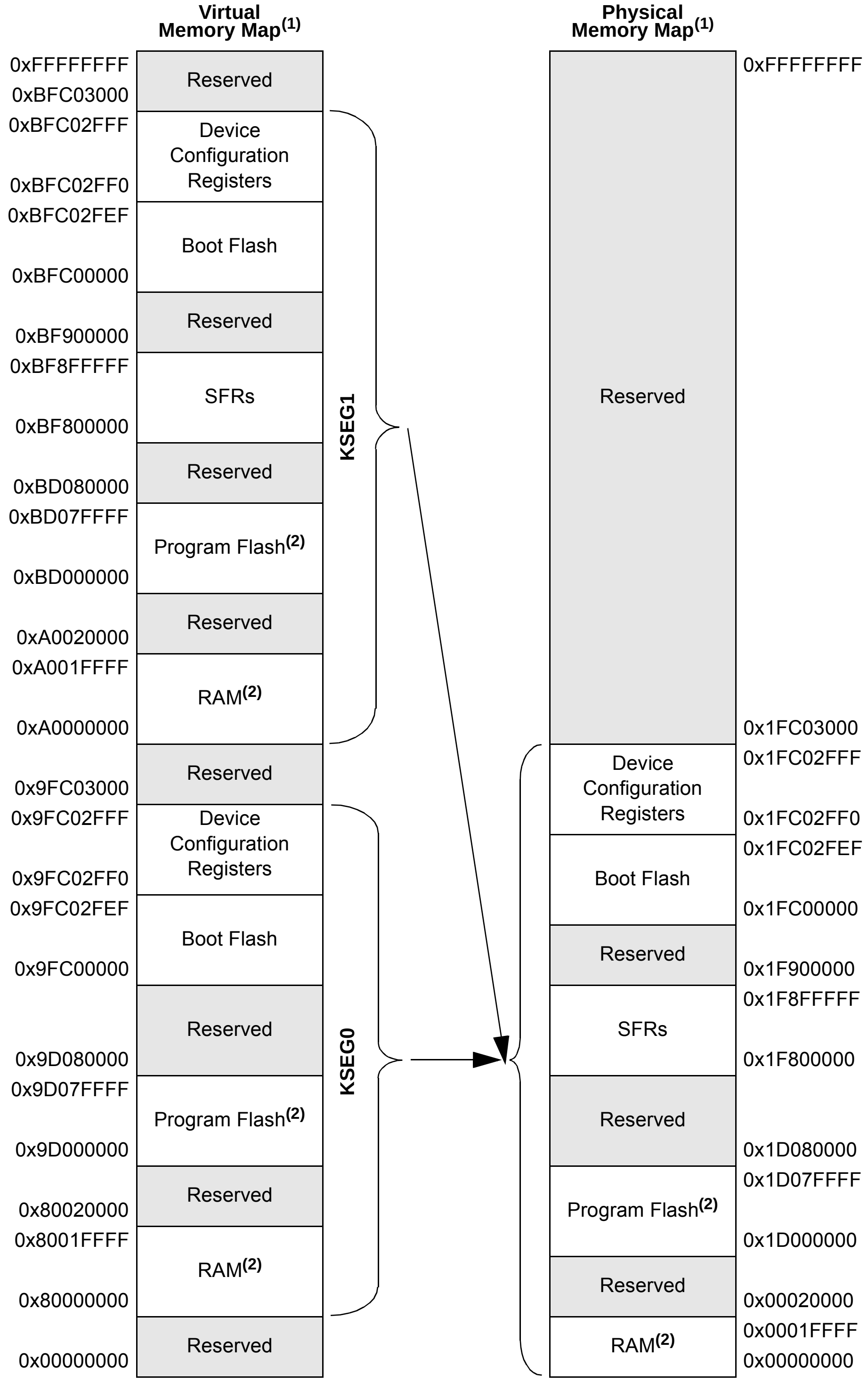
- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

4.1 Memory Layout

PIC32MX330/350/370/430/450/470 microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX330/350/370/430/450/470 devices are illustrated in Figure 4-1 through Figure 4-4.

FIGURE 4-4: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R-0	R-0	R-0	U-0	U-0	U-0
	WR	WREN	WRERR(1)	LVDERR(1)	LVDSTAT(1)	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	NVMOP<3:0>			

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘`0`’

bit 15 **WR:** Write Control bit

This bit is writable when WREN = `1` and the unlock sequence is followed.

`1` = Initiate a Flash operation. Hardware clears this bit when the operation completes
`0` = Flash operation complete or inactive

bit 14 **WREN:** Write Enable bit

`1` = Enable writes to WR bit and enables LVD circuit
`0` = Disable writes to WR bit and disables LVD circuit
This is the only bit in this register reset by a device Reset.

bit 13 **WRERR:** Write Error bit(1)

This bit is read-only and is automatically set by hardware.

`1` = Program or erase sequence did not complete successfully
`0` = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit (LVD circuit must be enabled)(1)

This bit is read-only and is automatically set by hardware.

`1` = Low-voltage detected (possible data corruption, if WRERR is set)
`0` = Voltage level is acceptable for programming

bit 11 **LVDSTAT:** Low-Voltage Detect Status bit (LVD circuit must be enabled)(1)

This bit is read-only and is automatically set, and cleared, by hardware.

`1` = Low-voltage event active
`0` = Low-voltage event NOT active

bit 10-4 **Unimplemented:** Read as ‘`0`’

bit 3-0 **NVMOP<3:0>:** NVM Operation bits

These bits are writable when WREN = `0`.

`1111` = Reserved
•
•
•
`0111` = Reserved
`0110` = No operation
`0101` = Program Flash (PFM) erase operation: erases PFM, if all pages are not write-protected
`0100` = Page erase operation: erases page selected by NVMADDR, if it is not write-protected
`0011` = Row program operation: programs row selected by NVMADDR, if it is not write-protected
`0010` = No operation
`0001` = Word program operation: programs word selected by NVMADDR, if it is not write-protected
`0000` = No operation

Note 1: This bit is cleared by setting NVMOP = `0000`, and initiating a Flash operation (i.e., WR).

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST[1]

Legend:	HC = Cleared by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as ‘`0`’

bit 0 **SWRST:** Software Reset Trigger bit[1]

`1` = Enable software Reset event
`0` = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 6. “Oscillator”** (DS60001112) in the *“PIC32 Family Reference Manual”* for details.

REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(1)

`1111` = Reserved; do not use
•
•
•
`1001` = Reserved; do not use
`1000` = REFCLKI
`0111` = System PLL output
`0110` = USB PLL output
`0101` = SOSC
`0100` = LPRC
`0011` = FRC
`0010` = POSC
`0001` = PBCLK
`0000` = SYSCLK

Note 1: The ROSEL and RODIV bits should not be written while the ACTIVE bit is ‘`1`’, as undefined behavior may result.

2: This bit is ignored when the ROSEL<3:0> bits = `0000` or `0001`.

3: While the ON bit is set to ‘`1`’, writes to these bits do not take effect until the DIVSWEN bit is also set to ‘`1`’.

9.0 PREFETCH CACHE

> **Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Prefetch Cache"** (DS60001119), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

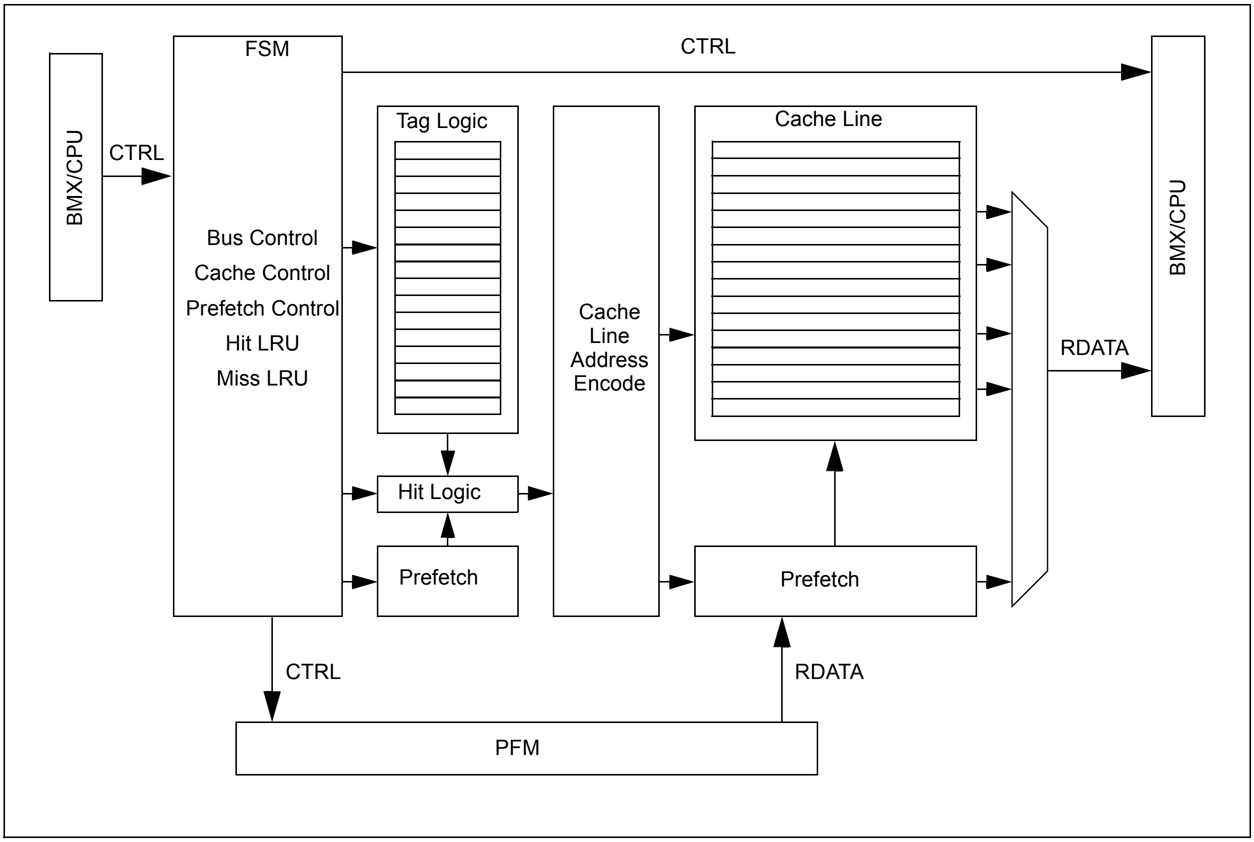
Prefetch cache increases performance for applications executing out of the cacheable program Flash memory regions by implementing instruction caching, constant data caching and instruction prefetching.

9.1 Features

- 16 fully associative lockable cache lines
- 16-byte cache lines
- Up to four cache lines allocated to data
- Two cache lines with address mask to hold repeated instructions
- Pseudo LRU replacement policy
- All cache lines are software writable
- 16-byte parallel memory fetch
- Predictive instruction prefetch

A simplified block diagram of the Prefetch Cache module is illustrated in Figure 9-1.

FIGURE 9-1: PREFETCH CACHE MODULE BLOCK DIAGRAM



REGISTER 9-4: CHEMSK: CACHE TAG MASK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LMASK<10:3>							
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	LMASK<2:0>			—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Write ‘`0`’; ignore read

bit 15-5 **LMASK<10:0>:** Line Mask bits

`1` = Enables mask logic to force a match on the corresponding bit position in the LTAG<19:0> bits (CHETAG<23:4>) and the physical address.

`0` = Only writeable for values of CHEIDX<3:0> bits (CHEACC<3:0>) equal to 0x0A and 0x0B. Disables mask logic.

bit 4-0 **Unimplemented:** Write ‘`0`’; ignore read

REGISTER 9-5: CHEW0: CACHE WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEW0<31:0>:** Word 0 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>)
Readable only if the device is not code-protected.

TABLE 12-17: PERIPHERAL PIN SELECT INPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FA04	INT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT1R<3:0>				0000
FA08	INT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT2R<3:0>				0000
FA0C	INT3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT3R<3:0>				0000
FA10	INT4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT4R<3:0>				0000
FA18	T2CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T2CKR<3:0>				0000
FA1C	T3CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T3CKR<3:0>				0000
FA20	T4CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T4CKR<3:0>				0000
FA24	T5CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T5CKR<3:0>				0000
FA28	IC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC1R<3:0>				0000
FA2C	IC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC2R<3:0>				0000
FA30	IC3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC3R<3:0>				0000
FA34	IC4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC4R<3:0>				0000
FA38	IC5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC5R<3:0>				0000
FA48	OCFAR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	OCFAR<3:0>				0000
FA50	U1RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1RXR<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

REGISTER 19-1: I2CxCON: I^{2}C CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend: HC = Cleared in Hardware
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** I^{2}C Enable bit(1)
1 = Enables the I^{2}C module and configures the SDA and SCL pins as serial port pins
0 = Disables the I^{2}C module; all I^{2}C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I^{2}C slave)
1 = Release SCLx clock
0 = Hold SCLx clock low (clock stretch)

If STREN = 1:
Bit is R/W (i.e., software can write ‘0’ to initiate stretch and write ‘1’ to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:
Bit is R/S (i.e., software can only write ‘1’ to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I^{2}C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
0 = Strict I^{2}C Reserved Address Rule is not enabled

bit 10 **A10M:** 10-bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enable I/O pin thresholds compliant with SMBus specification
0 = Disable SMBus input thresholds

Note 1: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

27.0 POWER-SAVING FEATURES

> **Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX330/350/370/430/450/470 family of devices. These PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

27.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- SOSC Run mode: the CPU is clocked from the SOSC clock source.

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

27.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- POSC Idle mode: the system clock is derived from the POSC. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- SOSC Idle mode: the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

27.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

27.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is Halted.
- The system clock source is typically shutdown. See **Section 27.3.3 "Peripheral Bus Scaling Method"** for specific information.
- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit remains operative during Sleep mode.
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode.
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption.

TABLE 31-12: DC CHARACTERISTICS: PROGRAM MEMORY[3]

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical[1]**	**Max.**	**Units**	**Conditions**
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
D138	TWW	Word Write Cycle Time[4]	44	—	59	µs	—
D136	TRW	Row Write Cycle Time[2,4]	2.8	3.3	3.8	ms	—
D137	TPE	Page Erase Cycle Time[4]	22	—	29	ms	—
D139	TCE	Chip Erase Cycle Time[4]	86	—	116	ms	—

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 8 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to the *“PIC32 Flash Programming Specification”* (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on the FRC accuracy (see Table 31-20) and the FRC tuning values (see Register 8-2).

TABLE 31-13: DC CHARACTERISTICS: PROGRAM FLASH MEMORY WAIT STATE

DC CHARACTERISTICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp		
Required Flash Wait States	**SYSCLK**	**Units**	**Conditions**
0 Wait State	0-40	MHz	-40ºC to +85ºC
	0-30	MHz	-40ºC to +105ºC
1 Wait State	41-80	MHz	-40ºC to +85ºC
	31-60	MHz	-40ºC to +105ºC
2 Wait States	81-100	MHz	-40ºC to +85ºC
	61-80	MHz	-40ºC to +105ºC
3 Wait States	101-120	MHz	0ºC to +70ºC

TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

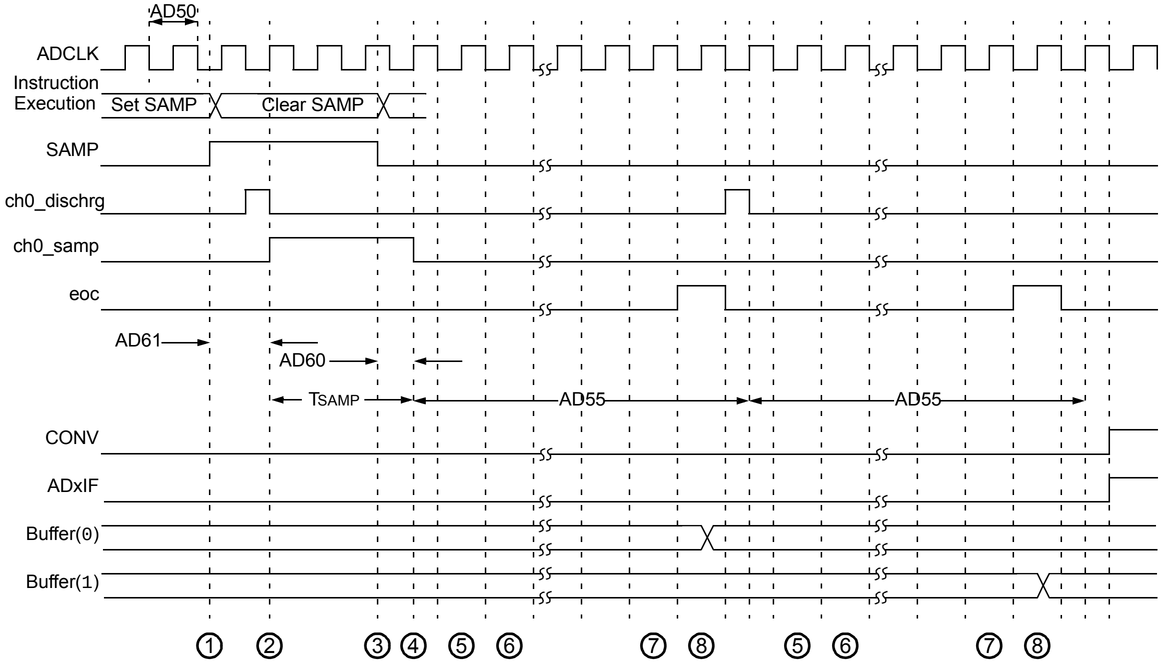
AC CHARACTERISTICS				**Standard Operating Conditions: 2.3V to 3.6V** **(unless otherwise stated)** Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	—
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	—
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 2)**	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	µs	—
			400 kHz mode	TPB * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	µs	

Note 1: BRG is the value of the I^{2}C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

FIGURE 31-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = `0`, SSRC<2:0> = `000`)



① – Software sets ADxCON. SAMP to start sampling.

② – Sampling starts after discharge period. TSAMP is described in **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104) in the *“PIC32 Family Reference Manual”*.

③ – Software clears ADxCON. SAMP to start conversion.

④ – Sampling ends, conversion sequence starts.

⑤ – Convert bit 9.

⑥ – Convert bit 8.

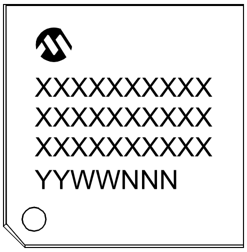
⑦ – Convert bit 0.

⑧ – One TAD for end of conversion.

33.0 PACKAGING INFORMATION

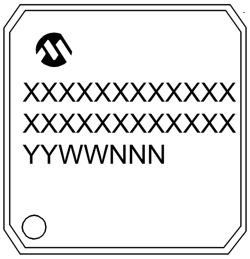
33.1 Package Marking Information

64-Lead TQFP (10x10x1 mm)



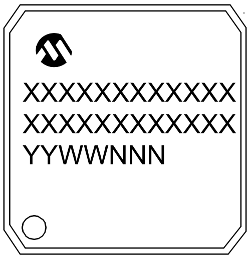
Example

100-Lead TQFP (14x14x1 mm)



Example

100-Lead TQFP (12x12x1 mm)



Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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ISBN: 978-1-5224-0959-5