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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx470f512lt-i-pf

PIC32MX330/350/370/430/450/470

NOTES:

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2.11 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-6, Figure 2-7, and Figure 2-8.

FIGURE 2-6: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION

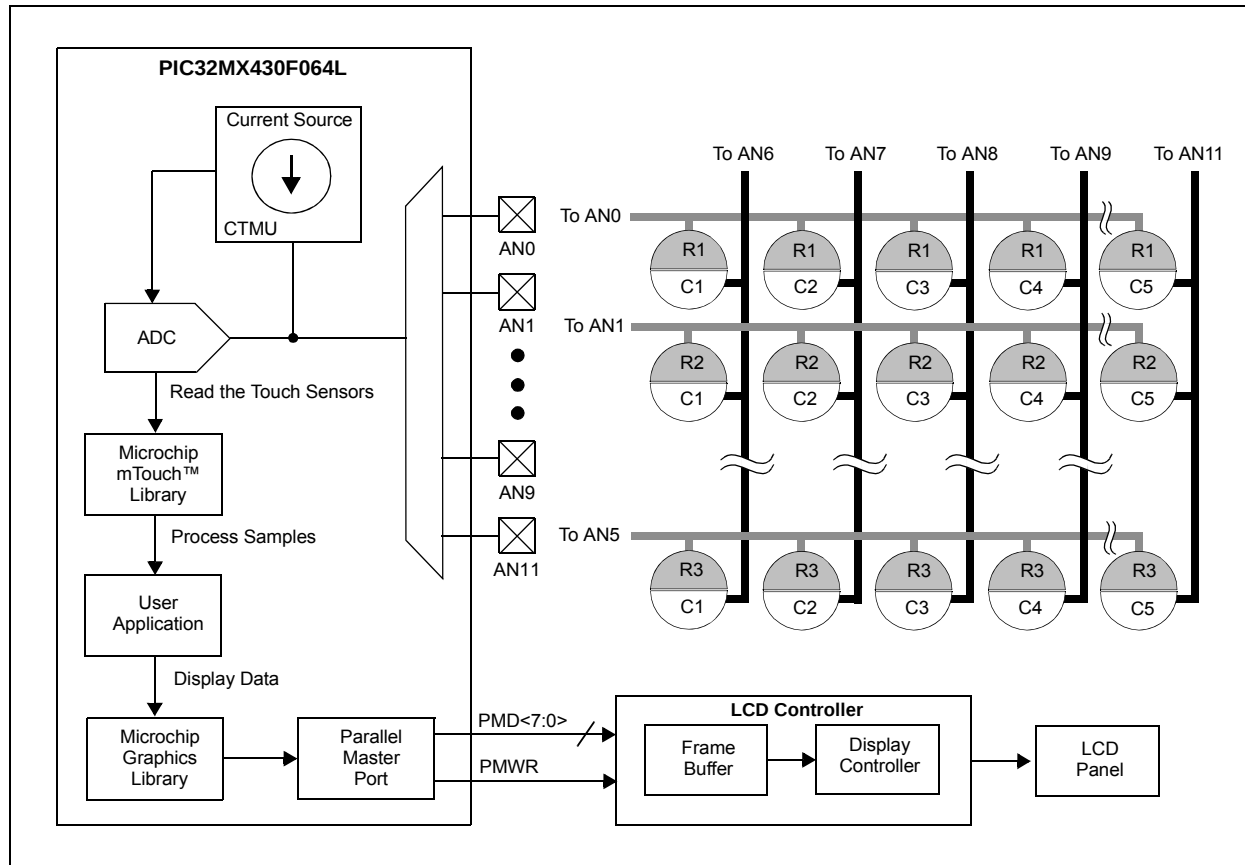
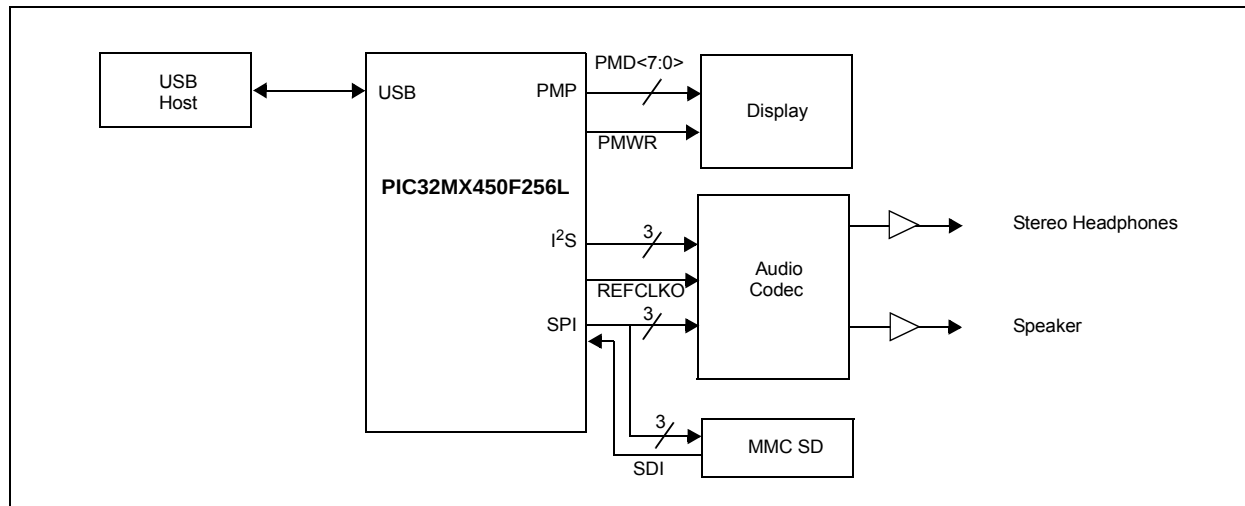
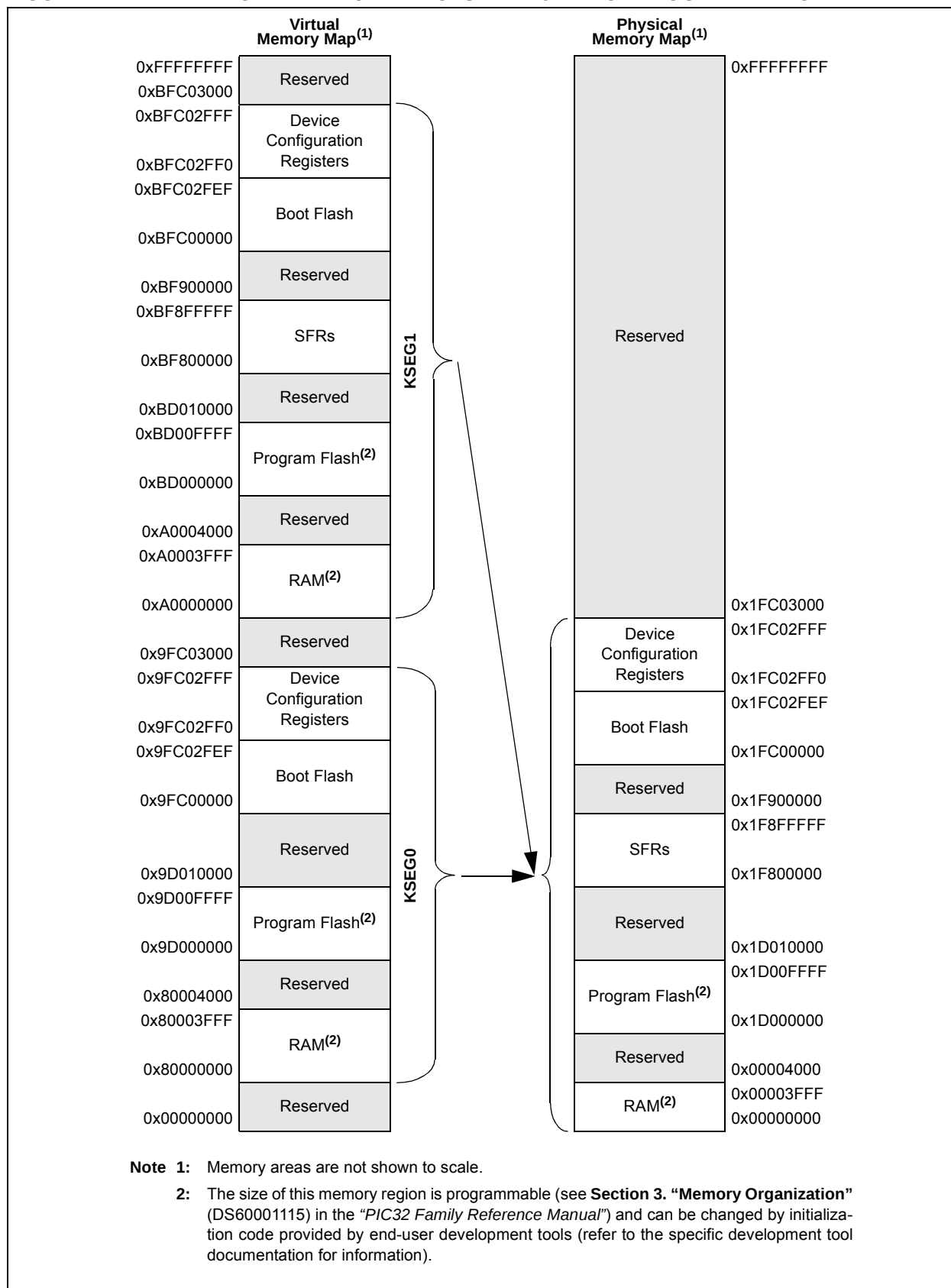


FIGURE 2-7: AUDIO PLAYBACK APPLICATION



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FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 64 KB OF PROGRAM MEMORY



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NOTES:

10.1 Control Registers

TABLE 10-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	0000	
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	RDWR	DMACH<2:0>			0000	
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 10-2: DMA CRC REGISTER MAP

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
3030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>		0000
3040	DCRCDATA	31:16	DCRCDATA<31:0>															0000
		15:0																0000
3050	DCRCXOR	31:16	DCRCXOR<31:0>															0000
		15:0																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 11-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.
- 2: This register does not have associated SET and INV registers.
- 3: This register does not have associated CLR, SET and INV registers.
- 4: Reset value for this bit is undefined.

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TABLE 12-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPN Pin Selection
INT1	INT1R	INT1R<3:0>	0000 = RPD1 0001 = RPG9
T3CK	T3CKR	T3CKR<3:0>	0010 = RPB14 0011 = RPD0
IC1	IC1R	IC1R<3:0>	0100 = RPD8 0101 = RPB6
$\overline{\text{U3CTS}}$	U3CTSR	U3CTSR<3:0>	0110 = RPD5 0111 = RPB2
U4RX	U4RXR	U4RXR<3:0>	1000 = RPF3 ⁽⁴⁾ 1001 = RPF13 ⁽³⁾
U5RX	U5RXR ⁽³⁾	U5RXR<3:0>	1010 = Reserved 1011 = RPF2 ⁽¹⁾
$\overline{\text{SS2}}$	SS2R	SS2R<3:0>	1100 = RPC2 ⁽³⁾ 1101 = RPE8 ⁽³⁾
OCFA	OCFAR	OCFAR<3:0>	1110 = Reserved 1111 = Reserved

- Note 1:** This selection is not available on 64-pin USB devices.
Note 2: This selection is only available on 100-pin General Purpose devices.
Note 3: This selection is not available on 64-pin USB and General Purpose devices.
Note 4: This selection is only available on General Purpose devices.

15.0 WATCHDOG TIMER (WDT)

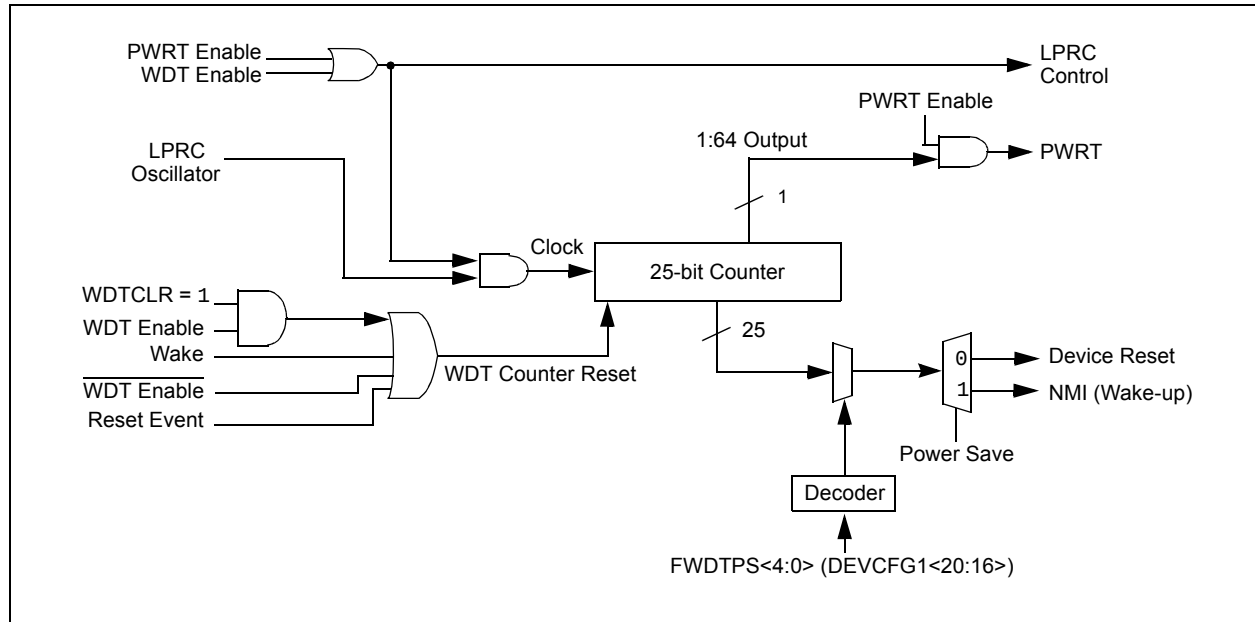
Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog, Deadman, and Power-up Timers”** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 15-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM



17.1 Control Registers

TABLE 17-1: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 5 REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3010	OC1R	31:16	OC1R<31:0>																XXXX
		15:0																	XXXX
3020	OC1RS	31:16	OC1RS<31:0>																XXXX
		15:0																	XXXX
3200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3210	OC2R	31:16	OC2R<31:0>																XXXX
		15:0																	XXXX
3220	OC2RS	31:16	OC2RS<31:0>																XXXX
		15:0																	XXXX
3400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3410	OC3R	31:16	OC3R<31:0>																XXXX
		15:0																	XXXX
3420	OC3RS	31:16 15:0	OC3RS<31:0>																XXXX XXXX
3600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3610	OC4R	31:16	OC4R<31:0>																XXXX
		15:0																	XXXX
3620	OC4RS	31:16	OC4RS<31:0>																XXXX
		15:0																	XXXX
3800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3810	OC5R	31:16 15:0	OC5R<31:0>																XXXX XXXX
3820	OC5RS	31:16	OC5RS<31:0>																XXXX
		15:0																	XXXX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 “CLR, SET, and INV Registers” for more information.

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REGISTER 21-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 5-2 **WAITM<3:0>**: Data Read/Write Strobe Wait States bits⁽¹⁾

1111 = Wait of 16 TPB

•
•
•

0001 = Wait of 2 TPB

0000 = Wait of 1 TPB (default)

bit 1-0 **WAITE<1:0>**: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾

11 = Wait of 4 TPB

10 = Wait of 3 TPB

01 = Wait of 2 TPB

00 = Wait of 1 TPB (default)

For Read operations:

11 = Wait of 3 TPB

10 = Wait of 2 TPB

01 = Wait of 1 TPB

00 = Wait of 0 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPB cycle for a write operation; WAITB = 1 TPB cycle, WAITE = 0 TPB cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

22.1 Control Registers

TABLE 22-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
0200	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>									0000	
		15:0	ON	—	SIDL	—	—	—	—	—	RTSECSSEL	RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>							0000	
0220	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	xx00	
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx00
0240	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	xx00	
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	C2OUT	C1OUT

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in IDLE Control bit

1 = All Comparator modules are disabled in IDLE mode

0 = All Comparator modules continue to operate in the IDLE mode

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **C2OUT:** Comparator Output bit

1 = Output of Comparator 2 is a '1'

0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit

1 = Output of Comparator 1 is a '1'

0 = Output of Comparator 1 is a '0'

26.1 Control Register

TABLE 26-1: CTMU REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
A200	CTMUCON	31:16	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
		15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	ITRIM<5:0>						IRNG<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

27.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 27-1 for more information.

Note: Disabling a peripheral module while its ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TABLE 27-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral ⁽¹⁾	PMDx bit Name ⁽¹⁾	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
CTMU	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
USB ⁽²⁾	USBMD	PMD5<24>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: “PIC32MX330/350/370/430/450/470 Controller Family Features”** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

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REGISTER 28-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

- bit 11-5 **Reserved:** Write '1'
- bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits
11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved
- bit 2 **JTAGEN:** JTAG Enable bit⁽¹⁾
1 = JTAG is enabled
0 = JTAG is disabled
- bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
1x = Debugger is disabled
0x = Debugger is enabled

Note 1: This bit sets the value for the JTAGEN bit in the CFGCON register.

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REGISTER 28-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	U-0	U-0	U-0	U-0
	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P
	—	—	—	—	—	FSRSSEL<2:0>		
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 31 **FVBUSONIO:** USB VBUS_ON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function
- bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function
- bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations
- bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations
- bit 27-19 **Unimplemented:** Read as '0'
- bit 18-16 **FSRSSEL<2:0>:** Shadow Register Set Priority Select bit
These bits assign an interrupt priority to a shadow register.
111 = Shadow register set used with interrupt priority 7
110 = Shadow register set used with interrupt priority 6
101 = Shadow register set used with interrupt priority 5
100 = Shadow register set used with interrupt priority 4
011 = Shadow register set used with interrupt priority 3
010 = Shadow register set used with interrupt priority 2
001 = Shadow register set used with interrupt priority 1
000 = Shadow register set used with interrupt priority 0
- bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

31.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX330/350/370/430/450/470 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX330/350/370/430/450/470 devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	-40°C to +105°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3)	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V (Note 3)	-0.3V to +6.0V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V (Note 3)	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	-0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin(s)	200 mA
Maximum current into VDD pin(s) (Note 2)	200 mA
Maximum output current sourced/sunk by any 4x I/O pin	15 mA
Maximum output current sourced/sunk by any 8x I/O pin	25 mA
Maximum current sunk by all ports	150 mA
Maximum current sourced by all ports (Note 2)	150 mA

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

3: See the “**Device Pin Tables**” section for the 5V tolerant pins.

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TABLE 31-25: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for Commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Max.	Units	Conditions	
TB10	T _{TXH}	TxCK High Time	Synchronous, with prescaler	$[(12.5\text{ ns or }1\text{ TPB})/N]$ + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	T _{TXL}	TxCK Low Time	Synchronous, with prescaler	$[(12.5\text{ ns or }1\text{ TPB})/N]$ + 25 ns	—	ns	Must also meet parameter TB15	
TB15	T _{TXP}	TxCK Input Period	Synchronous, with prescaler	$[(\text{Greater of } [(25\text{ ns or }2\text{ TPB})/N] + 30\text{ ns})]$	—	ns	V _{DD} > 2.7V	
				$[(\text{Greater of } [(25\text{ ns or }2\text{ TPB})/N] + 50\text{ ns})]$	—	ns	V _{DD} < 2.7V	
TB20	T _{CKEXTMRL}	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPB	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 31-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS

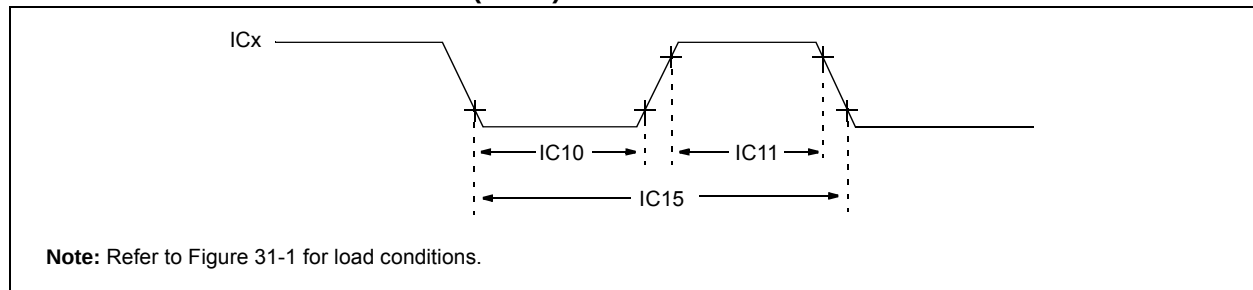


TABLE 31-26: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Max.	Units	Conditions	
IC10	TcCL	ICx Input Low Time	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	TcCH	ICx Input High Time	[(12.5 ns or 1 TPB)/N] + 25 ns	—	ns	Must also meet parameter IC15.	
IC15	TcCP	ICx Input Period	[(25 ns or 2 TPB)/N] + 50 ns	—	ns	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

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TABLE 31-31: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP52	Tsch2ssH TscL2ssH	SSx after SCKx Edge	Tsck + 20	—	—	ns	—

- Note 1:** These parameters are characterized, but not tested in manufacturing.
- 2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The minimum clock period for SCKx is 40 ns.
- 4:** Assumes 50 pF load on all SPIx pins.

32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 32-1: V_{OH} – 4x DRIVER PINS

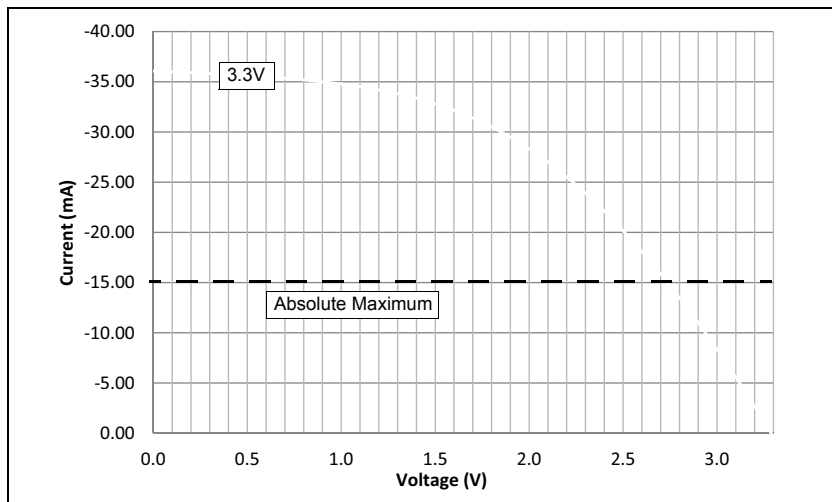


FIGURE 32-3: V_{OL} – 4x DRIVER PINS

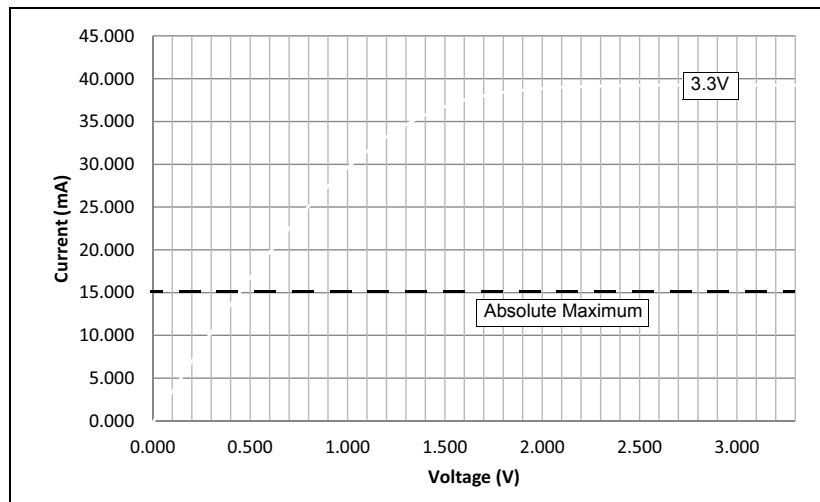


FIGURE 32-2: V_{OH} – 8x DRIVER PINS

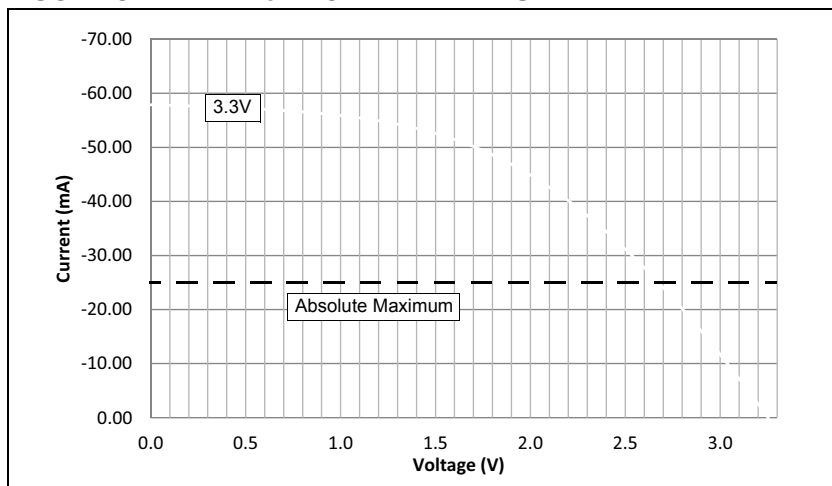


FIGURE 32-4: V_{OL} – 8x DRIVER PINS

