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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx470f512lt-v-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx470f512lt-v-pt</a>

# PIC32MX330/350/370/430/450/470

**TABLE 7: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)**

<b>124-PIN VTLA (BOTTOM VIEW)<sup>(1,2,3,4)</sup></b>  <b>PIC32MX430F064L</b> <b>PIC32MX450F128L</b> <b>PIC32MX450F256L</b> <b>PIC32MX470F512L</b>		A17  A1  Polarity Indicator	B13  B1  A68	B29  B41  A51	A34  Conductive Thermal Pad
Package Bump #	Full Pin Name	Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
B7	MCLR	B32	SDA2/RA3		
B8	Vss	B33	TDO/RA5		
B9	TMS/CTED1/RA0	B34	OSC1/CLK1/RC12		
B10	RPE9/RE9	B35	No Connect		
B11	AN4/C1INB/RB4	B36	SCL1/RPA14/RA14		
B12	Vss	B37	RPD8/RTCC/RD8		
B13	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	B38	RPD10/SCK1/PMCS2/RD10		
B14	PGED1/AN0/RPB0/RB0	B39	RPD0/INT0/RD0		
B15	No Connect	B40	SOSCO/RPC14/T1CK/RC14		
B16	PGED2/AN7/RPB7/CTED3/RB7	B41	Vss		
B17	VREF+/CVREF+/PMA6/RA10	B42	AN25/RPD2/RD2		
B18	AVss	B43	RPD12/PMD12/RD12		
B19	AN9/RPB9/CTED4/RB9	B44	RPD4/PMWR/RD4		
B20	AN11/PMA12/RB11	B45	PMD14/RD6		
B21	VDD	B46	No Connect		
B22	RPF13/RF13	B47	No Connect		
B23	AN12/PMA11/RB12	B48	VCAP		
B24	AN14/RPB14/CTED5/PMA1/RB14	B49	RPF0/PMD11/RF0		
B25	Vss	B50	RPG1/PMD9/RG1		
B26	RPD14/RD14	B51	TRCLK/RA6		
B27	RPF4/PMA9/RF4	B52	PMD0/RE0		
B28	No Connect	B53	VDD		
B29	RPF8/RF8	B54	TRD2/RG14		
B30	VUSB3v3	B55	TRD0/RG13		
B31	D+	B56	RPE3/CTPLS/PMD3/RE3		

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 “Peripheral Pin Select”** for restrictions.
  - 2: Every I/O port pin (RAX-RGX) can be used as a change notification pin (CNAX-CNGX). See **Section 12.0 “I/O Ports”** for more information.
  - 3: Shaded package bumps are 5V tolerant.
  - 4: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

# PIC32MX330/350/370/430/450/470

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA			
IC1	PPS	PPS	PPS	I	ST	Capture Input 1-5
IC2	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	I	ST	
OC1	PPS	PPS	PPS	O	ST	Output Compare Output 1
OC2	PPS	PPS	PPS	O	ST	Output Compare Output 2
OC3	PPS	PPS	PPS	O	ST	Output Compare Output 3
OC4	PPS	PPS	PPS	O	ST	Output Compare Output 4
OC5	PPS	PPS	PPS	O	ST	Output Compare Output 5
OCFA	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	A29	I	ST	Output Compare Fault B Input
INT0	35 <sup>(1)</sup> , 46 <sup>(2)</sup>	55 <sup>(1)</sup> , 72 <sup>(2)</sup>	B30 <sup>(1)</sup> , B39 <sup>(2)</sup>	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	I	ST	External Interrupt 4
RA0	—	17	B9	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	A26	I/O	ST	
RA2	—	58	A39	I/O	ST	
RA3	—	59	B32	I/O	ST	
RA4	—	60	A40	I/O	ST	
RA5	—	61	B33	I/O	ST	
RA6	—	91	B51	I/O	ST	
RA7	—	92	A62	I/O	ST	
RA9	—	28	A21	I/O	ST	
RA10	—	29	B17	I/O	ST	
RA14	—	66	B36	I/O	ST	
RA15	—	67	A44	I/O	ST	

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
TTL = TTL input buffer

**Note 1:** This pin is only available on devices without a USB module.  
**2:** This pin is only available on devices with a USB module.  
**3:** This pin is not available on 64-pin devices.

# PIC32MX330/350/370/430/450/470

## REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	BMXDUDBA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BMXDUDBA<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUDBA<15:10>:** DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 **BMXDUDBA<9:0>:** Read-Only bits

Value is always '0', which forces 1 KB increments

- Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.
- 2:** The value in this register must be less than or equal to BMXDRMSZ.

## 5.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. “Flash Program Memory”** (DS60001121), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

PIC32MX330/350/370/430/450/470 devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. “Flash Program Memory”** (DS60001121) in the *“PIC32 Family Reference Manual”*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *“PIC32 Flash Programming Specification”* (DS60001145), which can be downloaded from the Microchip web site.

**Note:** On PIC32MX330/350/370/430/450/470 devices, the Flash page size is 4 KB and the row size is 512 bytes (1024 IW and 128 IW, respectively).

# PIC32MX330/350/370/430/450/470

**REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	SS0
15:8	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	MVEC	—	TPC<2:0>		
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-17 **Unimplemented:** Read as '0'

bit 16 **SS0:** Single Vector Shadow Register Set bit

1 = Single vector is presented with a shadow register set

0 = Single vector is not presented with a shadow register set

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multi Vector Configuration bit

1 = Interrupt controller configured for multi vectored mode

0 = Interrupt controller configured for single vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits

111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer

110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer

101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer

100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer

011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer

010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer

001 = Interrupts of group priority 1 start the Interrupt Proximity timer

000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit

1 = Rising edge

0 = Falling edge

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**REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS9	IFS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS7	IFS6	IFS5	IFS4	IFS3	IFS2	IFS1	IFS0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IFS31-IFS0:** Interrupt Flag Status bits

1 = Interrupt request has occurred

0 = No interrupt request has occurred

**Note:** This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

**REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IEC31-IEC0:** Interrupt Enable bits

1 = Interrupt is enabled

0 = Interrupt is disabled

**Note:** This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

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## REGISTER 9-12: CHEPFABT: PREFETCH CACHE ABORT STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEPFABT<31:0>**: Prefab Abort Count bits

Incremented each time an automatic prefetch cache is aborted due to a non-sequential instruction fetch, load or store.



# PIC32MX330/350/370/430/450/470

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## REGISTER 11-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1    **PPBRST:** Ping-Pong Buffers Reset bit  
1 = Reset all Even/Odd buffer pointers to the EVEN BD banks  
0 = Even/Odd buffer pointers not being Reset
- bit 0    **USBEN:** USB Module Enable bit<sup>(4)</sup>  
1 = USB module and supporting circuitry is enabled  
0 = USB module and supporting circuitry is disabled
- SOFEN:** SOF Enable bit<sup>(5)</sup>  
1 = SOF token sent every 1 ms  
0 = SOF token is disabled

- Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).
- 2:** All host control logic is reset any time that the value of this bit is toggled.
- 3:** Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
- 4:** Device mode.
- 5:** Host mode.

## 12.0 I/O PORTS

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. “I/O Ports”** (DS60001120), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

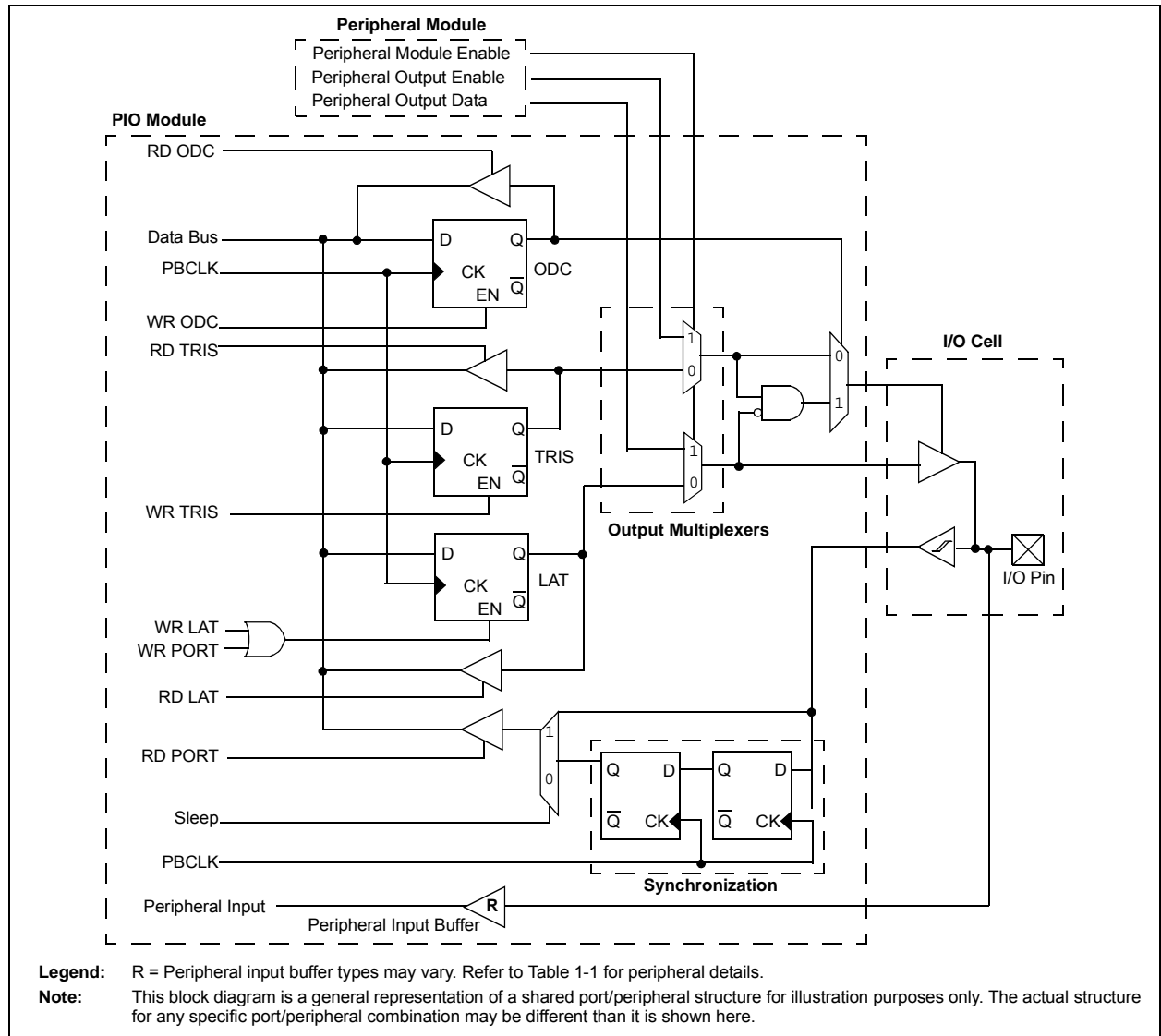
Following are key features of this module:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

**FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE**



## 12.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only options.

Peripheral pin select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The peripheral pin select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. Peripheral pin select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

### 12.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the peripheral pin select feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable port number.

### 12.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the peripheral pin select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the peripheral pin select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I<sup>2</sup>C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

### 12.3.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral pin select features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

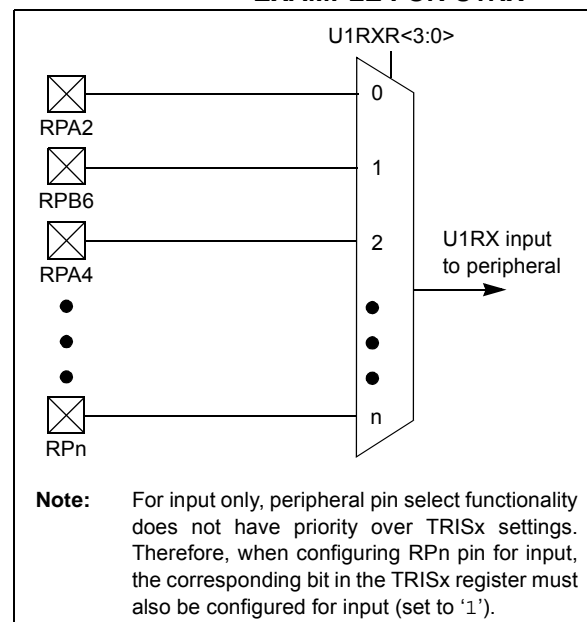
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

### 12.3.4 INPUT MAPPING

The inputs of the peripheral pin select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [pin name]R registers, where [pin name] refers to the peripheral pins listed in Table 12-1, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-1.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

**FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX**



**TABLE 12-12: PORTF REGISTER MAP FOR PIC32MX430F064L, PIC32MX450F128L, PIC32MX450F256L, AND PIC32MX470F512L DEVICES ONLY**

Virtual Address (BF88_#)	Register Name(!)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	xxxxx
6520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	—	—	RF5	RF4	RF3	RF2	RF1	RF0	xxxxx
6530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxxx
6540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	—	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	xxxxx
6550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPUF13	CNPUF12	—	—	—	CNPUF8	—	—	CNPUF5	CNPUF4	CNPUDF3	CNPUF2	CNPUF1	CNPUF0	xxxxx
6560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPDF13	CNPDF12	—	—	—	CNPDF8	—	—	CNPDF5	CNPFF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	xxxxx
6570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNIEF13	CNIEF12	—	—	—	CNIEF8	—	—	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	xxxxx
6590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CN STATF13	CN STATF12	—	—	—	CN STATF8	—	—	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	xxxxx

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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## REGISTER 18-3: SPIxSTAT: SPI STATUS REGISTER (CONTINUED)

- bit 3     **SPITBE:** SPI Transmit Buffer Empty Status bit  
1 = Transmit buffer, SPIxTXB is empty  
0 = Transmit buffer, SPIxTXB is not empty  
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.  
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.
- bit 2     **Unimplemented:** Read as '0'
- bit 1     **SPITBF:** SPI Transmit Buffer Full Status bit  
1 = Transmit not yet started, SPITXB is full  
0 = Transmit buffer is not full  
Standard Buffer Mode:  
Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.  
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPIxSR.  
Enhanced Buffer Mode:  
Set when CWPTR + 1 = SRPTR; cleared otherwise
- bit 0     **SPIRBF:** SPI Receive Buffer Full Status bit  
1 = Receive buffer, SPIxRXB is full  
0 = Receive buffer, SPIxRXB is not full  
Standard Buffer Mode:  
Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.  
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.  
Enhanced Buffer Mode:  
Set when SWPTR + 1 = CRPTR; cleared otherwise

## 19.0 INTER-INTEGRATED CIRCUIT (I<sup>2</sup>C)

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I<sup>2</sup>C)”** (DS60001116), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The I<sup>2</sup>C module provides complete hardware support for both Slave and Multi-Master modes of the I<sup>2</sup>C serial communication standard. Figure 19-1 illustrates the I<sup>2</sup>C module block diagram.

Each I<sup>2</sup>C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I<sup>2</sup>C module offers the following key features:

- I<sup>2</sup>C interface supporting both master and slave operation
- I<sup>2</sup>C Slave mode supports 7-bit and 10-bit addressing
- I<sup>2</sup>C Master mode supports 7-bit and 10-bit addressing
- I<sup>2</sup>C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I<sup>2</sup>C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I<sup>2</sup>C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

## REGISTER 19-1: I2CxCON: I<sup>2</sup>C CONTROL REGISTER (CONTINUED)

- bit 7     **GCEN:** General Call Enable bit (when operating as I<sup>2</sup>C slave)  
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)  
0 = General call address disabled
- bit 6     **STREN:** SCLx Clock Stretch Enable bit (when operating as I<sup>2</sup>C slave)  
Used in conjunction with SCLREL bit.  
1 = Enable software or receive clock stretching  
0 = Disable software or receive clock stretching
- bit 5     **ACKDT:** Acknowledge Data bit (when operating as I<sup>2</sup>C master, applicable during master receive)  
Value that is transmitted when the software initiates an Acknowledge sequence.  
1 = Send NACK during Acknowledge  
0 = Send ACK during Acknowledge
- bit 4     **ACKEN:** Acknowledge Sequence Enable bit  
(when operating as I<sup>2</sup>C master, applicable during master receive)  
1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit.  
Hardware clear at end of master Acknowledge sequence.  
0 = Acknowledge sequence not in progress
- bit 3     **RCEN:** Receive Enable bit (when operating as I<sup>2</sup>C master)  
1 = Enables Receive mode for I<sup>2</sup>C. Hardware clear at end of eighth bit of master receive data byte.  
0 = Receive sequence not in progress
- bit 2     **PEN:** Stop Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.  
0 = Stop condition not in progress
- bit 1     **RSEN:** Repeated Start Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence.  
0 = Repeated Start condition not in progress
- bit 0     **SEN:** Start Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.  
0 = Start condition not in progress

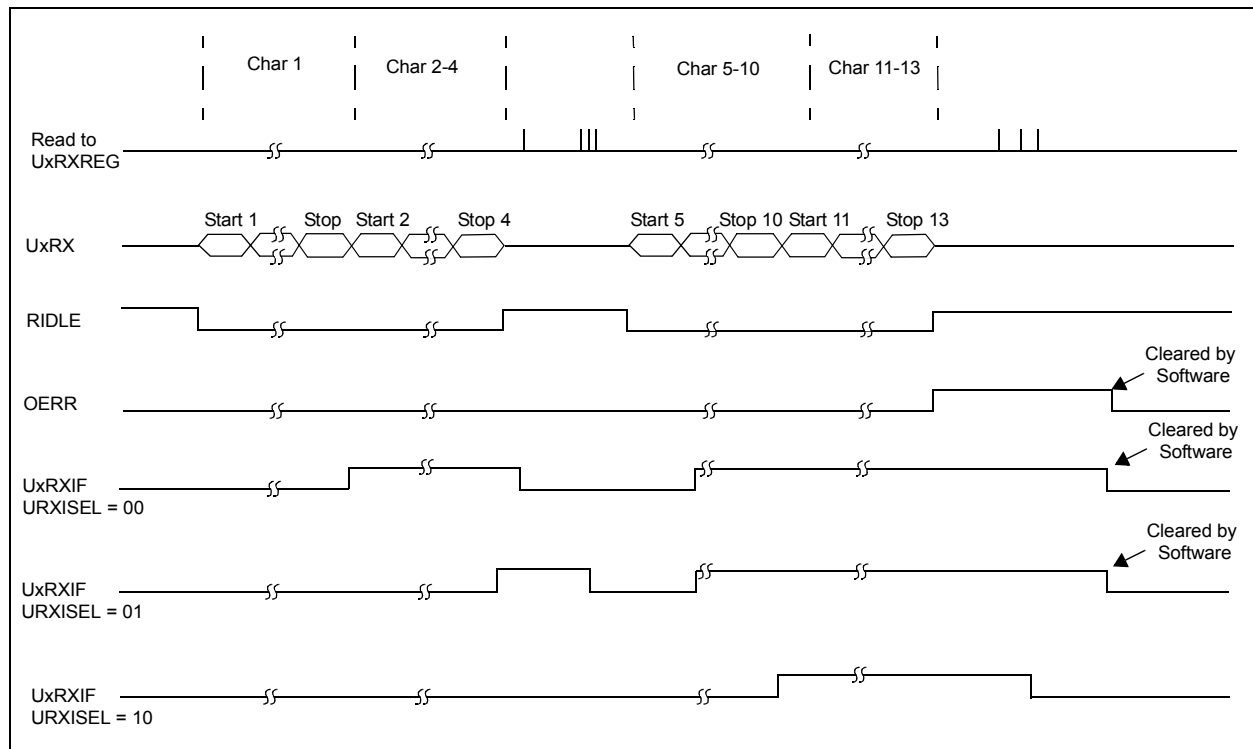
**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

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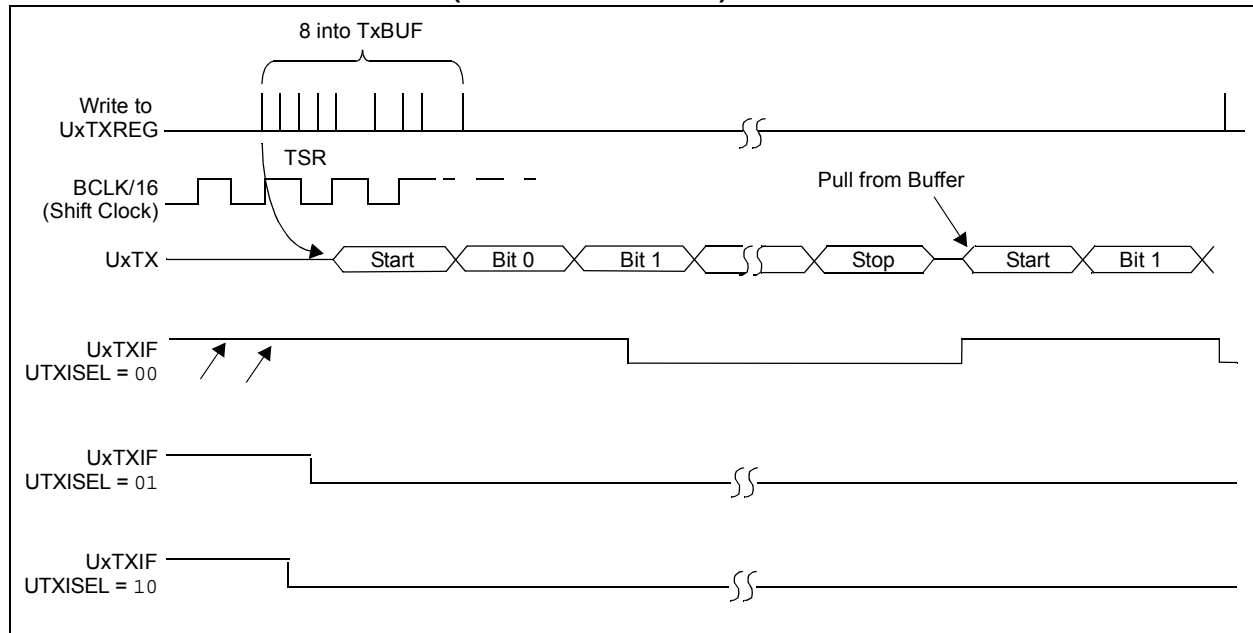
## 20.2 Timing Diagrams

Figure 20-2 and Figure 20-3 illustrate typical receive and transmit timing for the UART module.

**FIGURE 20-2: UART RECEPTION**



**FIGURE 20-3: TRANSMISSION (8-BIT OR 9-BIT DATA)**





## 24.1 Control Registers

**TABLE 24-1: COMPARATOR REGISTER MAP**

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		E1C3
A010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		E1C3
A060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

**Legend:** × = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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**TABLE 31-14: COMPARATOR SPECIFICATIONS**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D300	V <sub>IOFF</sub>	Input Offset Voltage	—	±7.5	±25	mV	AVDD = VDD, AVSS = VSS
D301	V <sub>ICM</sub>	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS (Note 2)
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max V <sub>ICM</sub> = (VDD - 1)V (Note 2)
D303	T <sub>RESP</sub>	Response Time	—	150	400	ns	AVDD = VDD, AVSS = VSS (Notes 1,2)
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	μs	Comparator module is configured before setting the comparator ON bit (Note 2)
D305	IVREF	Internal Voltage Reference	1.14	1.2	1.26	V	—

**Note 1:** Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

**2:** These parameters are characterized but not tested.

**3:** Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

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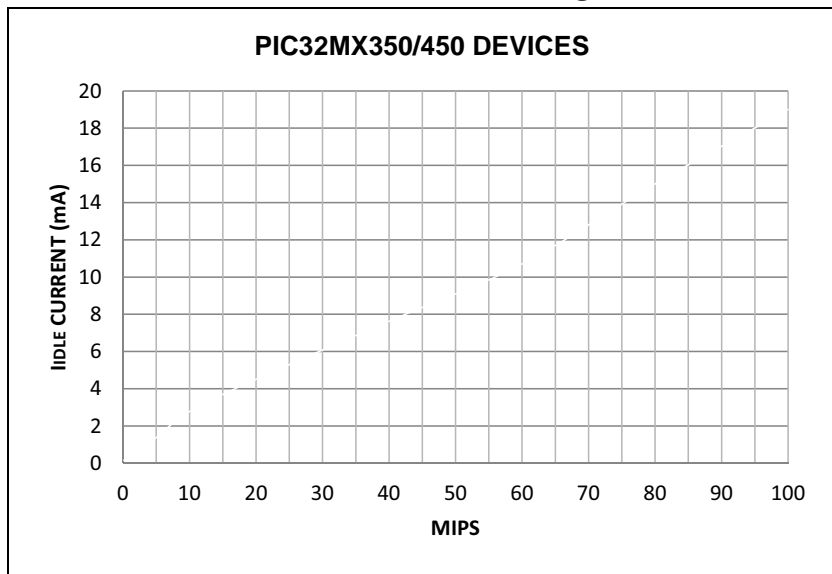
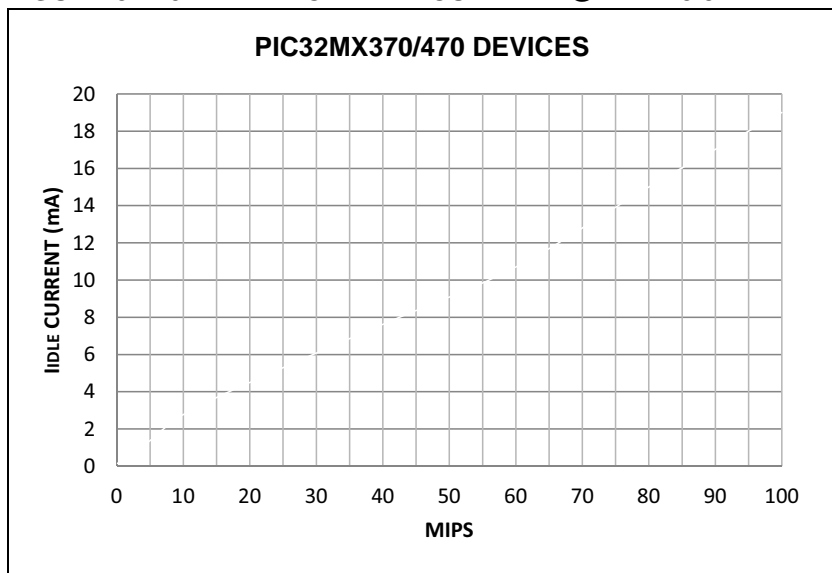
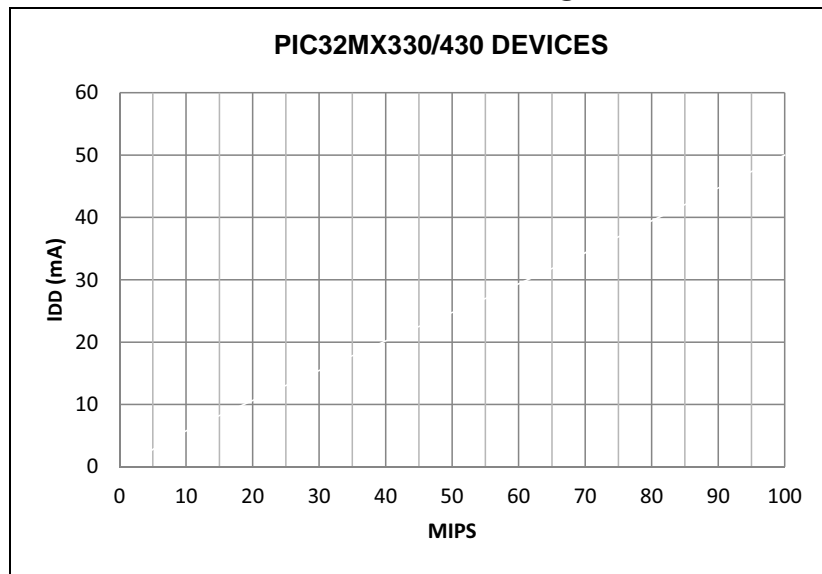
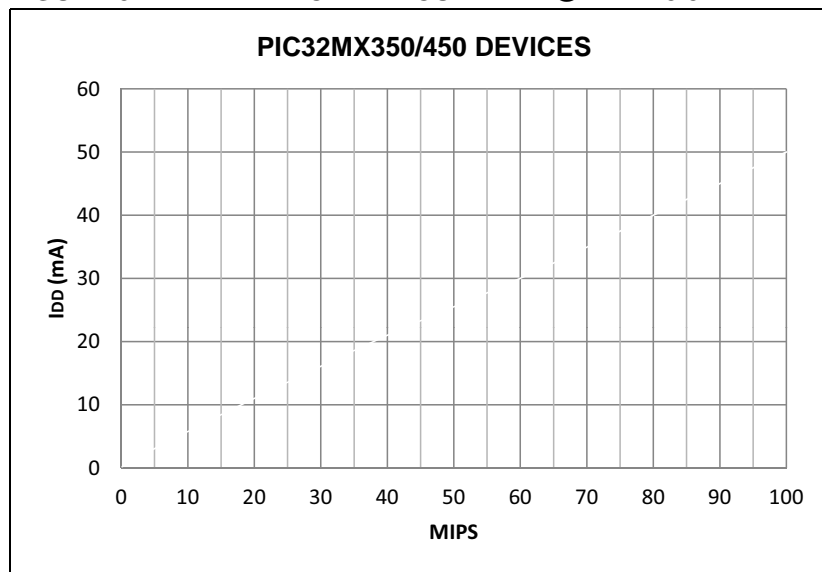
**TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics		Min. <sup>(1)</sup>	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TPB * (BRG + 2)	—	μs	—
			400 kHz mode	TPB * (BRG + 2)	—	μs	—
			1 MHz mode (Note 2)	TPB * (BRG + 2)	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	TPB * (BRG + 2)	—	μs	—
			400 kHz mode	TPB * (BRG + 2)	—	μs	—
			1 MHz mode (Note 2)	TPB * (BRG + 2)	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode (Note 2)	—	100	ns	
IM21	Tr:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode (Note 2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 2)	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	TPB * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPB * (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	TPB * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPB * (BRG + 2)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPB * (BRG + 2)	—	μs	—
			400 kHz mode	TPB * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPB * (BRG + 2)	—	μs	

**Note 1:** BRG is the value of the I<sup>2</sup>C Baud Rate Generator.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

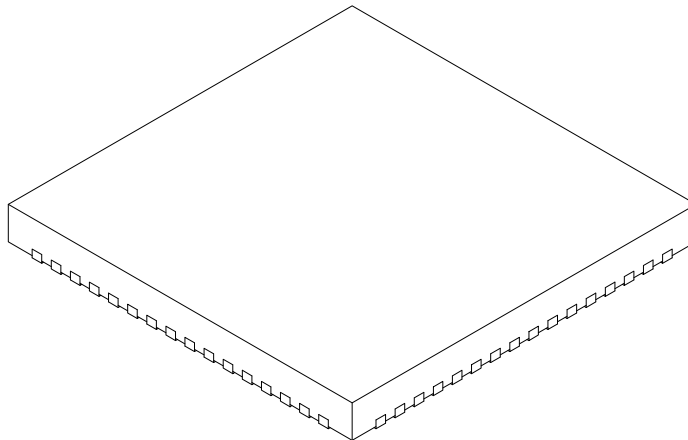
**3:** The typical value for this parameter is 104 ns.

**FIGURE 32-9: TYPICAL  $I_{IDLE}$  CURRENT @  $V_{DD} = 3.3V$** **FIGURE 32-10: TYPICAL  $I_{IDLE}$  CURRENT @  $V_{DD} = 3.3V$** **FIGURE 32-11: TYPICAL  $I_{DD}$  CURRENT @  $V_{DD} = 3.3V$** **FIGURE 32-12: TYPICAL  $I_{DD}$  CURRENT @  $V_{DD} = 3.3V$** 

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## 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2