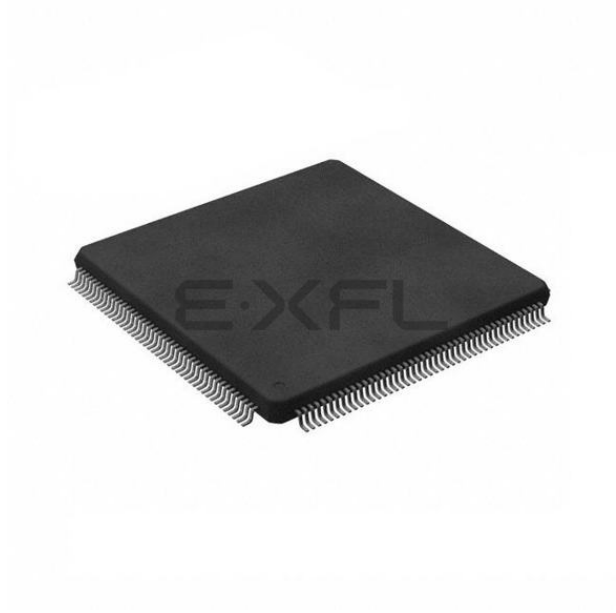
Infineon Technologies - MB9DF125EPMC-GSK5E2 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-R4
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	141
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 5.5V
Data Converters	A/D 50x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9df125epmc-gsk5e2

Table 18. Port Pin Multiplexing (Continued)

Register (offset)	Port	Resource functional output								Possible Resource Function Input
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7	
PCFGR241 (0x0152)	P2_41	GPIO2_41	SPI0_DATA1	I2S0_SD		PPG65_PPGB	OCU0_OTD0_I	RLT9_TOT	PPG9_PPGA	GPIO2_41, I2S0_SD, CAN0_RX, CAN1_RX, SPI0_DATA1, SPI1_DATA1, RLT8_TIN, ICU2_IN1, FRT17_FRCK, EIC0_INT08, EIC0_INT09, ADC0_AN8
PCFGR242 (0x0154)	P2_42	GPIO2_42	SPI0_DATA0	I2S0_WS	SG0_SGA	PPG66_PPGB	OCU0_OTD1_GI		PPG10_PPGA	GPIO2_42, I2S0_WS, SPI0_DATA0, SPI1_DATA0, RLT9_TIN, ICU3_IN0, FRT18_FRCK, EIC0_INT06, ADC0_AN9
PCFGR243 (0x0156)	P2_43	GPIO2_43	SPI0_CLK	I2S0_SCK	SG0_SGO	PPG67_PPGB	OCU0_OTD0_GI		PPG11_PPGA	GPIO2_43, I2S0_SCK, EIC0_NMI, SPI0_CLK, SPI1_CLK, RLT0_TIN, ICU3_IN1, FRT19_FRCK, ADC0_AN10
PCFGR244 (0x0158)	P2_44	GPIO2_44		CAN1_TX		PPG68_PPGB	OCU16_OTD1_I	RLT7_TOT	PPG12_PPGA	GPIO2_44, I2S1_ECLK, CAN0_RX, ICU18_IN0, FRT0_FRCK, EIC0_INT08, ADC0_AN11
PCFGR245 (0x015A)	P2_45	GPIO2_45		I2S1_SD		PPG69_PPGB	OCU16_OTD0_I		PPG13_PPGA	GPIO2_45, I2S1_SD, CAN1_RX, FRT0_FRCK, RLT7_TIN, ICU18_IN1, FRT1_FRCK, FRT2_FRCK, FRT3_FRCK, CAN0_RX, EIC0_INT09, EIC0_INT10, ADC0_AN12
PCFGR246 (0x015C)	P2_46	GPIO2_46		I2S1_WS	SG0_SGA	PPG70_PPGB	OCU16_OTD1_GI	RLT5_TOT	PPG14_PPGA	GPIO2_46, I2S1_WS, CAN0_RX, ICU19_IN0, FRT2_FRCK, EIC0_INT07, EIC0_INT10, EIC0_INT08, ADC0_AN13

Table 24. Resource Input Source Table (RICFG7) (Continued)

Register (offset)	Resource Input	RESSEL[3:0] /PORTSEL [3:0]	Source for resource input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
EIC0INT09 (0x1024)	EIC0_INT09	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	reserved	reserved	P0_43 (139)	P0_48 (144)	P0_50 (146)	P1_36 (40)	P1_02 (8)
			P2_41 (161)	P2_45 (165)	P2_47 (167)	reserved	reserved	reserved	reserved	reserved
EIC0INT10 (0x1028)	EIC0_INT10	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	reserved	reserved	P0_42 (138)	P0_49 (145)	P0_50 (146)	P1_38 (42)	P1_16 (26)
			P2_40 (160)	P2_45 (165)	P2_46 (166)	reserved	reserved	reserved	reserved	reserved
EIC0INT11 (0x102C)	EIC0_INT11	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	P0_26(118)	reserved	reserved	P0_40 (136)	P0_45 (141)	P1_30 (45)	reserved	P0_42 (138)
			P1_08 (16)	P3_00 (49)	P3_02 (53)	P3_04 (55)	reserved	reserved	reserved	reserved
EIC0INT12 (0x1030)	EIC0_INT12	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	P0_26(118)	P0_28(122)	reserved	P0_40 (136)	P0_45 (141)	reserved	P0_47 (143)	P1_12 (20)
			P3_00 (49)	P3_04 (55)	P3_06 (57)	reserved	reserved	reserved	reserved	reserved
EIC0INT13 (0x1034)	EIC0_INT13	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	P1_37 (41)	P1_02 (8)	P1_16 (26)	reserved	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
EIC0INT14 (0x1038)	EIC0_INT14	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	reserved	reserved	P1_17 (27)	reserved	P3_11 (62)	P3_34 (69)	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
EIC0INT15 (0x103C)	EIC0_INT15	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	P0_41 (137)	reserved	P1_18 (28)	reserved	P3_12 (63)	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
EIC0INT16 (0x1040)	EIC0_INT16	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	P0_46 (142)	reserved	P1_19 (29)	reserved	P3_13 (80)	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
EIC0INT17 (0x1044)	EIC0_INT17	RESSEL	-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	P0_47 (143)	reserved	P1_20 (30)	reserved	P3_14 (81)	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Table 27. Pin Circuit type of QFP-176 (Continued)

Pin Number	IO_TYPE
146	BIDI50_IO
147	BIDI50_IO
148	I2C_IO
149	I2C_IO
150	BIDI50A_IO
151	BIDI50A_IO
152	supply
153	supply
154	BIDI50A_IO
155	BIDI50A_IO
156	BIDI50A_IO
157	BIDI50A_IO
158	BIDI50A_IO
159	BIDI50A_IO
160	BIDI50_IO
161	BIDI50_IO
162	BIDI50_IO
163	BIDI50_IO
164	BIDI50_IO
165	BIDI50_IO
166	BIDI50_IO
167	BIDI50_IO
168	supply
169	supply
170	BIDI50_IO
171	BIDI50_IO
172	BIDI50_IO
173	supply
174	supply
175	BIDI50_IO
176	BIDI50_IO

Table 29. Interrupt Table (Continued)

Interrupt Line Number	Interrupt Name	Interrupt Description
91	EIC0IRQ22	External Interrupt 22 (EIC0_EIRR:ER22 is set when an interrupt condition is detected at the corresponding input pin)
92	EIC0IRQ23	External Interrupt 23 (EIC0_EIRR:ER23 is set when an interrupt condition is detected at the corresponding input pin)
93	EIC0IRQ24	External Interrupt 24 (EIC0_EIRR:ER24 is set when an interrupt condition is detected at the corresponding input pin)
94	EIC0IRQ25	External Interrupt 25 (EIC0_EIRR:ER25 is set when an interrupt condition is detected at the corresponding input pin)
95	EIC0IRQ26	External Interrupt 26 (EIC0_EIRR:ER26 is set when an interrupt condition is detected at the corresponding input pin)
96	EIC0IRQ27	External Interrupt 27 (EIC0_EIRR:ER27 is set when an interrupt condition is detected at the corresponding input pin)
97	EIC0IRQ28	External Interrupt 28 (EIC0_EIRR:ER28 is set when an interrupt condition is detected at the corresponding input pin)
98	EIC0IRQ29	External Interrupt 29 (EIC0_EIRR:ER29 is set when an interrupt condition is detected at the corresponding input pin)
99	EIC0IRQ30	External Interrupt 30 (EIC0_EIRR:ER30 is set when an interrupt condition is detected at the corresponding input pin)
100	EIC0IRQ31	External Interrupt 31 (EIC0_EIRR:ER31 is set when an interrupt condition is detected at the corresponding input pin)
101	RTCIRQ	Real Time Clock Interrupt (check RTC_WINS:[6:0] for detailed Real Time Clock interrupt cause)
102	SG0IRQ	Sound Generator 0 Interrupt (SG0_CR1:ZAINT (zero amplitude interrupt), SG0_CR1:TCINT (tone pulse count interrupt), SG0_CR1:AMINT (amplitude match interrupt))
104	FRT0IRQ	Free Running Timer 0 Interrupt (FRT0_TCCS:IVF (compare clear match/counter overflow), FRT0_ETCCS:IRQZF (counter zero detection))
105	FRT1IRQ	Free Running Timer 1 Interrupt (FRT1_TCCS:IVF (compare clear match/counter overflow), FRT1_ETCCS:IRQZF (counter zero detection))
106	FRT2IRQ	Free Running Timer 2 Interrupt (FRT2_TCCS:IVF (compare clear match/counter overflow), FRT2_ETCCS:IRQZF (counter zero detection))
107	FRT3IRQ	Free Running Timer 3 Interrupt (FRT3_TCCS:IVF (compare clear match/counter overflow), FRT3_ETCCS:IRQZF (counter zero detection)
112	FRT16IRQ	Free Running Timer 16 Interrupt (FRT16_TCCS:IVF (compare clear match/counter overflow), FRT16_ETCCS:IRQZF (counter zero detection))

Table 29. Interrupt Table (Continued)

Interrupt Line Number	Interrupt Name	Interrupt Description
175	RCSCTIRQ	RC Source Clock Timer Interrupt (SYSC_SUBSCTSTATR:INTF is set when counter matches or is greater than the corresponding compare register)
176	SRCSCTIRQ	Slow RC Source Clock Timer Interrupt (SYSC_SRCSCTSTATR:INTF is set when counter matches or is greater than the corresponding compare register)
177	CORE0IRQ	CORTEX R4 Performance Monitor Interrupt
178	RLT0IRQ	Reload Timer 0 Interrupt (RLT0_TMCSR:UF is set when reload timer counter underflows)
179	RLT1IRQ	Reload Timer 1 Interrupt (RLT1_TMCSR:UF is set when reload timer counter underflows)
180	RLT2IRQ	Reload Timer 2 Interrupt (RLT2_TMCSR:UF is set when reload timer counter underflows)
181	RLT3IRQ	Reload Timer 3 Interrupt (RLT3_TMCSR:UF is set when reload timer counter underflows)
182	RLT4IRQ	Reload Timer 4 Interrupt (RLT4_TMCSR:UF is set when reload timer counter underflows)
183	RLT5IRQ	Reload Timer 5 Interrupt (RLT5_TMCSR:UF is set when reload timer counter underflows)
184	RLT6IRQ	Reload Timer 6 Interrupt (RLT6_TMCSR:UF is set when reload timer counter underflows)
185	RLT7IRQ	Reload Timer 7 Interrupt (RLT7_TMCSR:UF is set when reload timer counter underflows)
186	RLT8IRQ	Reload Timer 8 Interrupt (RLT8_TMCSR:UF is set when reload timer counter underflows)
187	RLT9IRQ	Reload Timer 9 Interrupt (RLT9_TMCSR:UF is set when reload timer counter underflows)
194	UDC0IRQ0	Up/Down Counter 0 channel 0 Interrupt (UDN0_CS0:OVFF (overflow), UDFF (underflow), CMPF (compare match))
195	UDC0IRQ1	Up/Down Counter 0 channel 1 Interrupt (UDN0_CS1:OVFF (overflow), UDFF (underflow), CMPF (compare match))
198	I2S0IRQ	I2S0 Interrupt (check I2S0_STATUS:[31:24], [19], [17:16] for detailed interrupt cause)
199	I2S1IRQ	I2S1 Interrupt (check I2S1_STATUS:[31:24], [19], [17:16] for detailed interrupt cause)
202	I2C0IRQ	I2C0 Interrupt (I2C0_IBCSR_INT (masked by I2C0_IBCSR_INTE) set after end of 1 byte data transfer or reception including acknowledge bit (bus master, addressed as slave, GCA received, Arbitration lost), I2C0_IBCSR_BER (masked by I2C0_IBCSR_BEIE) indicates bus error (Start- or Stop-Condition detected at wrong places))
203	I2C0IRQERR	I2C0 Error Interrupt (I2C0_IBCSR_BER (masked by I2C0_IEIER_BEREIE) indicates bus error (Start- or Stop-Condition detected at wrong places), I2C0_IBCSR_AL (masked by I2C0_IEIER_ALEIE) indicates arbitration lost)
206	CRC0IRQ	CRC0 Interrupt (CRC0_CFG:CIRQ set after checksum is calculated and available in register)

Table 36. Memory Layout of MEMORY_CONFIG Registers (Continued)

Offset	+7	+6	+5	+4	+3	+2	+1	+0
0xB0400218	IRQ0_IRQVA99 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA98 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400220	IRQ0_IRQVA101 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA100 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400228	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				IRQ0_IRQVA102 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400230	IRQ0_IRQVA105 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA104 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400238	IRQ0_IRQVA107 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA106 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400240	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400248	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400250	IRQ0_IRQVA113 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA112 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400258	IRQ0_IRQVA115 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA114 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400260	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400268	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400270	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400278	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400280	IRQ0_IRQVA125 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA124 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400288	IRQ0_IRQVA127 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA126 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400290	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400298	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Table 39. Memory Layout of PERI0_RBUS Registers (Continued)

Offset	+1	+0
0xB072803E- B072FFFE	reserved XXXXXXXX XXXXXXXX	
0xB0730000	reserved XXXXXXXX	SMC0_PWC 00000000
0xB0730002	reserved XXXXXXXX	SMC0_PWCS 00000000
0xB0730004	reserved XXXXXXXX	SMC0_PWCC 00000000
0xB0730006	SMC0_PWC1 000000XX XXXXXXXX	
0xB0730008	SMC0_PWC2 000000XX XXXXXXXX	
0xB073000A	SMC0_PWS 00000000 00000000	
0xB073000C	SMC0_PWSS 00000000 XXXXXXXX	
0xB073000E	reserved XXXXXXXX	SMC0_PTRGDL 00000000
0xB0730010	reserved XXXXXXXX	SMC0_DEBUG 00000000
0xB0730012- B07303FE	reserved XXXXXXXX XXXXXXXX	
0xB0730400	reserved XXXXXXXX	SMC1_PWC 00000000
0xB0730402	reserved XXXXXXXX	SMC1_PWCS 00000000
0xB0730404	reserved XXXXXXXX	SMC1_PWCC 00000000
0xB0730406	SMC1_PWC1 000000XX XXXXXXXX	
0xB0730408	SMC1_PWC2 000000XX XXXXXXXX	
0xB073040A	SMC1_PWS 00000000 00000000	

Table 39. Memory Layout of PERI0_RBUS Registers (Continued)

Offset	+1	+0
0xB073040C	SMC1_PWSS 00000000 XXXXXXXX	
0xB073040E	reserved XXXXXXXX	SMC1_PTRGDL 00000000
0xB0730410	reserved XXXXXXXX	SMC1_DEBUG 00000000
0xB0730412- B07307FE	reserved XXXXXXXX XXXXXXXX	
0xB0730800	reserved XXXXXXXX	SMC2_PWC 00000000
0xB0730802	reserved XXXXXXXX	SMC2_PWCS 00000000
0xB0730804	reserved XXXXXXXX	SMC2_PWCC 00000000
0xB0730806	SMC2_PWC1 000000XX XXXXXXXX	
0xB0730808	SMC2_PWC2 000000XX XXXXXXXX	
0xB073080A	SMC2_PWS 00000000 00000000	
0xB073080C	SMC2_PWSS 00000000 XXXXXXXX	
0xB073080E	reserved XXXXXXXX	SMC2_PTRGDL 00000000
0xB0730810	reserved XXXXXXXX	SMC2_DEBUG 00000000
0xB0730812- B0730BFE	reserved XXXXXXXX XXXXXXXX	
0xB0730C00	reserved XXXXXXXX	SMC3_PWC 00000000
0xB0730C02	reserved XXXXXXXX	SMC3_PWCS 00000000
0xB0730C04	reserved XXXXXXXX	SMC3_PWCC 00000000

Table 39. Memory Layout of PERI0_RBUS Registers (Continued)

Offset	+1	+0
0xB07E816A	PPC_PCFGR253 0XX00000 00000000	
0xB07E816C	PPC_PCFGR254 0XX00000 00000000	
0xB07E816E	PPC_PCFGR255 0XX00000 00000000	
0xB07E8170	PPC_PCFGR256 0XX00000 00000000	
0xB07E8172	PPC_PCFGR257 0XX00000 00000000	
0xB07E8174	PPC_PCFGR258 0XX00000 00000000	
0xB07E8176	PPC_PCFGR259 0XX00000 00000000	
0xB07E8178	PPC_PCFGR260 0XX00000 00000000	
0xB07E817A	PPC_PCFGR261 0XX00000 00000000	
0xB07E817C	PPC_PCFGR262 0XX00000 00000000	
0xB07E817E	PPC_PCFGR263 0XX00000 00000000	
0xB07E8180	PPC_PCFGR300 0XX00000 00000000	
0xB07E8182	PPC_PCFGR301 0XX00000 00000000	
0xB07E8184	PPC_PCFGR302 0XX00000 00000000	
0xB07E8186	PPC_PCFGR303 0XX00000 00000000	
0xB07E8188	PPC_PCFGR304 0XX00000 00000000	
0xB07E818A	PPC_PCFGR305 0XX00000 00000000	

Table 40. Memory Layout of PERI1_RBUS Registers (Continued)

Offset	+1	+0
0xB0808456	CAN1_IF2DTB2 00000000 00000000	
0xB0808458- B080847E	reserved XXXXXXXX XXXXXXXX	
0xB0808480	CAN1_TREQR1 00000000 00000000	
0xB0808482	CAN1_TREQR2 00000000 00000000	
0xB0808484	CAN1_TREQR3 00000000 00000000	
0xB0808486	CAN1_TREQR4 00000000 00000000	
0xB0808488- B080848E	reserved XXXXXXXX XXXXXXXX	
0xB0808490	CAN1_NEWDT1 00000000 00000000	
0xB0808492	CAN1_NEWDT2 00000000 00000000	
0xB0808494	CAN1_NEWDT3 00000000 00000000	
0xB0808496	CAN1_NEWDT4 00000000 00000000	
0xB0808498- B080849E	reserved XXXXXXXX XXXXXXXX	
0xB08084A0	CAN1_INTPND1 00000000 00000000	
0xB08084A2	CAN1_INTPND2 00000000 00000000	
0xB08084A4	CAN1_INTPND3 00000000 00000000	
0xB08084A6	CAN1_INTPND4 00000000 00000000	
0xB08084A8- B08084AE	reserved XXXXXXXX XXXXXXXX	

Table 42. Memory Layout of PERI4_SLAVE Registers (Continued)

Offset	+3	+2	+1	+0
0xB0B38014	SPI0_TXF 00000000 00000000 00000000 00000000			
0xB0B38018	SPI0_TXE 00000000 00000000 00000000 00000000			
0xB0B3801C	SPI0_TXC 00000000 00000000 00000000 00000000			
0xB0B38020	SPI0_RXF 00000000 00000000 00000000 00000000			
0xB0B38024	SPI0_RXE 00000000 00000000 00000000 00000000			
0xB0B38028	SPI0_RXC 00000000 00000000 00000000 00000000			
0xB0B3802C	SPI0_FAULTF 00000000 00000000 00000000 00000000			
0xB0B38030	SPI0_FAULTC 00000000 00000000 00000000 00000000			
0xB0B38034	read0 00000000 00000000		SPI0_DMDMAEN 00000000	SPI0_DMCFG 00000001
0xB0B38038	SPI0_DMTRP 00000000	SPI0_DMPSEL 00000000	SPI0_DMSTOP 00000000	SPI0_DMSTART 00000000
0xB0B3803C	SPI0_DMBCS 00000000 00000000		SPI0_DMBCC 00000000 00000000	
0xB0B38040	SPI0_DMSTATUS 00000000 00000000 00000000 00000000			
0xB0B38044	read0 00000000 00000000		SPI0_RXBITCNT 00000000	SPI0_TXBITCNT 00000000
0xB0B38048	SPI0_RXSHIFT 00000000 00000000 00000000 00000000			
0xB0B3804C	SPI0_FIFOCFG 00000000 00000000 00000000 01110111			
0xB0B38050	SPI0_TXFIFO0 00000000 00000000 00000000 00000000			
0xB0B38054	SPI0_TXFIFO1 00000000 00000000 00000000 00000000			

Table 43. Memory Layout of PERI5_AHB Registers (Continued)

Offset	+3	+2	+1	+0
0xB0C009CC	DMA0_DA39 00000000 00000000 00000000 00000000			
0xB0C009D0	DMA0_C39 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C009D4	DMA0_D39 00000000 XXXXXXXX 00000000 XXXXXXXX			
0xB0C009D8	DMA0_SASHDW39 00000000 00000000 00000000 00000000			
0xB0C009DC	DMA0_DASHDW39 00000000 00000000 00000000 00000000			
0xB0C009E0- B0C009FC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C00A00	DMA0_A40 00000000 00001111 00000000 00000000			
0xB0C00A04	DMA0_B40 00000000 00000000 00110011 01111111			
0xB0C00A08	DMA0_SA40 00000000 00000000 00000000 00000000			
0xB0C00A0C	DMA0_DA40 00000000 00000000 00000000 00000000			
0xB0C00A10	DMA0_C40 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C00A14	DMA0_D40 00000000 XXXXXXXX 00000000 XXXXXXXX			
0xB0C00A18	DMA0_SASHDW40 00000000 00000000 00000000 00000000			
0xB0C00A1C	DMA0_DASHDW40 00000000 00000000 00000000 00000000			
0xB0C00A20- B0C00A3C	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C00A40	DMA0_A41 00000000 00001111 00000000 00000000			
0xB0C00A44	DMA0_B41 00000000 00000000 00110011 01111111			

Table 43. Memory Layout of PERI5_AHB Registers (Continued)

Offset	+3	+2	+1	+0
0xB0C021BC	DMA0_CMICIC103 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021C0	DMA0_CMICIC104 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021C4	DMA0_CMICIC105 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021C8	DMA0_CMICIC106 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021CC	DMA0_CMICIC107 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021D0	DMA0_CMICIC108 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021D4	DMA0_CMICIC109 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021D8	DMA0_CMICIC110 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021DC	DMA0_CMICIC111 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021E0	DMA0_CMICIC112 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021E4	DMA0_CMICIC113 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021E8	DMA0_CMICIC114 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021EC	DMA0_CMICIC115 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021F0	DMA0_CMICIC116 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021F4	DMA0_CMICIC117 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021F8	DMA0_CMICIC118 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C021FC	DMA0_CMICIC119 00000000 XXXXXXXX XXXXXXXX XXXXXXXX			

Table 43. Memory Layout of PERI5_AHB Registers (Continued)

Offset	+3	+2	+1	+0
0xB0C0281C	DMA0_CMCHIC7 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02820	DMA0_CMCHIC8 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02824	DMA0_CMCHIC9 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02828	DMA0_CMCHIC10 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C0282C	DMA0_CMCHIC11 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02830	DMA0_CMCHIC12 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02834	DMA0_CMCHIC13 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02838	DMA0_CMCHIC14 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C0283C	DMA0_CMCHIC15 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02840	DMA0_CMCHIC16 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02844	DMA0_CMCHIC17 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02848	DMA0_CMCHIC18 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C0284C	DMA0_CMCHIC19 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02850	DMA0_CMCHIC20 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02854	DMA0_CMCHIC21 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02858	DMA0_CMCHIC22 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C0285C	DMA0_CMCHIC23 XXXXXXXX XXXXXXXX 00000000 00000010			

Table 43. Memory Layout of PERI5_AHB Registers (Continued)

Offset	+3	+2	+1	+0
0xB0C02860	DMA0_CMCHIC24 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02864	DMA0_CMCHIC25 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02868	DMA0_CMCHIC26 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C0286C	DMA0_CMCHIC27 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02870	DMA0_CMCHIC28 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02874	DMA0_CMCHIC29 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02878	DMA0_CMCHIC30 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C0287C	DMA0_CMCHIC31 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02880	DMA0_CMCHIC32 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02884	DMA0_CMCHIC33 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02888	DMA0_CMCHIC34 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C0288C	DMA0_CMCHIC35 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02890	DMA0_CMCHIC36 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02894	DMA0_CMCHIC37 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C02898	DMA0_CMCHIC38 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C0289C	DMA0_CMCHIC39 XXXXXXXX XXXXXXXX 00000000 00000010			
0xB0C028A0	DMA0_CMCHIC40 XXXXXXXX XXXXXXXX 00000000 00000010			

Table 46. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"H" level average overall output current	$\Sigma I_{OHAVDP5}$	-	-50	mA	-
	$\Sigma I_{OHAVDP3}$	-	-50	mA	-
	$\Sigma I_{OHADVCC}$	-	-240	mA	-
Power consumption	P_{TOT}	-	2000	mW	-
Operating ambient temperature	T_A	-40	105	°C	-
Storage temperature	T_{STG}	-55	150	°C	-

Notes

6. AV_{DD5} and V_{DP5} must be set to the same voltage. It is required that AV_{DD5} does not exceed V_{DP5} and that the voltage at the analog inputs does not exceed AV_{DD5} neither when the power is switched on.
7. V_I and V_O should not exceed V_{DP5} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{DP5}.
8. Clamping current limitation:
   - Applicable to all general purpose I/O pins (Pi_jj)
   - Use within recommended operating conditions.
   - Use at DC voltage (current)
   - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
   - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
   - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{DP5} pin, and this may affect other devices.
   - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
   - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
   - Sample recommended circuits is shown in Figure 5.

Figure 5. ESD Protection Structure for GPIO Pins

9. DV_{CC}, AV_{DD5} and V_{DP5} must be set to the same voltage during zero point detection (ZPD) on any of the SMC ports. If zero point detection is not required on any of the SMC ports, then DV_{CC} can have any value with-in absolute rating, provided switches are disabled by RICFG0_ADC0ZPDEN:ZPDEN register. Note, for ZPD, conversion time will be more and accuracy of measurement will be low.

Figure 11. I2C Timing

HSSPI Timing

(T_A = -40°C to 105°C, V_{DD} = 1.1V to 1.3V, V_{DP3} = 3.0V to 3.6V, V_{DP5} = AV_{DD5} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS5} = DV_{SS} = 0V)

Table 58. HSSPI Interface Timing (Master Mode)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
HSSPI clock frequency		-	-	64	MHz	
Input setup time (HSSPIn_DATAi)	$T_{IS,DATA}$	12.1	-	-	ns	no clock retiming
		5.6	-	-	ns	with clock retiming
Input hold time (HSSPIn_DATAi)	$T_{IH,DATA}$	0	-	-	ns	no clock retiming
		1.5	-	-	ns	with clock retiming
Output delay time (HSSPIn_DATAo)	$T_{OD,DATA}$	-	-	3.8	ns	
Output hold time (HSSPIn_DATAo)	$T_{OH,DATA}$	5	-	-	ns	
Output delay time (HSSPIn_SSELo)	$T_{OD,SSEL}$	-	-	5.05	ns	
Output hold time (HSSPIn_SSELo)	$T_{OH,SSEL}$	0	-	-	ns	

Analog Digital Converter

(T_A = -40°C to +105°C, 3.0V -≤ AV_{RH5}, V_{DD} = 1.1V to 1.3V, V_{DP3} = 3.0V to 3.6V, V_{DP5} = AV_{DD5} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS5} = DV_{SS} = 0V)

Table 74. Analog Digital Converter

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Full scale transition voltage	V_{FST}	ANi	AV_{RH5} - 3.5 LSB	AV_{RH5} - 1.5 LSB	AV_{RH5} + 0.5 LSB	V	
Zero Transition Voltage	V_{FST}	ANi	Typ - 20	AV_{SS5} + 0.5 LSB	Typ + 20	mV	Between 0 and 1
Conversion Rate	TS	pi_jj(ANIN)	353	-	1186	KS/s	
Comparison Time	T_{COMP}	-	646.8	-	-	ns	Fclk=17MHz, Tclk=58.8ns * 11 clocks
			-	-	2750	ns	AVDD5 = 4.5V...5.5V, Fclk=4MHz, Tclk=250ns * 11 clocks
			-	-	1837	ns	AVDD5 = 3.0V...4.5V, Fclk=6MHz, Tclk=167ns * 11 clocks
Analog input leakage current (during conversion)	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25°C, AV_{SS5} < V_I < AV_{DD5}, AV_{RH5}
			-3	-	+3	µA	T_A ≤ 105°C, AV_{SS5} < V_I < AV_{DD5}, AV_{RH5}
Analog input voltage range	V_{AIN}	ANn	AV_{SS5}	-	AV_{RH5}	V	
Reference voltage range	AV_{RH5}	AV_{RH5}	AV_{DD5} - 0.5	-	AV_{DD5}	V	
Power supply current	I_A	AV_{DD5}	-	2	3.4	mA	A/D Converter active
	I_{AH}	AV_{DD5}	-	-	6	µA	25°C, A/D Converter not operated
			-	-	11	µA	105°C, A/D Converter not operated
Reference voltage current	I_R	AV_{RH5}	-	0.6	1	mA	A/D Converter active
	I_{RH}	AV_{RH5}	-	-	0.6	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note
24. The accuracy gets worse as |AV_{RH5}| becomes smaller.

Figure 26. ESD Diodes between DVCC, DVSS and VSS

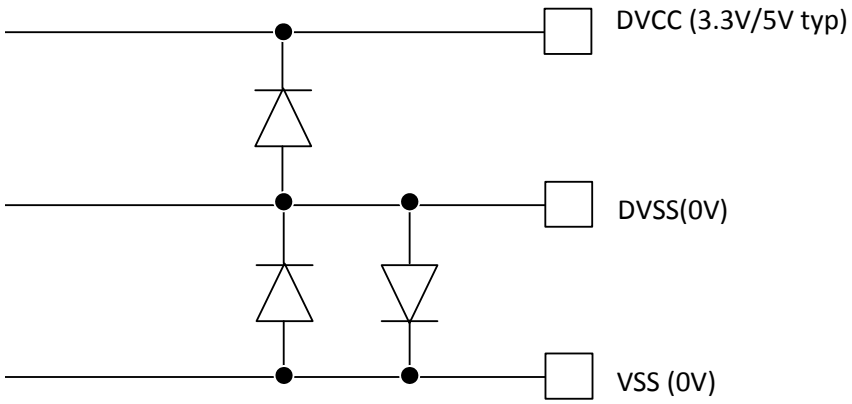
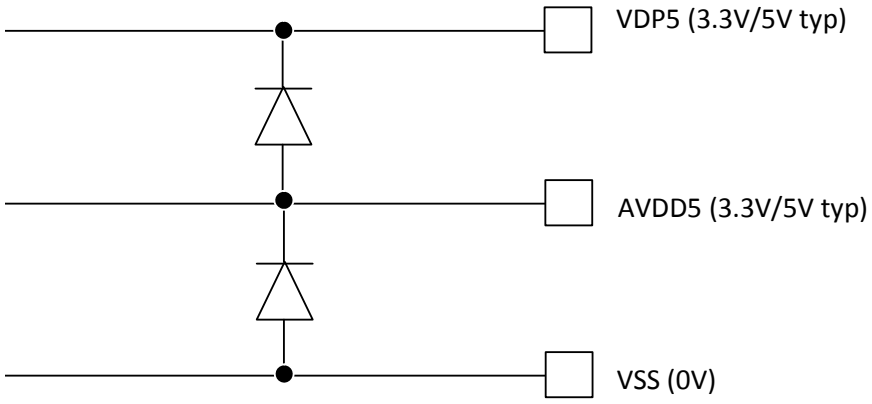


Figure 27. ESD Diodes between VDP5, AVDD5 and VSS



Problem may occur for Sub Source Clock Timer if all of the following conditions are met:

- Sub Source Clock Timer runs with compare value “old value”
- SYSC_SUBSCTCPR_CMPR is set to “new value”
- SYSC_SUBSCTTRG_CGCPT set to ‘1’ trigger compare value update
- Bitwise AND of “new value” and “old value” is equal to 0 and neither “new value” nor “old value” equal to 0.

By hard reset “old value” is initialized to 0x0400.

❒ **Cause of Failure**

The current implementation of the Source Clock Timer generates an asynchronous reset for the Source Clock Timer Counter in case the updated compare value is 0. This condition could be met for a short period of time when the compare value register in the Source Clock Timer capture the new compare value and generate a glitch at the reset of the counter registers. The width of this glitch does not guarantee a valid reset. As a result of this glitch it is unpredictable which of the counter register bits is reset and which not.

❒ **Workaround**

For changing the compare value of a Source Clock timer from effective “old value” to a “new value” ensure that following conditions is true.

- “old value” & “new value” != 0

❒ **Fix Status**

There is no plan to change this behaviour for MB9DF125 series.

9. Clock Supervisor Disable-Enable Problem

■ **Description**

A problem was found MB9DF125 series in the behavior of the Clock Supervisor (CSV).

Sporadically when re-enabling a CSV, a reset/NMI is triggered by the CSV even if the observed frequency is in the permitted range. This phenomenon can only happen, if the CSV had already been used since the last hard reset.

Affected are all Clock Supervisor instances:

❒ Main Oscillator CSV
❒ Sub Oscillator CSV
❒ Main PLL CSV
❒ SSCG PLL CSV

■ **Parameters Affected**

All part numbers of the MB9DF125 series are affected.

■ **Problem Conditions**

Problem occurs if all of the following conditions are met:

❒ The CSV had been running, then got disabled and is re-enabled again
❒ The sequence above has not been interrupted by any hard reset

The typical use case leading to the occurrence of the problem may be the supervising of clocks which are active in RUN state and switched off during power-save state (PSS), e.g. Main Oscillator and Main PLL.

❒ **Cause of Failure**

The CSV does not reset internal counters, when it is disabled.

After re-enabling the CSV it starts from the previous position and it is possible that it detects the observed frequency being out of range, although it is inside.

Due to desired short reaction time the error counters do not tolerate some additional margin at its start-up condition.