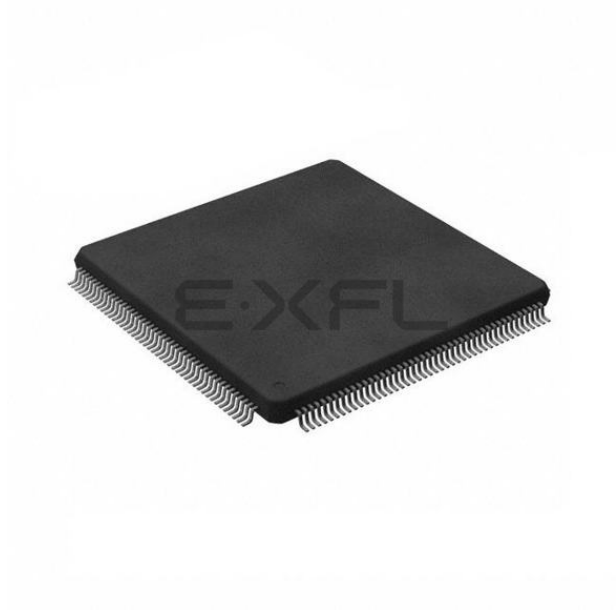
Infineon Technologies - MB9DF125PMC-GSK5E2 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-R4
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	141
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 5.5V
Data Converters	A/D 50x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9df125pmc-gsk5e2

ID-Values for Module Identification Registers

For several peripheral and system related modules, the hardware contains Module Identification Registers that hold read-only values which contain information about the module number, the version and possible patches.

Table 15. List of Module ID

Module	ID-Register	ID Value
System Controller	SYSC_SYSIDR	0x00031101
Security Checker	SCCFG_MODID	0x00020400
SRAM Interface	SRCFG_MID	0x00040300
TC-Flash Interface	TCFCFG_FMIDR	0x000E0300
EE-Flash Interface	EEFCFG_MIR	0x00090700
Interrupt Controller 0	IRQ0_MID	0x000B0100
DMA Controller 0	DMA0_ID	0x00010300
Timing Protection Unit 0	TPU0_MID	0x00050200
Memory Protection Unit for AXI	MPUXDMA0_MID	0x000D0200
Memory Protection Unit for AXI	MPUXSHE_MID	0x000D0200
Bus Error Collection Unit 0	BECU0_MIDH / BECU0_MIDL	0x0008 / 0x0200
Bus Error Collection Unit 1	BECU1_MIDH / BECU1_MIDL	0x0008 / 0x0200
Bus Error Collection Unit 3	BECU3_MIDH / BECU3_MIDL	0x0008 / 0x0200
High Speed SPI Interface 0	HSSPI0_MID	0x00060300
SPI Interface 0	SPI0_MID	0x00070300
SPI Interface 1	SPI1_MID	0x00070300
SPI Interface 2	SPI2_MID	0x00070300
Inter IC Sound 0	I2S0_MIDREG	0x000A0300
Inter IC Sound 1	I2S1_MIDREG	0x000A0300
SHE	SHE_MID	0x000F0200

Table 18. Port Pin Multiplexing (Continued)

Register (offset)	Port	Resource functional output								Possible Resource Function Input
		POF=0	POF=1	POF=2	POF=3	POF=4	POF=5	POF=6	POF=7	
PCFGR026 (0x0034)	P0_26	GPIO0_26		OCU1_OTD0_GI		PPG10_PPGB	OCU1_OTD0		PPG2_PPGA	GPIO0_26, EIC0_INT11, EIC0_INT12, USART0_SIN, USART6_SIN, ICU3_IN0, RLT3_TIN
PCFGR027 (0x0036)	P0_27	GPIO0_27	USART0_SCK	OCU1_OTD1_GI		PPG11_PPGB	OCU1_OTD1		PPG3_PPGA	GPIO0_27, EIC0_INT29, USART0_SCK, USART6_SCK, ICU3_IN1, RLT4_TIN
PCFGR028 (0x0038)	P0_28	GPIO0_28	USART0_SOT	OCU16_OTD0_GI		PPG12_PPGB	OCU16_OTD0	RLT5_TOT	PPG4_PPGA	GPIO0_28, EIC0_INT12, USART6_SIN, ICU18_IN0I
PCFGR040 (0x0050)	P0_40	GPIO0_40	SPI2_SS	RTC_WOT		PPG64_PPGB	OCU16_OTD0_G		PPG8_PPGA	GPIO0_40, EIC0_INT05, EIC0_INT12, EIC0_INT11, SPI2_SS, USART6_SIN, USART0_SIN, FRT0_FRCK, RLT5_TIN, ADC0_AN15
PCFGR041 (0x0052)	P0_41	GPIO0_41	SPI2_DATA1	SYSC_CKOT	USART6_SCK	PPG65_PPGB	OCU16_OTD1_G		PPG9_PPGA	GPIO0_41, EIC0_INT15, SPI2_DATA1, USART6_SCK, USART0_SCK, FRT1_FRCK, RLT6_TIN, ICU2_IN0, ICU18_IN1, ADC0_AN16
PCFGR042 (0x0054)	P0_42	GPIO0_42	SPI2_DATA0	SYSC_CKOTX	USART6_SOT	PPG66_PPGB	OCU17_OTD0_G	RLT2_TOT	PPG10_PPGA	GPIO0_42, EIC0_INT08, EIC0_INT10, EIC0_INT11, SPI2_DATA0, CAN0_RX,, FRT2_FRCK, CAN1_RX,, ICU2_IN1, ICU19_IN0, USART0_SIN, ADC0_AN17
PCFGR043 (0x0056)	P0_43	GPIO0_43	SPI2_CLK	WDG_OBSERVE	CAN0_TX	PPG67_PPGB	OCU17_OTD1_G		PPG11_PPGA	GPIO0_43, EIC0_INT09, SPI2_CLK, CAN1_RX, FRT3_FRCK, RLT2_TIN, ADC0_AN18
PCFGR044 (0x0058)	P0_44	GPIO0_44	SPI0_SS	SPI2_SSO2	SPI2_DATA2	PPG68_PPGB	OCU0_OTD0_G	RLT3_TOT	PPG12_PPGA	GPIO0_44, EIC0_INT03, SPI2_DATA2, SPI0_SS, FRT16_FRCK, UDC0_AIN0, ADC0_AN19

Table 22. Resource Input Source Table (RICFG3) (Continued)

Register (offset)	Resource Input	RESSEL[3:0]/PORTSEL[3:0]	Source for resource input							
			0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
RLT5TIN (0x08A0)	RLT5_TIN	RESSEL	Port Sel	RLT4_TOT	RLT4_UFSET	RLT6_TOT	PPG5_PPGA	USART0_SOT	USART6_SOT	reserved
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	P0_40 (136)	reserved	reserved	P1_12 (20)	P3_00 (49)	P3_30 (101)	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT6TIN (0x08C0)	RLT6_TIN	RESSEL	Port Sel	RLT5_TOT	RLT5_UFSET	RLT7_TOT	PPG6_PPGA	UDC0_UDOT0	UDC0_UDOT1	reserved
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	P0_41 (137)	reserved	P1_13 (21)	P3_01 (52)	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT7TIN (0x08E0)	RLT7_TIN	RESSEL	Port Sel	RLT6_TOT	RLT6_UFSET	RLT8_TOT	PPG7_PPGA	UDC0_UDOT0	UDC0_UDOT1	reserved
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	reserved	reserved	P2_38 (158)	P2_45 (165)	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT8TIN (0x0900)	RLT8_TIN	RESSEL	Port Sel	RLT7_TOT	RLT7_UFSET	RLT9_TOT	PPG8_PPGA	UDC0_UDOT0	UDC0_UDOT1	reserved
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	reserved	reserved	P2_37 (157)	P2_41 (161)	reserved	reserved	reserved
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
RLT9TIN (0x0920)	RLT9_TIN	RESSEL	Port Sel	RLT8_TOT	RLT8_UFSET	RLT0_TOT	PPG9_PPGA	UDC0_UDOT0	UDC0_UDOT1	reserved
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	reserved	reserved	P2_36 (156)	P2_42 (162)	reserved	reserved	reserved
			P0_09(111)	reserved	reserved	reserved	reserved	reserved	reserved	reserved
UDC0AIN0 (0x1000)	UDC0_AIN0	RESSEL	Port Sel	RLT0_TOT	RLT3_TOT	RLT7_TOT	reserved	reserved	reserved	reserved
			-	-	-	-	-	-	-	-
		PORTSEL	reserved	reserved	P1_34 (38)	reserved	P0_44 (140)	P2_33 (151)	P3_14 (81)	P3_34 (69)
			P0_08(110)	reserved	reserved	reserved	reserved	reserved	reserved	reserved
UDC0AIN1 (0x1004)	UDC0_AIN1	RESSEL	Port Sel	RLT1_TOT	RLT4_TOT	RLT7_TOT	reserved	reserved	reserved	reserved
			-	-	-	-	-	-	-	-
		PORTSEL	P0_12(114)	reserved	reserved	reserved	P0_48 (144)	P2_37 (157)	P3_04 (55)	P3_18 (85)
			P3_38 (73)	reserved	reserved	reserved	reserved	reserved	reserved	reserved
UDC0BIN0 (0x1008)	UDC0_BIN0	RESSEL	Port Sel	RLT1_TOT	RLT4_TOT	RLT8_TOT	reserved	reserved	reserved	reserved
			-	-	-	-	-	-	-	-
		PORTSEL	P0_09(111)	reserved	P1_35 (39)	reserved	P0_45 (141)	P2_34 (154)	P3_15 (82)	P3_35 (70)
			reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Table 29. Interrupt Table (Continued)

Interrupt Line Number	Interrupt Name	Interrupt Description
175	RCSCTIRQ	RC Source Clock Timer Interrupt (SYSC_SUBSCTSTATR:INTF is set when counter matches or is greater than the corresponding compare register)
176	SRCSCTIRQ	Slow RC Source Clock Timer Interrupt (SYSC_SRCSCTSTATR:INTF is set when counter matches or is greater than the corresponding compare register)
177	CORE0IRQ	CORTEX R4 Performance Monitor Interrupt
178	RLT0IRQ	Reload Timer 0 Interrupt (RLT0_TMCSR:UF is set when reload timer counter underflows)
179	RLT1IRQ	Reload Timer 1 Interrupt (RLT1_TMCSR:UF is set when reload timer counter underflows)
180	RLT2IRQ	Reload Timer 2 Interrupt (RLT2_TMCSR:UF is set when reload timer counter underflows)
181	RLT3IRQ	Reload Timer 3 Interrupt (RLT3_TMCSR:UF is set when reload timer counter underflows)
182	RLT4IRQ	Reload Timer 4 Interrupt (RLT4_TMCSR:UF is set when reload timer counter underflows)
183	RLT5IRQ	Reload Timer 5 Interrupt (RLT5_TMCSR:UF is set when reload timer counter underflows)
184	RLT6IRQ	Reload Timer 6 Interrupt (RLT6_TMCSR:UF is set when reload timer counter underflows)
185	RLT7IRQ	Reload Timer 7 Interrupt (RLT7_TMCSR:UF is set when reload timer counter underflows)
186	RLT8IRQ	Reload Timer 8 Interrupt (RLT8_TMCSR:UF is set when reload timer counter underflows)
187	RLT9IRQ	Reload Timer 9 Interrupt (RLT9_TMCSR:UF is set when reload timer counter underflows)
194	UDC0IRQ0	Up/Down Counter 0 channel 0 Interrupt (UDN0_CS0:OVFF (overflow), UDFF (underflow), CMPF (compare match))
195	UDC0IRQ1	Up/Down Counter 0 channel 1 Interrupt (UDN0_CS1:OVFF (overflow), UDFF (underflow), CMPF (compare match))
198	I2S0IRQ	I2S0 Interrupt (check I2S0_STATUS:[31:24], [19], [17:16] for detailed interrupt cause)
199	I2S1IRQ	I2S1 Interrupt (check I2S1_STATUS:[31:24], [19], [17:16] for detailed interrupt cause)
202	I2C0IRQ	I2C0 Interrupt (I2C0_IBCSR_INT (masked by I2C0_IBCSR_INTE) set after end of 1 byte data transfer or reception including acknowledge bit (bus master, addressed as slave, GCA received, Arbitration lost), I2C0_IBCSR_BER (masked by I2C0_IBCSR_BEIE) indicates bus error (Start- or Stop-Condition detected at wrong places))
203	I2C0IRQERR	I2C0 Error Interrupt (I2C0_IBCSR_BER (masked by I2C0_IEIER_BEREIE) indicates bus error (Start- or Stop-Condition detected at wrong places), I2C0_IBCSR_AL (masked by I2C0_IEIER_ALEIE) indicates arbitration lost)
206	CRC0IRQ	CRC0 Interrupt (CRC0_CFG:CIRQ set after checksum is calculated and available in register)

Table 34. Memory Layout of HSSPI0 Registers (Continued)

Offset	+3	+2	+1	+0
0xB007FC04	BSU8_BTST 00000000 00000000 00000000 00000000			
0xB007FC08- B007FC0C	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB007FC10	BSU8_PEN0 00000000 00000000 00000000 00000000			
0xB007FC14- B007FFFC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Table 36. Memory Layout of MEMORY_CONFIG Registers (Continued)

Offset	+7	+6	+5	+4	+3	+2	+1	+0
0xB0400190	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400198	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB04001A0	IRQ0_IRQVA69 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB04001A8	IRQ0_IRQVA71 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA70 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001B0	IRQ0_IRQVA73 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA72 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001B8	IRQ0_IRQVA75 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA74 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001C0	IRQ0_IRQVA77 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA76 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001C8	IRQ0_IRQVA79 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA78 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001D0	IRQ0_IRQVA81 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA80 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001D8	IRQ0_IRQVA83 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA82 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001E0	IRQ0_IRQVA85 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA84 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001E8	IRQ0_IRQVA87 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA86 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001F0	IRQ0_IRQVA89 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA88 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04001F8	IRQ0_IRQVA91 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA90 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400200	IRQ0_IRQVA93 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA92 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400208	IRQ0_IRQVA95 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA94 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400210	IRQ0_IRQVA97 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA96 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			

Table 36. Memory Layout of MEMORY_CONFIG Registers (Continued)

Offset	+7	+6	+5	+4	+3	+2	+1	+0
0xB04003B0	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB04003B8	IRQ0_IRQVA203 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA202 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04003C0	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB04003C8	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				IRQ0_IRQVA206 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04003D0	IRQ0_IRQVA209 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA208 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04003D8	IRQ0_IRQVA211 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA210 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04003E0	IRQ0_IRQVA213 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA212 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04003E8	IRQ0_IRQVA215 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA214 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04003F0	IRQ0_IRQVA217 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA216 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB04003F8	IRQ0_IRQVA219 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA218 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400400	IRQ0_IRQVA221 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA220 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400408	IRQ0_IRQVA223 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA222 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			
0xB0400410	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400418	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400420	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400428	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400430	IRQ0_IRQVA233 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00				IRQ0_IRQVA232 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXX00			

Table 36. Memory Layout of MEMORY_CONFIG Registers (Continued)

Offset	+7	+6	+5	+4	+3	+2	+1	+0
0xB0400CA8	IRQ0_NMIPS 00000000 00000000 00000000 00000000				IRQ0_NMIRS 00000000 00000000 00000000 00000000			
0xB0400CB0	IRQ0_IRQRS1 00000000 00000000 00000000 00000000				IRQ0_IRQRS0 00000000 00000000 00000000 00000000			
0xB0400CB8	IRQ0_IRQRS3 00000000 00000000 00000000 00000000				IRQ0_IRQRS2 00000000 00000000 00000000 00000000			
0xB0400CC0	IRQ0_IRQRS5 00000000 00000000 00000000 00000000				IRQ0_IRQRS4 00000000 00000000 00000000 00000000			
0xB0400CC8	IRQ0_IRQRS7 00000000 00000000 00000000 00000000				IRQ0_IRQRS6 00000000 00000000 00000000 00000000			
0xB0400CD0	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				read0 00000000 00000000 00000000 00000000			
0xB0400CD8	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400CE0	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400CE8	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400CF0	IRQ0_IRQPS1 00000000 00000000 00000000 00000000				IRQ0_IRQPS0 00000000 00000000 00000000 00000000			
0xB0400CF8	IRQ0_IRQPS3 00000000 00000000 00000000 00000000				IRQ0_IRQPS2 00000000 00000000 00000000 00000000			
0xB0400D00	IRQ0_IRQPS5 00000000 00000000 00000000 00000000				IRQ0_IRQPS4 00000000 00000000 00000000 00000000			
0xB0400D08	IRQ0_IRQPS7 00000000 00000000 00000000 00000000				IRQ0_IRQPS6 00000000 00000000 00000000 00000000			
0xB0400D10	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400D18	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400D20	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0400D28	read0 00000000 00000000 00000000 00000000				reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			

Table 38. Memory Layout of MCU_CONFIG Registers (Continued)

Offset	+3	+2	+1	+0
0xB0600308	SYSC_CSVMPCFGR 00000000 00000000 00000000 00000000			
0xB060030C	SYSC_CSVSPCFGR 00000000 00000000 00000000 00000000			
0xB0600310	SYSC_CSVGPCFGR 00000000 00000000 00000000 00000000			
0xB0600314	SYSC_CSVTESTR 00000000 00000000 00000000 00000000			
0xB0600318- B060037C	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0600380	SYSC_RSTCNTR 00000000 00000000 00000000 00000000			
0xB0600384	SYSC_RSTCAUSEUR 00011110 00000000 00000000 00000001			
0xB0600388	SYSC_RSTCAUSEBT X0011110 00000000 00000000 00000001			
0xB060038C- B06003FC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0600400	SYSC_SRCSCTTRG 00000000 00000000 00000000 00000000			
0xB0600404	SYSC_SRCSCTCNTR 00000000 00000000 00000000 00000000			
0xB0600408	SYSC_SRCSCTCPR 00000000 00000110 00000000 00000001			
0xB060040C	SYSC_SRCSCTSTATR 00000000 00000000 00000000 00000000			
0xB0600410	SYSC_SRCSCTINTER 00000000 00000000 00000000 00000000			
0xB0600414	SYSC_SRCSCTICLR 00000000 00000000 00000000 00000000			
0xB0600418- B060047C	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0600480	SYSC_RCSCTTRG 00000000 00000000 00000000 00000000			

Table 39. Memory Layout of PERI0_RBUS Registers (Continued)

Offset	+1	+0
0xB073B008	PPG12_TRIGCLR 00000000	PPG12_STRD 00000000
0xB073B00A	PPG12_EPCN1 00000000 00000000	
0xB073B00C	PPG12_EPCN2 00000000 00000000	
0xB073B00E	PPG12_GCN3 00000000	PPG12_GCN1 00000000
0xB073B010	PPG12_GCN5 00000000	PPG12_GCN4 00000110
0xB073B012	PPG12_PCSR XXXXXXXX XXXXXXXX	
0xB073B014	PPG12_PDUT XXXXXXXX XXXXXXXX	
0xB073B016	PPG12_PTMR 11111111 11111111	
0xB073B018	PPG12_PSDR 00000000 00000000	
0xB073B01A	PPG12_PTPC 00000000 00000000	
0xB073B01C	PPG12_PEDR 00000000 00000000	
0xB073B01E	PPG12_DEBUG 00000000	PPG12_DMACFG 00000000
0xB073B020- B073B3FE	reserved XXXXXXXX XXXXXXXX	
0xB073B400	PPG13_PCN 00000000 00000000	
0xB073B402	PPG13_SWTRIG 00000000	PPG13_IRQCLR 00000000
0xB073B404	PPG13_CNTEN 00000000	PPG13_OE 00000000
0xB073B406	PPG13_RMPCFG 00000000	PPG13_OPTMSK 00000000

Table 40. Memory Layout of PERI1_RBUS Registers (Continued)

Offset	+1	+0
0xB08F0010	BECU1_MASTERID 00000000 00000000	
0xB08F0012	BECU1_MIDL XXXXXXXX XXXXXXXX	
0xB08F0014	BECU1_MIDH XXXXXXXX XXXXXXXX	
0xB08F0016	reserved 00000000 00000000	
0xB08F0018	BECU1_NMIEN XXXXXXXX 00000001	
0xB08F001A- B08F83FE	reserved XXXXXXXX XXXXXXXX	
0xB08F8400	RICFG1_CAN0RX 00000000 00000000	
0xB08F8402- B08F841E	reserved XXXXXXXX XXXXXXXX	
0xB08F8420	RICFG1_CAN1RX 00000000 00000000	
0xB08F8422- B08F8BFE	reserved XXXXXXXX 00000000	
0xB08F8C00	RICFG1_FRT16TEXT 00000000 00000000	
0xB08F8C02- B08F8C1E	reserved XXXXXXXX 00000000	
0xB08F8C20	RICFG1_FRT17TEXT 00000000 00000000	
0xB08F8C22- B08F8C3E	reserved XXXXXXXX 00000000	
0xB08F8C40	RICFG1_FRT18TEXT 00000000 00000000	
0xB08F8C42- B08F8C5E	reserved XXXXXXXX 00000000	
0xB08F8C60	RICFG1_FRT19TEXT 00000000 00000000	

Table 40. Memory Layout of PERI1_RBUS Registers (Continued)

Offset	+1	+0
0xB08F8C62- B08F903E	reserved XXXXXXXX 00000000	
0xB08F9040	RICFG1_ICU18IN0 00000000 XXXXXXXX	
0xB08F9042	RICFG1_ICU18IN1 00000000 XXXXXXXX	
0xB08F9044	RICFG1_ICU18FRTSEL XXXXXXXX 00000000	
0xB08F9046- B08F905E	reserved XXXXXXXX 00000000	
0xB08F9060	RICFG1_ICU19IN0 00000000 XXXXXXXX	
0xB08F9062	RICFG1_ICU19IN1 00000000 XXXXXXXX	
0xB08F9064	RICFG1_ICU19FRTSEL XXXXXXXX 00000000	
0xB08F9066- B08F93FE	reserved XXXXXXXX 00000000	
0xB08F9400	RICFG1_OCU16OTD0GATE XXXXXXXX 00000000	
0xB08F9402	RICFG1_OCU16OTD0GM XXXXXXXX 00000000	
0xB08F9404	RICFG1_OCU16OTD1GATE XXXXXXXX 00000000	
0xB08F9406	RICFG1_OCU16OTD1GM XXXXXXXX 00000000	
0xB08F9408- B08F941E	reserved XXXXXXXX 00000000	
0xB08F9420	RICFG1_OCU17CMP0EXT XXXXXXXX 00000000	
0xB08F9422	RICFG1_OCU17FRTSEL XXXXXXXX 00000000	
0xB08F9424	RICFG1_OCU17OTD0GATE XXXXXXXX 00000000	

Table 40. Memory Layout of PERI1_RBUS Registers (Continued)

Offset	+1	+0
0xB08FA4A4	RICFG1_PPG69PPGBGATE XXXXXXXX 00000000	
0xB08FA4A6	RICFG1_PPG69PPGBGM XXXXXXXX 00000000	
0xB08FA4A8- B08FA4BE	reserved XXXXXXXX 00000000	
0xB08FA4C0	RICFG1_PPG70PPGAGATE XXXXXXXX 00000000	
0xB08FA4C2	RICFG1_PPG70PPGAGM XXXXXXXX 00000000	
0xB08FA4C4	RICFG1_PPG70PPGBGATE XXXXXXXX 00000000	
0xB08FA4C6	RICFG1_PPG70PPGBGM XXXXXXXX 00000000	
0xB08FA4C8- B08FA4DE	reserved XXXXXXXX 00000000	
0xB08FA4E0	RICFG1_PPG71PPGAGATE XXXXXXXX 00000000	
0xB08FA4E2	RICFG1_PPG71PPGAGM XXXXXXXX 00000000	
0xB08FA4E4	RICFG1_PPG71PPGBGATE XXXXXXXX 00000000	
0xB08FA4E6	RICFG1_PPG71PPGBGM XXXXXXXX 00000000	
0xB08FA4E8- B08FABFE	reserved XXXXXXXX 00000000	
0xB08FAC00	RICFG1_PPGGRP16ETRG0 XXXXXXXX 00000000	
0xB08FAC02	RICFG1_PPGGRP16ETRG1 XXXXXXXX 00000000	
0xB08FAC04	RICFG1_PPGGRP16ETRG2 XXXXXXXX 00000000	
0xB08FAC06	RICFG1_PPGGRP16ETRG3 XXXXXXXX 00000000	

Table 42. Memory Layout of PERI4_SLAVE Registers (Continued)

Offset	+3	+2	+1	+0
0xB0B2003C	I2S0_RXFDAT15 00000000 00000000 00000000 00000000			
0xB0B20040	I2S0_TXFDAT0 00000000 00000000 00000000 00000000			
0xB0B20044	I2S0_TXFDAT1 00000000 00000000 00000000 00000000			
0xB0B20048	I2S0_TXFDAT2 00000000 00000000 00000000 00000000			
0xB0B2004C	I2S0_TXFDAT3 00000000 00000000 00000000 00000000			
0xB0B20050	I2S0_TXFDAT4 00000000 00000000 00000000 00000000			
0xB0B20054	I2S0_TXFDAT5 00000000 00000000 00000000 00000000			
0xB0B20058	I2S0_TXFDAT6 00000000 00000000 00000000 00000000			
0xB0B2005C	I2S0_TXFDAT7 00000000 00000000 00000000 00000000			
0xB0B20060	I2S0_TXFDAT8 00000000 00000000 00000000 00000000			
0xB0B20064	I2S0_TXFDAT9 00000000 00000000 00000000 00000000			
0xB0B20068	I2S0_TXFDAT10 00000000 00000000 00000000 00000000			
0xB0B2006C	I2S0_TXFDAT11 00000000 00000000 00000000 00000000			
0xB0B20070	I2S0_TXFDAT12 00000000 00000000 00000000 00000000			
0xB0B20074	I2S0_TXFDAT13 00000000 00000000 00000000 00000000			
0xB0B20078	I2S0_TXFDAT14 00000000 00000000 00000000 00000000			
0xB0B2007C	I2S0_TXFDAT15 00000000 00000000 00000000 00000000			

Table 43. Memory Layout of PERI5_AHB Registers (Continued)

Offset	+3	+2	+1	+0
0xB0C00494	DMA0_D18 00000000 XXXXXXXX 00000000 XXXXXXXX			
0xB0C00498	DMA0_SASHDW18 00000000 00000000 00000000 00000000			
0xB0C0049C	DMA0_DASHDW18 00000000 00000000 00000000 00000000			
0xB0C004A0- B0C004BC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C004C0	DMA0_A19 00000000 00001111 00000000 00000000			
0xB0C004C4	DMA0_B19 00000000 00000000 00110011 01111111			
0xB0C004C8	DMA0_SA19 00000000 00000000 00000000 00000000			
0xB0C004CC	DMA0_DA19 00000000 00000000 00000000 00000000			
0xB0C004D0	DMA0_C19 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C004D4	DMA0_D19 00000000 XXXXXXXX 00000000 XXXXXXXX			
0xB0C004D8	DMA0_SASHDW19 00000000 00000000 00000000 00000000			
0xB0C004DC	DMA0_DASHDW19 00000000 00000000 00000000 00000000			
0xB0C004E0- B0C004FC	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C00500	DMA0_A20 00000000 00001111 00000000 00000000			
0xB0C00504	DMA0_B20 00000000 00000000 00110011 01111111			
0xB0C00508	DMA0_SA20 00000000 00000000 00000000 00000000			
0xB0C0050C	DMA0_DA20 00000000 00000000 00000000 00000000			

Table 43. Memory Layout of PERI5_AHB Registers (Continued)

Offset	+3	+2	+1	+0
0xB0C00700	DMA0_A28 00000000 00001111 00000000 00000000			
0xB0C00704	DMA0_B28 00000000 00000000 00110011 01111111			
0xB0C00708	DMA0_SA28 00000000 00000000 00000000 00000000			
0xB0C0070C	DMA0_DA28 00000000 00000000 00000000 00000000			
0xB0C00710	DMA0_C28 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C00714	DMA0_D28 00000000 XXXXXXXX 00000000 XXXXXXXX			
0xB0C00718	DMA0_SASHDW28 00000000 00000000 00000000 00000000			
0xB0C0071C	DMA0_DASHDW28 00000000 00000000 00000000 00000000			
0xB0C00720- B0C0073C	reserved XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0xB0C00740	DMA0_A29 00000000 00001111 00000000 00000000			
0xB0C00744	DMA0_B29 00000000 00000000 00110011 01111111			
0xB0C00748	DMA0_SA29 00000000 00000000 00000000 00000000			
0xB0C0074C	DMA0_DA29 00000000 00000000 00000000 00000000			
0xB0C00750	DMA0_C29 XXXXXXXX XXXXXXXX 00000000 00000000			
0xB0C00754	DMA0_D29 00000000 XXXXXXXX 00000000 XXXXXXXX			
0xB0C00758	DMA0_SASHDW29 00000000 00000000 00000000 00000000			
0xB0C0075C	DMA0_DASHDW29 00000000 00000000 00000000 00000000			

■ SRAM Write Timing

Table 70. SRAM Write Timing Parameters

Parameter	Symbol	Pin names	Value		Unit	Note
			Min	Max		
SRAM WE delay time	T_{weo}	EBI0_MCLK, EBI0_MWEX		7	ns	
MDQM[3:0] delay time	T_{wro}	EBI0_MCLK, EBI0_MDQM[3:0]		7	ns	

Figure 15. SRAM Write Timing

Procedures

Boundary Scan

Boundary scan is supported using standard 1EEE 1149.1 JTAG interface. A 5-pin JTAG connection is available on QFP-176 (production variant), as well as QFP-240 (bond-out variant). Instruction register supported is 5-bits wide, and the standard instructions listed in Table 78 are supported. Any other value of instruction register is reserved, and should not be entered. Entering reserved values can result in indeterminate operation

Boundary scan mode may be entered by setting pins MODE = “1” and MD[0] = “0”.

Table 78. Standard Instructions

Instruction Code (in binary)	Instruction	Accessible Data Register	Remarks
‘000000’	EXTEST	Boundary scan chain	
‘000001’	SAMPLE	Boundary scan chain	
‘000010’	PRELOAD	Boundary scan chain	
‘000011’	IDCODE	Device ID code register	For MB9DF125 (ATLAS-L), IDCODE is 0x0F153009
‘000100’	USERCODE	Device user code register	For MB9DF125 (ATLAS-L), USERCODE is 32-bits long, and is 0xC4AB2012
‘000101’	HIGHZ	Boundary scan chain	
‘000110’	CLAMP	Boundary scan chain	
‘010001’	IO_CNTRL	Boundary scan chain	Command must be followed by 16bit data value: 0x04pp, where “pp” is a pin control setting from Table 79.
‘111111’	BYPASS	Bypass register	

Table 79. IO Control (IO_CNTRL) Register

IO_CNTRL															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	SEL	I2C	reserved	reserved	reserved	DCPDN	DCPUP	OUTDR[1]	OUTDR[0]	PITILS[1]	PITILS[0]
R0W0	R0W0	R0W0	R0W0	R0W0	RW	RW	R0W0	R0W0	R0W0	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1. TCFlash Programming

■ **Problem Definition**

A problem was found in the logic of the TCFlash Interface in the MB9DF125 series.Because of this problem the behaviour of the TCFlash programming is not working as specified. This problem is called 'TCFlash programming Problem'.

■ **Parameters Affected**

All part numbers of the MB9DF125 series are affected.

■ **Trigger Condition(s)**

Programming the TCFlash with ECC is not possible with 16 bit access sequences

■ **Root Cause**

Data abort of 16-bit programming sequence.

■ **Scope of Impact**

Not applicable

■ **Workaround**

In order to handle ECC calculation and Flash writes, Flash write in CPU mode is restricted to 32-bit mode.

■ **Fix Status**

There is no plan to change this behavior for MB9DF125 series.

2. 3V IO Domain ESD Diode

■ **Problem Definition**

A problem was found in the specific use-case of switching off the VDP3 supply (3V IO domain) in the MB9DF125 series.

Due to an ESD diode between VDD (core supply) and VDP3 (3V IO domain supply) the voltage on VDP3 does not reach 0V even if not supplied.

External components connected to same supply as VDP3 will be supplied with a voltage around 0.55V from VDD supply, hence power saving target in standby modes may not be achieved. This problem is called '3V IO domain ESD diode'.

■ **Parameters Affected**

All part numbers of the MB9DF125 series are affected.

■ **Trigger Condition(s)**

The problem occurs if the supply of the 3V IO domain (VDP3) is switched off.

■ **Root Cause**

There is an ESD diode between VDD and VDP3 in the core supply cell to protect VDD against ESD overvoltage.

In case VDP3 supply is switched off then VDP3 is supplied by VDD - Uth (threshold voltage of diode) which is around 1.2V - 0.65V = 0.55V.

Appendix

Workaround for IRQ Unit Register Read Timing Issue

General Considerations

It is assumed that for normal operation of the MCU and most use cases it is not necessary to read back any I-Unit registers, i.e. the application software e.g. knows which vector addresses are configured, which priorities are set and which IRQ channels are enabled.

Furthermore, it is assumed that for IRQ handling the application enables the ARM VIC port which is not affected by the read timing issue.

It is not necessary to poll the I-Unit lock status bit (IRQ0_CSR_LST) after unlocking/locking the I-Unit. This bit does not indicate any I-Unit internal time consuming operations. Its purpose is to inform the application about the current lock state so that exceptions caused by double unlocking or locking can be avoided. This can also be implemented with software means (e.g. semaphore).

For debugging during development or error logging purposes it may be useful to read certain status registers from the I-Unit (e.g. IRQ0_IRQST, IRQ0_EAN) which still can be done but it must be regarded that the gathered information may not be reliable.

Considering above mentioned assumptions the only functionality that is affected by the read timing issue is the NMI handling. FCR4 MCUs by default use the ARM “high exception vectors” option with exception vector table located at address 0xFFFF0000. This area is implemented as ROM and its contents are not changeable. The instruction placed at the FIQ exception vector (Note: FIQ and NMI are used synonymously throughout the document) will read from the NMIVAS mirror register at address 0xFFFEFBFC to retrieve the branch target. Due to the read timing issue the target address is not reliable and the read must be prevented.

Following two workarounds exist to overcome this situation and still provide NMI functionality.

- Workaround #1 (MPU) on page 413 using Memory Protection Unit ' preventing the read from NMIVAS mirror
- Workaround #2 (Low Exception) on page 416 using ARM “low exception vector” option ' allowing to replace the instruction at FIQ exception vector

All described preparatory steps in these workarounds (e.g. MPU configuration) must be completed before application enables NMIs (clearing of 'F'-bit in CPU Current Program Status Register).

If these workarounds are used, it is also not necessary to initialize the NMI specific I-Unit registers (NMI priorities, NMI vectors).

Software samples are provided to demonstrate both workarounds:

- Workaround #1: fcr4_nmi_mpu_mbxxxxx-vxx
- Workaround #2: fcr4_nmi_low_exception_mbxxxxx-vxx