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Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	MCU, Ethernet Core
Core Processor	eZ80F91
Co-Processor	-
Speed	50MHz
Flash Size	256KB (Internal), 1MB (External)
RAM Size	8KB (Internal), 512KB (External)
Connector Type	Header 2x30
Size / Dimension	2.5" x 3.1" (63.5mm x 78.7mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f915050mod

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List of Tables

Table 2-1. Z8036/Z8536 Z-CIO/CIO Register Summary--Continued

Internal Address (Binary)	Read/Write	Register Name
		Counter/Timer Related Registers
010000	R	Counter/Timer 1 Current Count MS Byte
010001	R	Counter/Timer 1 Current Count LS Byte
010010	R	Counter/Timer 2 Current Count MS Byte
010011	R	Counter/Timer 2 Current Count LS Byte
010100	R	Counter/Timer 3 Current Count MS Byte
010101	R	Counter/Timer 3 Current Count LS Byte
010110	R/W	Counter/Timer 1 Time Constant MS Byte
010111	R/W	Counter/Timer 1 Time Constant LS Byte
011000	R/W	Counter/Timer 2 Time Constant MS Byte
011001	R/W	Counter/Timer 2 Time Constant LS Byte
011010	R/W	Counter/Timer 3 Time Constant MS Byte
011011	R/W	Counter/Timer 3 Time Constant LS Byte
011100	R/W	Counter/Timer 1 Mode Specification
011101	R/W	Counter/Timer 2 Mode Specification
011110	R/W	Counter/Timer 3 Mode Specification
011111	R	Current Vector
		Port A Specification Registers
100000	R/W	Port A Mode Specification
100001	R/W	Port A Handshake Specification
100010	R/W	Port A Data Path Polarity
100011	R/W	Port A Data Direction
100100	R/W	Port A Special I/O Control
100101	R/W	Port A Pattern Polarity
100110	R/W	Port A Pattern Transition
100111	R/W	Port A Pattern Mask
		Port B Specification Registers
101000	R/W	Port B Mode Specification
101001	R/W	Port B Handshake Specification
101010	R/W	Port B Data Path Polarity
101011	R/W	Port B Data Direction
101100	R/W	Port B Special I/O Control
101101	R/W	Port B Pattern Polarity
101110	R/W	Port B Pattern Transition
101111	R/W	Port B Pattern Mask

* All bits can be read and some bits can be written.

** Also directly addressable in Z8536 using pins A_0 and A_1. (See Table 2-2 and Figures 8-1 and 8-2.)

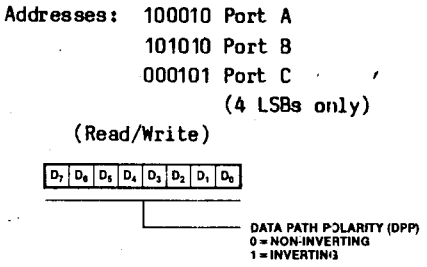


Figure 2-7. Data Path Polarity Registers

A 0 in a particular bit position of this register specifies the corresponding bit path of the port as non-inverting (that is, a High level at the port pin is 1). If a bit in this register is written with 1, the data path is programmed inverting (that is, a Low level at the pin is 1). A reset clears all bits to 0 (the port is non-inverting). The bits are read/write.

2.6.2 Data Direction Registers

Each of the Data Direction registers define the direction of data flow for the individual bits of its port if configured as a bit port. The state of this register is ignored for ports with handshake.

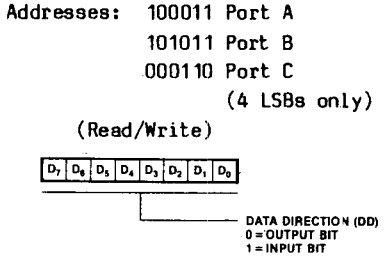


Figure 2-8. Data Direction Registers

A 0 in a bit position of this register specifies the corresponding bit of the port as an output bit, while a 1 specifies it as an input. The value programmed in this register for Ports A and B is overridden if the port is one with handshake.

An input bit specification is overridden for bits in Port C used as outputs for handshake signals or a REQUEST/$\overline{\text{WAIT}}$ line. Bits used as handshake inputs must be specified as inputs.

A reset forces all bits in these registers to 0. All bits are read/write.

2.6.3 Special I/O Control Registers

Each of the Special I/O Control registers is a dual-function register which specifies special characteristics about its port's data path. Its exact function depends on the direction of data flow defined for the path.

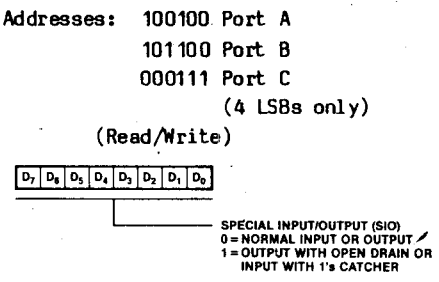


Figure 2-9. Special I/O Control Registers

If a bit is an input bit, a 1 in this register's corresponding bit position invokes a 1's catcher. A 1's catcher functions by automatically latching a 1 if its input goes to 1. It is cleared only by writing a 0 to the Input Data register. A 1's catcher is inserted into the input path after the bit's invert/non-invert logic. If the bit is programmed 0, it is a normal input bit. The 1's catcher is available only for input bit port bits.

If a bit is an output bit, a 0 in the corresponding bit position of this register specifies the output as a normal output with both a pull-up and a pull-down transistor. A 1 in this register defines the output as open-drain; no pull-up transistor is provided. The value programmed in this register applies to all output modes, independent of utilization.

A reset forces all bits to 0. All bits are read/write.

2.7 PATTERN DEFINITION REGISTERS

These registers collectively specify the match pattern for the port. As the registers must be taken together to define the pattern, they are described differently than the previous registers.

Addresses: 100101 Port A
101101 Port B
(Read/Write)

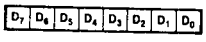


Figure 2-10. Pattern Polarity Registers

Addresses: 100110 Port A
101110 Port B
(Read/Write)

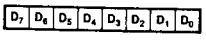


Figure 2-11. Pattern Transition Registers

Addresses: 100111 Port A
101111 Port B
(Read/Write)

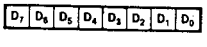


Figure 2-12. Pattern Mask Registers

A reset forces all of these registers to 0. All are read/write.

The pattern specification for each bit is defined as shown in Table 2-8.

The pattern specified by the Pattern Definition registers is a logical (not a physical) specification--this concept is important in understanding the interaction between the pattern match logic and the invert/non-invert logic. An example which shows the logical (as opposed to physical) nature of the specification is: a High level (V_{CC}) on an input pin programmed as inverting matches a 0 specification. Similarly, an output written with a 1 matches a 1 specification even if it is programmed inverting and the output pin is at a Low voltage level.

If the port is programmed as a port with handshake, or if the pattern match mode is OR-Priority Encoded Vector, the transition detection patterns should not be specified (PTn should be set to 0). If the AND mode is specified, no more than one bit should be specified to detect transitions.

2.8 PORT DATA REGISTERS

Ports A and B each have a data path that is composed of three registers: an Input Data register, an Output Data register, and a Buffer register (See Figure 1-2). Output data written to the data register is stored in the Output Data register. Reading the data register returns the contents of the Input Data register. The Buffer register is used to buffer the input and output data if the port is configured as a port with handshake. If so enabled, it is used by the bit port to latch data when a pattern match is detected.

Addresses: 001101 Port A
001110 Port B
(Read/Write)

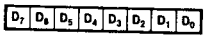


Figure 2-13. Port A and B Data Registers

Table 2-8. Pattern Specification Definition

Pattern Mask Register$_n$	Pattern Transition Register$_n$	Pattern Polarity Register$_n$	Pattern Specification
0	0	0	Bit Masked Off (X)
0	1	0	Any Transition (⇕)
1	0	0	Zero (0)
1	0	1	One (1)
1	1	0	One to Zero Transition (↓)
1	1	1	Zero to One Transition (↑)

External Output Enable--EOE (D_6). By programming this bit to be 1, the output of the counter/timer is provided on the I/O line of the port associated with that particular counter/timer (see Table 4-1). This bit should not be set to 1 unless the corresponding bit is available, (it is not being used as part of an input, output, or bidirectional port, or it is not being used as a handshake or REQUEST/WAIT line). The bit must be programmed to be an output bit in the Data Direction register of its port.

External Count Enable--ECE (D_5). When ECE is set to 1, the counter/timer is put into the counter mode. The I/O line of the port associated with the counter/timer (Table 4-1) is used as an external counter input. On each rising edge of the count input (when the data path is specified non-inverting), the down-counter is decremented. The bit must be available and it must be specified to be an input. (Even if the port bit is programmed as an output bit, the port pin [if enabled] is used as the counter/timer input, allowing the CPU to write this input directly.)

External Trigger Enable--ETE (D_4). When ETE is set to 1, the I/O line of the port associated with the counter/timer (see Table 4-1) is used as a trigger input to the counter/timer. A rising edge (when the data path is specified non-inverting) on this line will cause the down-counter to be loaded. To guarantee that the counter/timer will be triggered on a particular rising edge of the clocking signal (PCLK/2 or counter input), the trigger rising edge must satisfy a setup time to the preceding falling edge of the clocking signal. As in the external count input, the bit of the port must be available for use by the counter/timer, and must be programmed as an input bit. (Even if the port bit is programmed as an output bit, the port pin is used as the counter/timer input [if enabled], allowing the CPU to write this input directly.)

External Gate Enable--EGE (D_3). By setting EGE to 1, the I/O line of the port associated with the counter/timer (see Table 4-1) is used as an external gate input to the counter/timer. If the external gate input is a 0 (assuming the data path is programmed non-inverting), the countdown sequence is suspended; forcing it to a 1 enables the countdown sequence to continue. To guarantee the enabling or disabling of the counter/timer for a particular rising edge of the clocking signal (PCLK/2 or counter input), the gate input must satisfy a setup time to the preceeding falling edge of the clocking signal. Like external trigger input, the bit must be available and it must be programmed to be an input. (Even if the port bit is programmed as an output bit, the port pin is used as the counter/timer input if enabled. This allows the CPU to write this input directly.)

Retrigger Enable Bit--REB (D_2). If REB is set to 0, triggers (internal or external) which occur during a countdown sequence are ignored. If REB is 1, each trigger causes the time constant value to be reloaded and a new countdown sequence to be initiated. When a counter/timer is programmed in square-wave mode, a retrigger will cause the Time Constant value to be reloaded and the new countdown will start on the first half of the square-wave cycle.

Output Duty Cycle Selects--DCS_1 & DCS_0 (D_1 & D_0). These two bits select the output duty cycle according to the information indicated in Table 2-9.

Table 2-9. Output Duty Cycle Selects

DCS_1	DCS_0	Output Duty Cycle
0	0	Pulse Output
0	1	One-Shot Output
1	0	Square Wave Output
1	1	- DO NOT USE -

(See Section 4.2.5 for a description of each output duty cycle type.)

2.10.2 Current Vector Register

When the Current Vector register is read, it returns the interrupt vector that would have been output by the device during an Interrupt Acknowledge cycle if its IEI input had been High. The vector returned corresponds to the highest priority IP independent of the IUS. The order of priority (highest to lowest) is: Counter/Timer 3, Port A, Counter/Timer 2, Port B, Counter/Timer 1. If no enabled interrupts are pending, a pattern of all 1s is output. This is useful in a polled environment or when CPU does not read vectors. This register is a read-only register. Since a reset disables all interrupts, reading the Current Vector register after a reset will return all 1s.

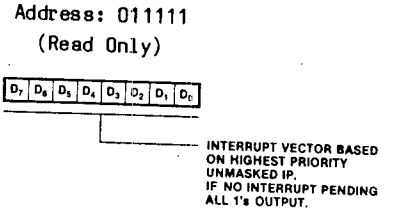


Figure 2-20. Current Vector Register

Chapter 3
I/O Port Operation

3.1 OVERVIEW

There are three I/O ports provided by the CIO device. Ports A and B are 8-bit general-purpose ports; Port C is a 4-bit special-purpose port. There are two port configurations: bit port and port with handshake. All three ports can be programmed as bit ports; only Ports A and B can function as handshake ports.

In general, bit ports are used to provide status input lines and control output lines. When the I/O ports are configured as bit ports, data can be moved in either direction on an individual, pin-by-pin basis. There are up to twenty pins available for this kind of data handling by the three ports.

By configuring Ports A and B as ports with handshake (input, output, or bidirectional), the data can be moved in either direction on a byte-by-byte (parallel 8-bit or 16-bit) basis. Four different handshakes are available: Interlocked, Strobed, Pulsed, or 3-Wire.

Port C is a 4-bit wide, special-purpose port that provides the handshake control lines for Ports A and B, when required. A REQUEST/$\overline{\text{WAIT}}$ line can also be provided to synchronize Port A and B data transfers with DMAs or CPUs. Any Port C bits not used as handshake lines can be used as I/O lines.

Another I/O Port function is to provide external access for the control of three independent counter/timers and distribution of their outputs. Port B provides access for Counter/Timers 1 and 2. Port C provides access to Counter/Timer 3.

Pattern-recognition capability is provided in Ports A and B. In general, it is possible to test data for specified patterns and to generate interrupt requests based on the match obtained.

3.2 PATTERN-RECOGNITION LOGIC OPERATION

Both Ports A and B can be programmed to generate interrupts when a specific pattern is recognized at the port. The pattern-recognition logic is independent of the port application, thereby allowing the port to recognize patterns in all of its configurations. The pattern can be independently specified for each bit as: 1, 0, 0-to-1 transition, 1-to-0 transition, or any transition. Individual bits can be masked off. Three modes of pattern-recognition operation are supported: AND, OR, and OR-Priority Encoded Vector (OR-PEV). A pattern match is defined as the simultaneous satisfaction of all nonmasked bit specifications in the AND mode or the satisfaction of any nonmasked bit specifications in either the OR or OR-PEV modes.

The pattern specified in the Pattern Definition register assumes that the data path is programmed to be non-inverting. If an input bit in the data path is programmed to be inverting, the pattern detected is the opposite of the one specified. Output bits used in the pattern match logic are internally sampled before the invert/non-invert logic.

The operation of the pattern-recognition logic in the various port modes will be described in detail in the following sections.

3.3 BIT PORT OPERATION

Bit ports are used to provide the CPU with input lines to monitor status, and with output lines to provide control. There are up to twenty bits available for this type of data handling provided by the three ports of the CIO: eight each by Ports A and B and four by Port C.

In summary, then, careful interrupt testing and handling is required if ITB = 1 and the pattern match logic is enabled.

Interrupt on Match Only (IMO = 1) Specified

When the Interrupt on Match Only (IMO) bit of the Port Mode Specification register is set to 1, an interrupt will be generated only when the data moved into the Input Data register matches the pattern specification. For input ports, the IMO capability is especially useful when data transfer is under the control of an external device (for example, a DMA controller). In this way the bulk of data transfers can be accomplished without interrupts (that is, without involvement of the CPU), by having an interrupt generated only when the match pattern in encountered.

NOTE

IMO must be 0 if either ITB or SB = 1, or if the port is a bit port.

3.4.2.2 Handshake Types

The operation of the Port A and B input handshakes is explained in this section by describing in detail the sequence of operations performed by an input port programmed with the Interlocked Handshake. Any differences encountered when using the other handshakes will then be described. Table 3-1 identifies the handshake lines furnished by Port C bits for Ports A and B.

Interlocked Input Handshake

As noted in Section 3.3, the Interlocked Input Handshake requires the input port to not indicate that it is ready for data until the data source indicates that the previous byte of data is no longer available, thereby acknowledging that the input port has accepted the previous byte. A primary benefit of Interlocked Handshake port configuration is that it allows the CIO to communicate directly with a variety of other devices without the need for intervening external logic. Devices such as another Z-CIO/CIO, an FIO, an FIFO, a Z8 Port, etc., can be directly connected and serviced. Figure 3-2 shows two interconnected CIOs: output port's $\overline{DAV}$ output connects to input port's $\overline{ACKIN}$ input and input port's RFD output connects to output port's $\overline{ACKIN}$ input.

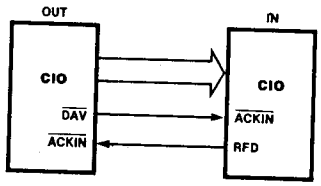


Figure 3-2. Two Interconnected CIOs Using Interlocked Handshake

In Interlocked Handshake mode (Figure 3-3), on the falling edge of the Acknowledge Input ($\overline{ACKIN}$), the data on the port input lines is latched in the Buffer register. This fills the Buffer register and the Ready for Data (RFD) output is pulled Low. If the Input Data register is empty, the data is moved to it ("emptying" the Buffer register) and the Input Data register Full (IRF) flag is automatically set to 1. When the Buffer register becomes empty (and if $\overline{ACKIN}$ is High), the RFD line will return High only if the $\overline{ACKIN}$ input is High. This achieves the interlock.

The following example provides a step-by-step analysis of a double-buffered input port using Interlocked Handshake. (This description uses Figure 3-3 as reference).

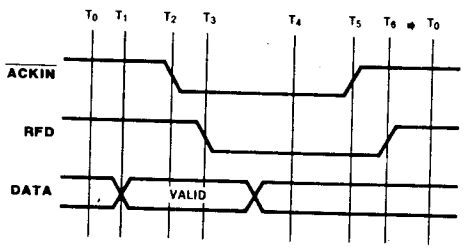


Figure 3-3. Interlocked Input Handshake Timing Diagram

T_0. $\overline{ACKIN}$ and RFD are both High. $\overline{ACKIN}$ High indicates that the data is not valid; RFD High indicates that the Buffer register is empty and ready for data.

T_1. Data on port pins becomes valid.

T_2. $\overline{ACKIN}$ goes Low, indicating that the data is valid, and causing it to be latched into the Buffer register.

T_3. RFD goes Low, indicating that the Buffer register is full and the port is not ready for more data.

T_4. The data is transferred into the Input Data register, the Input Data register Full (IRF) flag goes High and the Buffer register is emptied. The port is now ready for the next byte of data. RFD could go High if $\overline{ACKIN}$ is High; but because $\overline{ACKIN}$ is Low, RFD stays Low.

T_5. $\overline{ACKIN}$ goes High.

T_6 **becomes** T_0. RFD goes High, concluding the handshake process; the cycle is ready to repeat.

Strobed Input Handshake

The Strobed Handshake (Figure 3-4) operates in the same way as the Interlocked Handshake, except that the rising edge of the RFD output is independent of $\overline{ACKIN}$ going High. As soon as the Buffer register is emptied, RFD goes High, even if $\overline{ACKIN}$ is still Low. In all other respects, the two handshakes are the same. The falling edge of the $\overline{ACKIN}$ input "strobes" the data into the port.

The following example provides a step-by-step analysis of an input port configured as double-buffered and using Strobed Handshake. (This description uses Figure 3-4 as reference.)

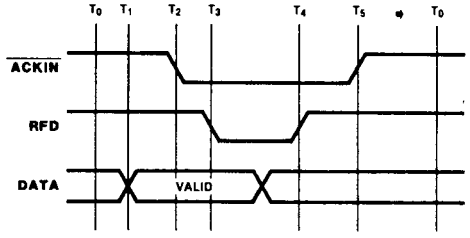


Figure 3-4. Strobed Input Handshake Timing Diagram

T_0. $\overline{ACKIN}$ and RFD are both High. $\overline{ACKIN}$ High indicates that the data is not valid; RFD High indicates that the Buffer register is empty and ready for data.

T_1. Data on port pins becomes valid.

T_2. $\overline{ACKIN}$ goes Low, indicating that the data is valid, and causing it to be latched in the Buffer register.

T_3. RFD goes Low, indicating that the Buffer register is full and the port is not ready for more data.

T_4. The data is moved into the Input Data register, the Input Data register Full (IRF) flag goes High, the Buffer register is emptied, and RFD goes High.

T_5 **becomes** T_0. $\overline{ACKIN}$ is High; the cycle is ready to repeat.

tells the Talker when the last Listener is ready to receive data (final Listener's RFD goes High). The Talker then tells the Listeners that data is now available by bringing $\overline{DAV}$ Low.

Each Listener, working at its individual pace, signals when data reception is done by letting its DAC line go High. The wired-AND DAC signal will tell the Talker when the last Listener has accepted the current data (the last Listener's DAC finally goes High).

The Talker then tells the Listeners that the data is no longer valid ($\overline{DAV}$ goes High). Each Listener puts DAC Low and, when ready for new data, puts RFD high.

The wired-AND RFD and the Low DAC tells the Talker that all Listeners are ready for new data, and the cycle is ready to begin again.

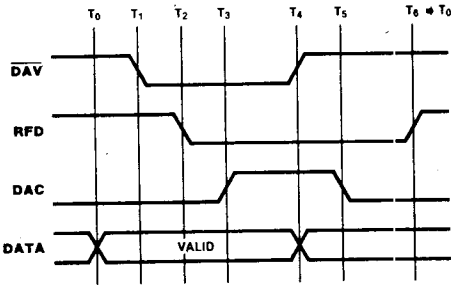


Figure 3-7. 3-Wire Input Handshake Timing Diagram

This procedure is in agreement with the IEEE-488 3-Wire Handshake.

The following example provides a step-by-step analysis of an input port configured as double-buffered and using the 3-Wire Handshake. (This description uses Figure 3-7 as reference).

T_0. $\overline{DAV}$ and RFD are both High. $\overline{DAV}$ High indicates that the data is not valid.

T_1. $\overline{DAV}$ goes Low, indicating that the data is ready to be read and that the input ports are ready for data (the interlock requires RFD to be High before the output port can lower $\overline{DAV}$. The data is latched into the input port Buffer register.

T_2. RFD goes Low, indicating that the Buffer register is full and the port is not ready for more data.

T_3. The individual input ports allow DAC to go High. The wire-ANDed DAC goes High, indicating that the data was received by all input ports.

T_4. $\overline{DAV}$ goes High as the start of the completion of data handling handshake, acknowledging that the data was received.

T_5. DAC goes Low as the data transfer is completed.

T_6 becomes T_0. When their Buffer registers are empty, the individul input ports allow RFD to go High. The wire-ANDed RFD goes High, indicating that the port is ready for the next byte; the cycle is ready to repeat.

3.4.3 Output Port With Handshake

Output ports handle data movement from the CPU to the CIO port pins. This allows the writing of 8-bit (or 16-bit if Ports A and B are linked) data to external devices. (See Figure 3-8.)

There are two Bit Path Definition registers that can affect output port operation: The data path

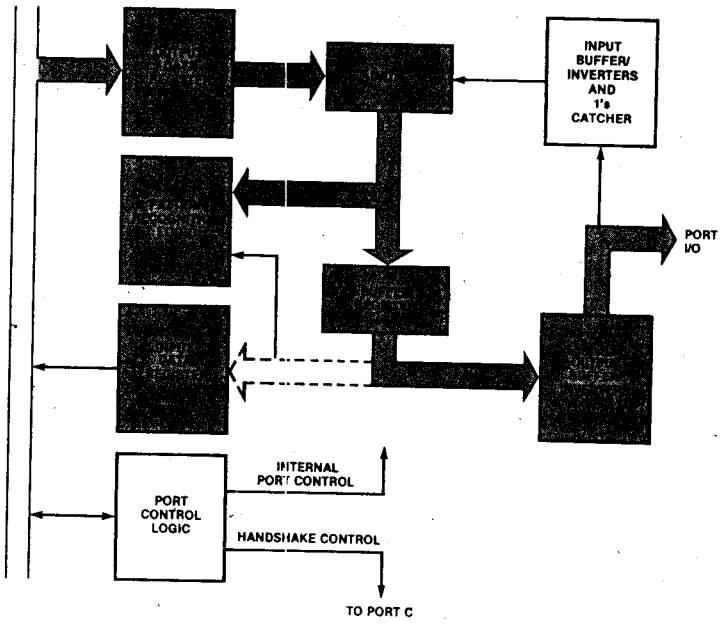


Figure 3-8. Output Port Data Path

is modified as specified by the Data Path Polarity register (see Section 2.6.1); and the Special I/O Control register allows selection of either normal or open-drain outputs (see Section 2.6.3).

When a port is programmed in the output mode, its Input Data Register Full (IRF) flag of the Port Command and Status register is automatically held at 0.

Because the port operation is independent of the handshake, the port operation modes will be examined in this section independent of handshake types. This will be followed by an examination of the four handshake types (Interlocked, Strobed, Pulsed, and 3-Wire) in the output port context.

3.4.3.1 Basic Modes of Operation

There are three independent modes of operation that, taken together, characterize a particular output port configuration. These modes of operation are:

- double- or single-buffered
- interrupt on one or two bytes
- using or not using pattern match logic

Double-Buffered (SB = 0)

The CPU writes data to the Output Data register. The data is moved to the Buffer register if it is empty. When the output port is specified as double-buffered (SB = 0) in the Port Mode Specification register, the data move to the Buffer register "empties" the Output Data register, setting the Output Data Register Empty (ORE) flag; the CPU can then write another byte into the Output Data register. The falling edge of $\overline{\text{ACKIN}}$ indicates that the data has been taken, and empties the Buffer register. Reading the Input Data register will return the current value in the Buffer register.

The $\overline{\text{DAV}}$ output tells receivers that the output port data is available and valid when this signal is Low.

The Interrupt on Two Bytes (ITB) control bit of the Port Mode Specification register determines when IP is set and when an interrupt should be requested.

While programmed to interrupt on every byte (ITB = 0), Interrupt Pending (IP) of the Port

T_S becomes T_0. $\overline{ACKIN}$ goes High, indicating that the input port is ready for data; the cycle is ready to repeat.

Pulsed Output Handshake

The Pulsed Handshake operates exactly like the Interlocked Handshake with Counter/Timer 3 inserted internally in the $\overline{DAV}$ output path (see Figure 3-11). The timer is triggered on the falling edge of an internal $\overline{DAV}$ signal. The output of the timer is inverted and used as the Data Available output for the handshake. The interlock is between the $\overline{ACKIN}$ input and the internal $\overline{DAV}$ signal (the internal $\overline{DAV}$ cannot go Low until $\overline{ACKIN}$ is High). Because all the capabilities of Counter/Timer 3 are available for use, many operations are possible depending on how the timer is programmed. However, since only Counter/Timer 3 is used, only one port can have Pulsed Handshake at a time. The deskew timers can be used to delay the internal $\overline{DAV}$ signal as described before.

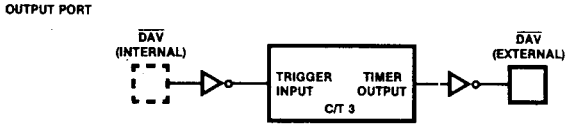


Figure 3-11. Pulsed Output Handshake Counter/Timer Insertion

If Counter/Timer 3's output duty cycle is programmed in the pulse mode, then TC cycles (where TC is the value programmed in the counter/timer Time Constant register) after the internal $\overline{DAV}$ falling edge is detected, the $\overline{DAV}$ output falls and the external $\overline{DAV}$ rises a cycle later.

If the counter is programmed with the one-shot duty cycle, then the $\overline{DAV}$ output falls as soon as the external falling edge on the internal $\overline{DAV}$ signal is detected; it rises TC cycles later. When the counter duty cycle is selected to be square-wave, the $\overline{DAV}$ output goes Low TC cycles after internal $\overline{DAV}$ falls and it stays Low for TC cycles. The duty cycle selected for Counter/Timer 3 determines which $\overline{DAV}$ outputs are available (see the timing diagrams in Figure 3-12).

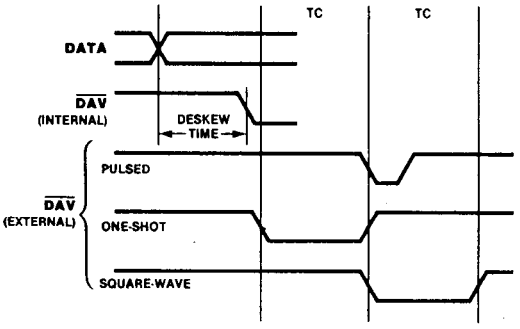


Figure 3-12. Pulsed Output Handshake Counter/Timer Duty Cycles

Many simple interfaces can be made with the Pulsed Handshake by linking the $\overline{DAV}$ output to the $\overline{ACKIN}$ input. For example, if the duty cycle selected for Counter/Timer 3 is square-wave, the port will provide valid data with a setup of TC clock cycles to the external $\overline{DAV}$ falling edge (even longer if the deskew timer is enabled). Also the $\overline{DAV}$'s Low time will be TC clock cycles. This could be used for interfacing to a device which requires a large data setup time to a strobe and a minimum time between characters.

3-Wire Output Handshake

The 3-Wire Handshake (Figure 3-13) is the same as the Interlocked Handshake, except that the role of the $\overline{ACKIN}$ input is replaced by two signals: Ready for Data (RFD) and Data Accepted (DAC). This nomenclature is consistent with the IEEE-488 specification.

When the output port Buffer register is full, its data is available to send. However, the 3-Wire Interlock requires that the receiver(s) first signal that it is ready for data by having DAC Low and raising RFD High (the interlock).

If the deskew timer is enabled, the deskew countdown starts with data moved into the Buffer register. On deskew timeout, the $\overline{DAV}$ signal goes Low; the data has been valid for the whole Deskew count. If the deskew timer is not enabled, the output port then immediately lowers $\overline{DAV}$, signaling that the data is available.

3.4.6 Linked Port Operation

Ports A and B can be linked to form a 16-bit port by programming a 1 in the Port Link Control (PLC) bit of the Master Configuration Control register. In this mode, only Port A's Handshake Specification and Status registers are used. Port B must be specified as a bit port. When linked, only Port A has pattern-match capability. Port B's pattern-match capability must be disabled. Also, when the ports are linked, Port B's Data register must be read or written before Port A's. The PLC bit must be set to 1 before the ports are enabled.

Chapter 4
Counter/Timer Operation

4.1 COUNTER/TIMER ARCHITECTURE

The three independent 16-bit counter/timers each consist of a presettable 16-bit down-counter, a 16-bit Time Constant register, a 16-bit Current Counter register, an 8-bit Mode Specification register, an 8-bit Command and Status register, and the associated control logic that links these registers.

The flexibility of the counter/timers is enhanced by the provision of up to four lines per counter/timer (counter input, gate input, trigger input, and counter/timer output) for direct external control and status. Counter/Timer 1's external I/O lines are provided by the four most-significant bits of Port B. Counter/Timer 2's external I/O lines are provided by the four least-significant bits of Port B. Counter/Timer 3's external I/O lines are provided by the four bits of Port C. The utilization of these lines (Table 4-1) is programmable on a bit-by-bit basis via the Counter/Timer Mode Specification registers.

When external counter/timer I/O lines are to be used, the associated port lines must be vacant and programmed in the proper data direction. Lines used for counter/timer I/O have the same characteristics as simple input lines. They can be specified as inverting or non-inverting, and can be read and used with the pattern-recognition logic. They can also include the 1's catcher input.

4.2 COUNTER/TIMER SEQUENCE OF EVENTS

The following discussion assumes that the inputs and outputs are programmed non-inverting.

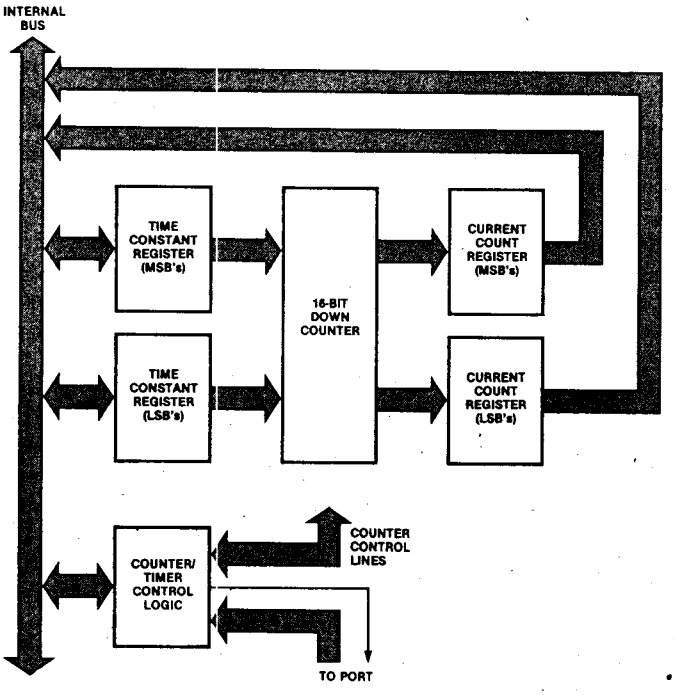


Figure 4-1. Counter/Timer Block Diagram

when a terminal count is reached, the countdown sequence stops. If the C/$\overline{SC}$ bit is 1 each time the count-down counter reaches 1, the next cycle causes the time constant value to be reloaded. The time constant value may be changed by the CPU, and on reload, the new time constant value is loaded. **This must be done with care.**

Each time the counter reaches terminal count, its Interrupt Pending (IP) bit is set to 1, and if interrupts are enabled (IE = 1), an interrupt request is generated. If a terminal count occurs while IP is already set, an internal error flag is set. As soon as IP is cleared, it is forced to a 1 along with the Interrupt Error (ERR) flag. Errors that occur after the internal flag is set are ignored. ERR is cleared to 0 when the corresponding IP is cleared.

4.2.5 Counter/Timer Output

There are three duty cycles available for the timer/counter output: pulse, one-shot, and square-wave. Figure 4-4 shows the counter/timer timing diagrams. When the Pulse mode is specified, the output goes High for one cycle, beginning when the down-counter leaves the count of 1. In the One-Shot mode, the output goes High when the counter/timer is triggered and goes Low when the down-counter reaches 0. When the square-wave output duty cycle is specified, the counter/timer goes through two full sequences for each cycle. The initial trigger causes the down-counter to be loaded and the normal count-down sequence to begin. When a 1 count is detected on the down-counter's clocking edge, the output goes High and the time constant value is reloaded. On the clocking edge, when both the down-counter and the output are 1's, the output is forced Low.

4.2.6 Linked Sequence

Counter/Timers 1 and 2 can be linked internally in three different ways. Counter/Timer 1's output (inverted) can be used as Counter/Timer 2's trigger, gate, or counter input. When linked, the counter/timers have the same capabilities as when used separately. However, when they are linked, they should be linked before they are enabled. The only restriction is that when Counter/Timer 1 drives Counter/Timers 2's count input, Counter/Timer 2 must be programmed with its external count input disabled (ECE = 0).

The initialization procedure, then, is the same as for individual counter/timers, except that the linking bits need to be appropriately set.

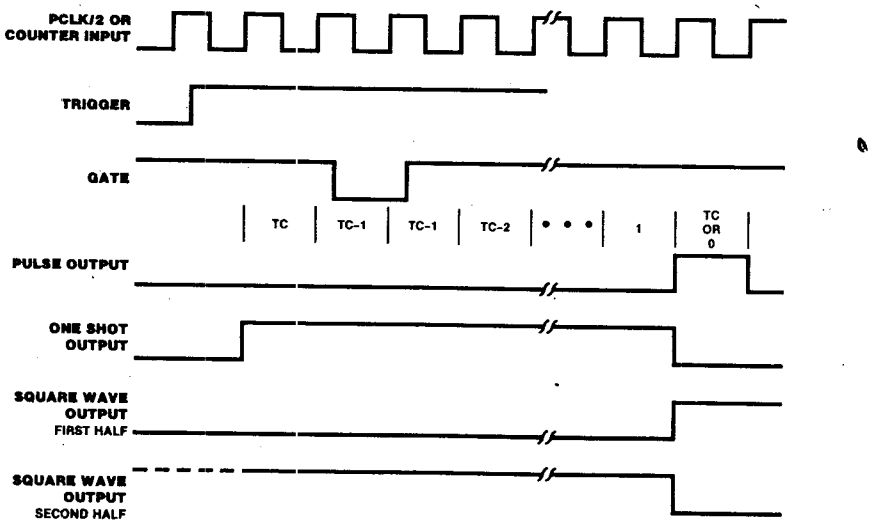


Figure 4-4. Counter/Timer Timing Diagram

5.3.3 Inhibiting Preemption by Lower-Priority Sources

When $\overline{DS}$ (Z8036) or $\overline{RD}$ (Z8536) falls during an Interrupt Acknowledge cycle, the IUS corresponding to the highest unmasked IP is automatically set to 1. As long as IUS is set, IEO is held Low, prohibiting interrupt requests from lower-priority interrupt sources. This guarantees that an interrupt service routine will not be interrupted to service a lower-priority interrupt. IUS can be reset to 0 only by writing to the corresponding Counter/Timer or Port Command and Status register. It is not cleared automatically. IUS can be cleared before interrupt servicing is complete if lower-priority interrupts wish to be recognized. However, IP must be cleared or a second interrupt request will be generated.

The Disable Lower Chain (DLC) bit is included to allow the CPU to modify the system daisy-chain. When the DLC bit is set to 1, the CIO's IEO is forced Low (independent of the state of the CIO or its IEI input) and interrupts from all lower-priority devices are disabled.

Daisy-chain operation is handled differently between the Z8000 peripherals and the Z80 peripherals--however, they are compatible. (Refer to Interfacing 8500 Peripherals to the Z80, Microcomputer Applications Reference Book, document #00-2145-01). The CIO forces IEO Low when IEI is Low, or when an IUS is 1 (except during an Interrupt Acknowledge cycle with an unmasked IP = 1 when IEO is also forced Low).

The Z80 peripherals (CTC, PIO, DMA, and SIO) normally force IEO Low if IEI is Low, or if either IP or IUS is set. However, they use the Z80 Return from Interrupt Instruction (RETI ED_H - $4D_H$) to automatically clear the highest IUS set. To implement this when an ED is decoded as the first byte of an instruction fetch, Z80 peripherals inhibit IP from affecting the daisy-chain.

Although the daisy-chains are different, during critical times (during an Interrupt Acknowledge or when a RETI instruction is executed), they are the same and are therefore compatible.

5.3.4 Identification of the Highest-Priority Interrupt Request; The Use of Vectors.

As part of the Interrupt Acknowledge cycle, the CIO is capable of responding with an 8-bit interrupt vector that specifies the highest-priority interrupt requestor (see Table 5-1). The vector is output when $\overline{DS}$ (Z8036) or $\overline{RD}$ (Z8536) goes Low and IUS is set. The identification vector is a key item of the Z8000 Family interrupt handling logic. It speeds the information passing and can, if desired, include additional status information identifying the cause of the interrupt as well as the source identification.

The CIO contains three vector registers: one for Port A, one for Port B, and one shared by the three counter/timers. Unique identification information can be placed by the user in the Interrupt Vector register for each interrupt source needed during initialization. The vector output can be modified to include status information to pinpoint the cause of interrupt. A Vector Includes Status (VIS) control bit controls whether or not the vector includes status.

Each base vector has its own VIS bit and is controlled independently. When MIE = 1, reading the base vector register always includes status, independent of the state of the VIS bit. All the information obtained by the vector, including status, can thus be obtained with one additional instruction when VIS is set to 0. When MIE = 0,

Table 5-1. Interrupt Vector Encoding if Vector Includes Status

Port Vector Status

OR-Priority Encoded Vector Mode:

D_3	D_2	D_1	
x	x	x	Number of highest-priority bit with a match

All Other Modes:

D_3	D_2	D_1	
ORE	IRF	PMF	Normal
0	0	0	Error

Counter/Timer Status

D_2	D_1	
0	0	Counter/Timer 3
0	1	Counter/Timer 2
1	0	Counter/Timer 1
1	1	Error

Some time after $\overline{INT}$ has been pulled Low, the CPU initiates an Interrupt Acknowledge transaction. Between the falling edge of $\overline{INTACK}$ and the falling edge of $\overline{RD}$, the IEI/IEO daisy-chain settles. Any peripheral with one of its interrupts pending (IP is 1) or one of its interrupts under service (IUS is 1) holds its IEO line Low; all other conditions make IEO follow IEI.

When $\overline{RD}$ falls, only the highest-priority interrupt source with a pending interrupt (IP is 1) has its IEI input High, its IE bit set to 1, and its IUS bit set to 0. This is the interrupt source being acknowledged, and at this point it sets its IUS bit to 1. If its NV bit is 0, the Z8536 identifies itself by placing its interrupt vector from the corresponding interrupt vector register on data lines D_0-D_7. If NV is 1, the Z8536's D_0-D_7 lines remain floating, allowing external logic to supply a vector.

If the Z8536 VIS is 1, the vector also contains status information (see Table 5-1) which further identifies the source of the interrupt within the Z8536. If VIS is 0, the vector held in the interrupt vector is output without status included (base vector). The bit codes are in Section 2.9.1.

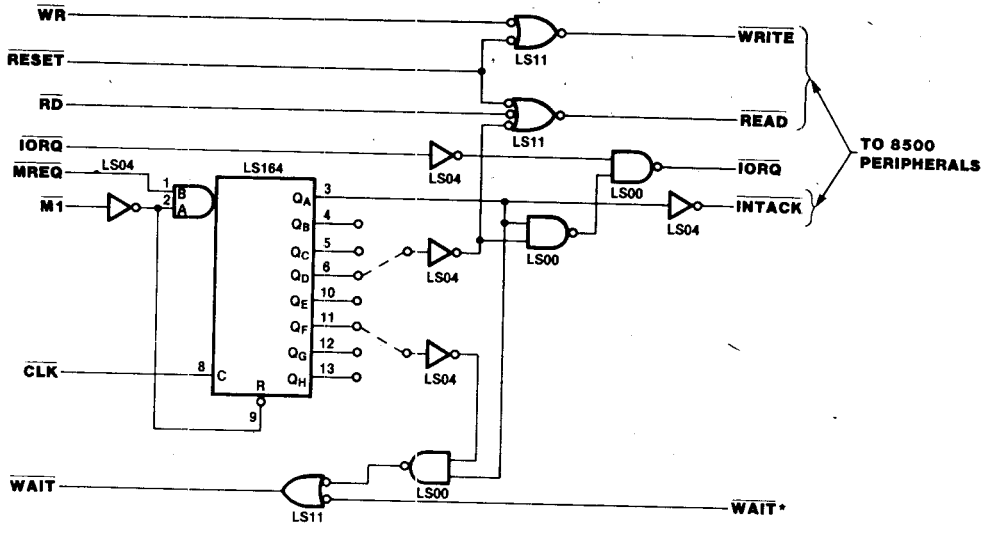


Figure 5-4. $\overline{WAIT}$ and $\overline{INTACK}$ Generation Logic

Chapter 8
Z8536 (CIO) Interfacing

8.1 INTRODUCTION

This section provides information on pin functions and assignments and functional timing diagrams for the Z8536.

8.2 FEATURES

The following features of the Z8536 are not obvious without reference to the ac timing diagrams in the Z8536 Product Specification, document #00-2021-A0.

- The state machine conventions relating to programming and register addresssing (see Section 6.5.2) must be followed.
- PCLK can be asynchronous with respect to the CPU--it does not have to be the same as the CPU. However, a minimum of three PCLK cycles must occur between two successive accesses of the Z8536 (that is, between the end of the first access and the beginning of the second access).
- The $\overline{\text{INTACK}}$ input is synchronous, that is, $\overline{\text{INTACK}}$ and PCLK have a relationship that must be maintained.
- The assertion of REQUEST is synchronous with PCLK.
- The release of $\overline{\text{WAIT}}$ is synchronous with PCLK.

8.3 PIN FUNCTIONS AND ASSIGNMENTS

The Z8536 is configured for general microcomputer interface controls and timing. The pin functions and assignments are shown in Figures 8-1 and 8-2. Section 8.4 is a description of the pin functions for the Z8536 CIO.

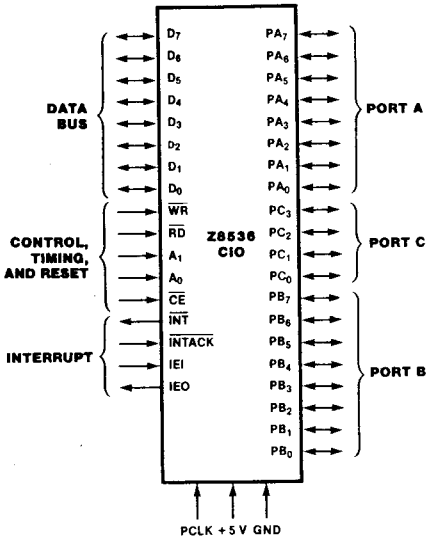


Figure 8-1. Z8536 (CIO) Pin Functions

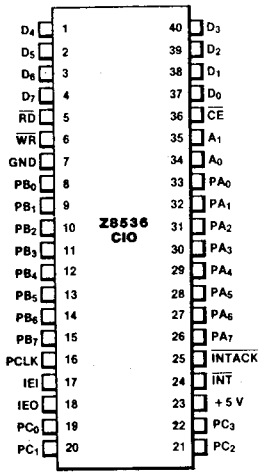
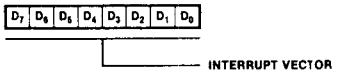


Figure 8-2. Z8536 (CIO) Pin Assignments

Registers (Continued)

Interrupt Vector Register
Addresses: 000010 Port A
000011 Port B
000100 Counter/Timers
(Read/Write)



PORT VECTOR STATUS

PRIORITY ENCODED VECTOR MODE:

D3	D2	D1	
x	x	x	NUMBER OF HIGHEST PRIORITY BIT WITH A MATCH

ALL OTHER MODES:

D3	D2	D1	
ORE	IRF	PMF	NORMAL
0	0	0	ERROR

COUNTER/TIMER STATUS

D2	D1	
0	0	C/T 3
0	1	C/T 2
1	0	C/T 1
1	1	ERROR

Current Vector Register
Address: 011111
(Read Only)

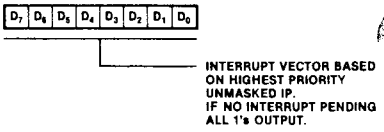


Figure B-7. Interrupt Vector Registers

Register Address Summary

Main Control Registers

Address	Register Name
000000	Master Interrupt Control
000001	Master Configuration Control
000010	Port A's Interrupt Vector
000011	Port B's Interrupt Vector
000100	Counter/Timer's Interrupt Vector
000101	Port C's Data Path Polarity
000110	Port C's Data Direction
000111	Port C's Special I/O Control

Most Often Accessed Registers

Address	Register Name
001000	Port A's Command and Status
001001	Port B's Command and Status
001010	Counter/Timer 1's Command and Status
001011	Counter/Timer 2's Command and Status
001100	Counter/Timer 3's Command and Status
001101	Port A's Data
001110	Port B's Data
001111	Port C's Data

Counter/Timer Related Registers

Address	Register Name
010000	Counter/Timer 1's Current Count-MSBs
010001	Counter/Timer 1's Current Count-LSBs
010010	Counter/Timer 2's Current Count-MSBs
010011	Counter/Timer 2's Current Count-LSBs
010100	Counter/Timer 3's Current Count-MSBs
010101	Counter/Timer 3's Current Count-LSBs
010110	Counter/Timer 1's Time Constant-MSBs
010111	Counter/Timer 1's Time Constant-LSBs
011000	Counter/Timer 2's Time Constant-MSBs
011001	Counter/Timer 2's Time Constant-LSBs
011010	Counter/Timer 3's Time Constant-MSBs
011011	Counter/Timer 3's Time Constant-LSBs
011100	Counter/Timer 1's Mode Specification
011101	Counter/Timer 2's Mode Specification
011110	Counter/Timer 3's Mode Specification
011111	Current Vector

Port A Specification Registers

Address	Register Name
100000	Port A's Mode Specification
100001	Port A's Handshake Specification
100010	Port A's Data Path Polarity
100011	Port A's Data Direction
100100	Port A's Special I/O Control
100101	Port A's Pattern Polarity
100110	Port A's Pattern Transition
100111	Port A's Pattern Mask

Port B Specification Registers

Address	Register Name
101000	Port B's Mode Specification
101001	Port B's Handshake Specification
101010	Port B's Data Path Polarity
101011	Port B's Data Direction
101100	Port B's Special I/O Control
101101	Port B's Pattern Polarity
101110	Port B's Pattern Transition
101111	Port B's Pattern Mask