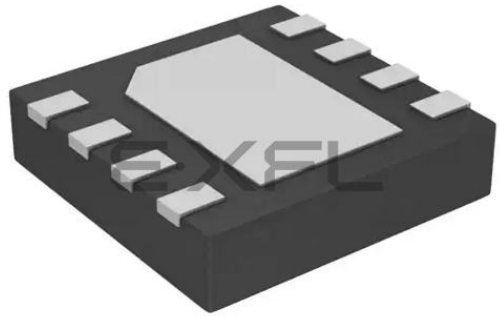

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Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
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Supplier Device Package	8-UDFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18313-i-rf

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Table 2-1. Z8036/Z8536 Z-CIO/CIO Register Summary--Continued

Internal Address (Binary)	Read/Write	Register Name
		Counter/Timer Related Registers
010000	R	Counter/Timer 1 Current Count MS Byte
010001	R	Counter/Timer 1 Current Count LS Byte
010010	R	Counter/Timer 2 Current Count MS Byte
010011	R	Counter/Timer 2 Current Count LS Byte
010100	R	Counter/Timer 3 Current Count MS Byte
010101	R	Counter/Timer 3 Current Count LS Byte
010110	R/W	Counter/Timer 1 Time Constant MS Byte
010111	R/W	Counter/Timer 1 Time Constant LS Byte
011000	R/W	Counter/Timer 2 Time Constant MS Byte
011001	R/W	Counter/Timer 2 Time Constant LS Byte
011010	R/W	Counter/Timer 3 Time Constant MS Byte
011011	R/W	Counter/Timer 3 Time Constant LS Byte
011100	R/W	Counter/Timer 1 Mode Specification
011101	R/W	Counter/Timer 2 Mode Specification
011110	R/W	Counter/Timer 3 Mode Specification
011111	R	Current Vector
		Port A Specification Registers
100000	R/W	Port A Mode Specification
100001	R/W	Port A Handshake Specification
100010	R/W	Port A Data Path Polarity
100011	R/W	Port A Data Direction
100100	R/W	Port A Special I/O Control
100101	R/W	Port A Pattern Polarity
100110	R/W	Port A Pattern Transition
100111	R/W	Port A Pattern Mask
		Port B Specification Registers
101000	R/W	Port B Mode Specification
101001	R/W	Port B Handshake Specification
101010	R/W	Port B Data Path Polarity
101011	R/W	Port B Data Direction
101100	R/W	Port B Special I/O Control
101101	R/W	Port B Pattern Polarity
101110	R/W	Port B Pattern Transition
101111	R/W	Port B Pattern Mask

* All bits can be read and some bits can be written.

** Also directly addressable in Z8536 using pins A_0 and A_1. (See Table 2-2 and Figures 8-1 and 8-2.)

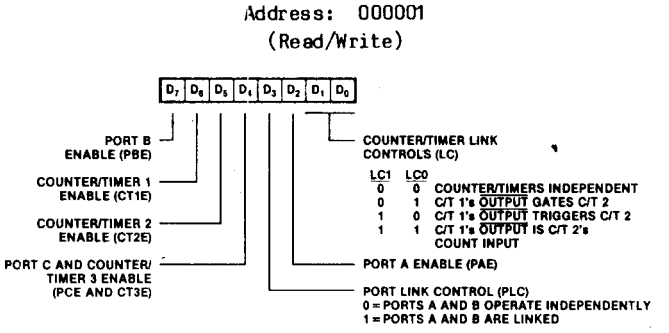


Figure 2-3. Master Configuration Control Register

Port B Enable--PBE (D_7). This bit, when set to 1, allows Port B to operate normally. When cleared to 0, it inhibits the Port B logic from issuing an interrupt request (its IP cannot be set); however, if IP was already set, clearing PBE does not clear IP. While cleared to 0, PBE inhibits READY/$\overline{WAIT}$ assertion, holds all 1's catchers in a transparent condition, and forces the Port B I/O lines into a high-impedance state. The purpose of this bit is to allow Port B to be configured initially without setting its IP erroneously or having its I/O lines go low-impedance until it is safe to do so.

Counter/Timer 1 Enable--CT1E (D_6). When cleared to 0, Counter/Timer 1 is put into an initialized state: its IP cannot be set (however, if IP was already set, clearing CT1E does not clear IP), the Count In Progress (CIP) flag is cleared, Read Counter Control (RCC) is forced to 0, and all trigger inputs are ignored. Setting CT1E to 1 allows the counter/timer to function normally.

Counter/Timer 2 Enable--CT2E (D_5). The CT2E bit performs the same function for Counter/Timer 2 that CT1E performs for Counter/Timer 1.

Port C and Counter/Timer 3 Enable--PCE and CT3E (D_4). This bit enables both Port C and Counter/Timer 3. The function is the same as D_7 (PBE) and D_6 (CT1E) for Port B and Counter/Timer 1, respectively. In addition, while this bit is cleared to 0, the handshake logic for Ports A and B is forced into an idle state and the internal Acknowledge Input ($\overline{ACKIN}$) signal is forced High. This allows the start-up of handshake operations to be precisely controlled.

Port Link Control--PLC (D_3). When PLC is set to 1, Ports A and B are linked to form a 16-bit port. In this mode, only the Port A Handshake Specification and Command and Status registers are used. Port B must be specified as a bit port and its pattern match capability must be disabled. Also, when linked, the Port B data register must be read or written before the Port A data register. A 0 in the PLC bit allows the ports to operate independently. If the ports are to be linked, this bit must be set before the ports are enabled.

Port A Enable--PAE (D_2). The Port A Enable bit performs the same function for Port A that the Port B Enable bit (D_7) performs for Port B.

Counter/Timer Link Controls--LC_1 & LC_0 (D_1 & D_0). These two bits specify if and how Counter/Timers 1 and 2 are linked. The Counter/Timers must be linked before they are enabled. The various configurations are shown in Table 2-3.

Table 2-3. Counter/Timer Link Controls

LC_1	LC_0	Configuration
0	0	Counter/Timers are independent
0	1	Counter/Timer 1's output (inverted) gates Counter/Timer 2
1	0	Counter/Timer 1's output (inverted) triggers Counter/Timer 2
1	1	Counter/Timer 1's output (inverted) is Counter/Timer 2's count input (Counter/Timer 2's External Count Enable* bit must be cleared to 0)

* (See Section 2.9.1 for description of External Count Enable bit.)

Table 3-1. Port C Pin Utilization

Port A/B Configuration	Port C Bits: Pin C_3	Pin C_2	Pin C_1	Pin C_0
Ports A & B = Bit Ports	Bit I/O	Bit I/O	Bit I/O	Bit I/O
Port A = Input or Output port (Interlocked, Strobed, or Pulsed Handshake)*	RFD or $\overline{DAV}$	$\overline{ACKIN}$	REQUEST/$\overline{WAIT}$ or Bit I/O	Bit I/O
Port B = Input or Output port (Interlocked, Strobed, or Pulsed Handshake)*	REQUEST/$\overline{WAIT}$ or Bit I/O	Bit I/O	RFD or $\overline{DAV}$	$\overline{ACKIN}$
Port A or B = Input port (3-Wire Handshake)	RFD (Output)	$\overline{DAV}$ (Input)	REQUEST/$\overline{WAIT}$ or Bit I/O	DAC (Output)
Port A or B = Output port (3-Wire Handshake)	$\overline{DAV}$ (Output)	DAC (Input)	REQUEST/$\overline{WAIT}$ or Bit I/O	RFD (Input)
Port A or B = Bidirectional port (Interlocked or Strobed Handshake)	RFD or $\overline{DAV}$	$\overline{ACKIN}$	REQUEST/$\overline{WAIT}$ or Bit I/O	IN/$\overline{OUT}$

* Both Ports A & B can be specified input or output with Interlocked, Strobed, or Pulsed Handshake at the same time if neither uses REQUEST/$\overline{WAIT}$. However, only one port can use the Pulsed Handshake at a time.

3.4.1 Four Handshake Modes

There are four handshake modes: Interlocked, Strobed, Pulsed, and 3-Wire.

3.4.1.1 Interlocked Handshake

In the Interlocked Handshake mode, the action of the CIO must be acknowledged by the external device before the next action can take place. An output port does not indicate that new data is available until the external device indicates it is ready for the data. Similarly, an input port does not indicate that it is ready for new data until the data source indicates that the previous byte of data is no longer available, thereby acknowledging the input port's acceptance of the last byte. This handshake allows the CIO to interface directly to the port of a Z8 microcomputer, a UPC, an FIO, an FIFO, or to another CIO port, etc., with no external logic.

3.4.1.2 Strobed Handshake

In the Strobed Handshake mode, data is "strobed" into or out of the port by the external logic. The falling edge of the Acknowledge Input ($\overline{ACKIN}$) strobes data into or out of the port. In contrast to the Interlocked Handshake, the signal indicating that the port is ready for another data transfer operates independently of the $\overline{ACKIN}$ input. The external logic must ensure that data does not transfer at too fast or too slow a rate.

3.4.1.3 Pulsed Handshake

The Pulsed Handshake mode is designed to interface to mechanical-type devices which require data to be held for long periods of time and need relatively wide pulses to gate the data into or out of the device. The logic is the same as the Interlocked Handshake mode, except that an internal counter/timer (Counter/Timer 3) is linked to the

T_0. $\overline{ACKIN}$ and RFD are both High. $\overline{ACKIN}$ High indicates that the data is not valid; RFD High indicates that the Buffer register is empty and ready for data.

T_1. Data on port pins becomes valid.

T_2. $\overline{ACKIN}$ goes Low, indicating that the data is valid, and causing it to be latched into the Buffer register.

T_3. RFD goes Low, indicating that the Buffer register is full and the port is not ready for more data.

T_4. The data is transferred into the Input Data register, the Input Data register Full (IRF) flag goes High and the Buffer register is emptied. The port is now ready for the next byte of data. RFD could go High if $\overline{ACKIN}$ is High; but because $\overline{ACKIN}$ is Low, RFD stays Low.

T_5. $\overline{ACKIN}$ goes High.

T_6 **becomes** T_0. RFD goes High, concluding the handshake process; the cycle is ready to repeat.

Strobed Input Handshake

The Strobed Handshake (Figure 3-4) operates in the same way as the Interlocked Handshake, except that the rising edge of the RFD output is independent of $\overline{ACKIN}$ going High. As soon as the Buffer register is emptied, RFD goes High, even if $\overline{ACKIN}$ is still Low. In all other respects, the two handshakes are the same. The falling edge of the $\overline{ACKIN}$ input "strobes" the data into the port.

The following example provides a step-by-step analysis of an input port configured as double-buffered and using Strobed Handshake. (This description uses Figure 3-4 as reference.)

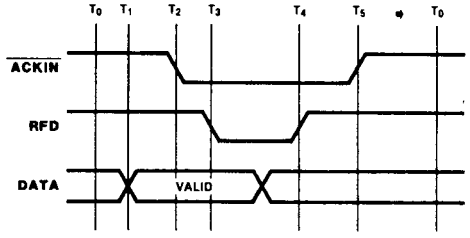


Figure 3-4. Strobed Input Handshake Timing Diagram

T_0. $\overline{ACKIN}$ and RFD are both High. $\overline{ACKIN}$ High indicates that the data is not valid; RFD High indicates that the Buffer register is empty and ready for data.

T_1. Data on port pins becomes valid.

T_2. $\overline{ACKIN}$ goes Low, indicating that the data is valid, and causing it to be latched in the Buffer register.

T_3. RFD goes Low, indicating that the Buffer register is full and the port is not ready for more data.

T_4. The data is moved into the Input Data register, the Input Data register Full (IRF) flag goes High, the Buffer register is emptied, and RFD goes High.

T_5 **becomes** T_0. $\overline{ACKIN}$ is High; the cycle is ready to repeat.

Command and Status register is automatically set to 1 along with Output Data Register Empty (ORE) of the Port Command and Status register when the data is moved out of the Output Data register and into the Buffer register. Writing to the port data register "fills" the Output Data register and automatically clears the IP (hence, ORE = 0 and IP = 0). IP can be cleared (IP = 0) by software command; that is, by writing bits D_7-D_5 of the Port Command and Status register. However, the Output Data register is not "filled" until the data is written. Since IP is set only when data is moved out of the Output Data register, then if the port is enabled (PAE or PBE is set to 1) without writing any data, IP will not be set even though the Output Data register is empty.

While programmed to interrupt on two bytes (ITB = 1), IP is not automatically set to 1 until both the Output Data and Buffer registers are empty; that is, the Buffer register becomes empty while the Output Data register is empty. IP is automatically cleared (IP = 0) when the second byte of data is written by the CPU to the data register. The first data write fills the Output Data register and allows the data to be moved into the Buffer register. The second data write fills the now empty Output Data register and automatically clears the IP. As when ITB = 0, when the port is initially enabled, the IP will not be set nor will an interrupt request be generated until a byte of data is written to it. Data can be written to it after it is initially configured and before it is enabled.

When ITB = 1, the Output Data register should not be written unless IP = 1, even if ORE = 1. Otherwise, the data may be written just as the Buffer register is going empty and as IP is being set. In this case, an interrupt may be requested for a two-byte write, when only one byte is needed, because the first byte has already been written but not output.

NOTE

The IP can be cleared on command. This suggests the following possible sequence for providing byte-by-byte control of the DAV output: writing one byte of data and then clearing IP by command allows an interrupt when the Buffer register is "emptied" by the handshake logic.

Single-Buffered (SB = 1)

When the output port is specified as single-buffered (SB = 1), output data is moved from the Output Data register to the Buffer register as in the double-buffered case. However, when the data is moved into the Buffer register, the Output Data register is not emptied. A copy of the data is maintained there. In this mode, the handshake logic "empties" both registers: when $\overline{ACKIN}$ falls, the Output Data and Buffer registers are emptied, and both ORE and IP are automatically set to 1. Writing the port data register fills the Output Data register and clears IP (ORE = IP = 0).

NOTE

Unlike the double-buffered operation, ITB = 1 does not make sense in single-buffered operation. Thus, when SB = 1, ITB must = 0.

With Pattern Match Added (PMS_1 = PMS_0 ≠ 0)

The port's built-in pattern match logic can be used to test the data as it is coming into or through the data register. The available pattern match modes operate independently of handshake type and are specified by the Pattern Mode Specification bits (PMS_1 and PMS_0). In the output port operation, the AND and the OR modes are available for use, but the OR-PEV is not. This pattern availability for AND and OR logic is a consequence of the pattern being tested as the data is moved into the Input Data register, eliminating access to the transition information. Because of this, transition patterns cannot be used.

The Pattern Match Flag (PMF) of the Port Command and Status register is set to 1 or is cleared to 0 as the data is moved from the Output Data register to the Buffer register.

When ITB = 0, IP is set when data is moved out of the Output Data register. If PMF = 1, writing the data register does not automatically clear the IP--the IP can only be cleared by writing to the Port Command and Status Register. Also, writing the Output Data register does not "fill" it; the Output Data register can be "filled" (and ORE cleared to 0) only if it is written and the IP is cleared, (in any order). Data that is written

Interrupt on Match Only (IMO = 1) Specified

When the Interrupt on Match Only bit of the Port Mode Specification register is set to 1, an interrupt request will be generated only when the data moved out of the Output Data register into the Buffer register matches the pattern specification. For output ports, the IMO capability is especially useful when data transfer is under the control of an external device (for example, a DMA controller). In this way the bulk of the data transfers can be accomplished without interrupts (that is, without involvement of the CPU) by having an interrupt generated only when the match pattern is encountered. The CIO, through the IMO, allows a long string of bytes to be output without interrupts. This is accomplished by simply waiting on a pattern which is inserted at the end of a string to signal the end of the transmission by way of a single CPU interrupt request. This way, many bytes can be moved with only one interrupt request being generated.

NOTE

IMO must be 0 if either ITB or SB = 1, or if the port is a bit port.

3.4.3.2 Handshake Types

The operation of Port A and B output handshakes will be explained by describing in detail the sequence of operations performed by an output port programmed with Interlocked Handshake. Any differences encountered when using the other handshakes will then be described. See Table 3-1 for identification of the handshake lines furnished by Port C bits for Ports A and B.

Deskew Timer Description

Because external devices may require that the data be valid for a certain minimum amount of time prior to the $\overline{DAV}$ signal being pulled Low (to indicate data available), the CIO provides a separate deskew timer for each port. As data is transferred to the Buffer register, the deskew timer is triggered (if the timer is enabled (DTE = 1). After the number of PCLK cycles (up to 16) specified by the deskew timer Time Constant (see Figure 2-5), $\overline{DAV}$ is allowed to go Low (the interlock may keep $\overline{DAV}$ High). The deskew timer does not extend the time from $\overline{ACKIN}$ rising to $\overline{DAV}$ falling. The deskew timer therefore guarantees that the output data is valid for a specified minimum amount of time before $\overline{DAV}$ goes Low.

Deskew timers are available for output ports independent of the type of handshake employed. Each port has a separate 4-bit deskew timer. Thus, the CIO can provide the proper timing to interface to those external devices that require a large data valid to $\overline{DAV}$ falling setup time. For example, the IEEE-488 specification requires data to be valid for 2 microseconds before $\overline{DAV}$ can go Low.

Interlocked Output Handshake

The Interlocked Output Handshake requires that the output port does not indicate that it has data available ($\overline{DAV}$ goes Low) until the receiving port indicates that the previous byte of data has been accepted (indicated by $\overline{ACKIN}$ being High).

Interlocked Handshake port configuration allows the CIO to communicate directly with a variety of other devices without the need for external logic. Devices such as another CIO, FIO, FIFO, Z8 Port, etc., can be interfaced directly. Figure 3-2 shows two interconnected CIOs: the output port's $\overline{DAV}$ output connects to the input port's $\overline{ACKIN}$ input and the input port's RFD output connects to the output port's $\overline{ACKIN}$ input.

In Interlocked Output Handshake mode (Figure 3-9), the CPU writes data into the Output Data register. If the Buffer register is empty, the data is moved to it and on to the port output pins ("emptying" the Output Data register). The Output Data register Empty (ORE) bit in the port Command and Status register is then set to 1 and Data Available ($\overline{DAV}$) handshake line goes Low (if $\overline{ACKIN}$ is High). The CPU can now write another byte into the Output Data register, setting ORE to 0. When

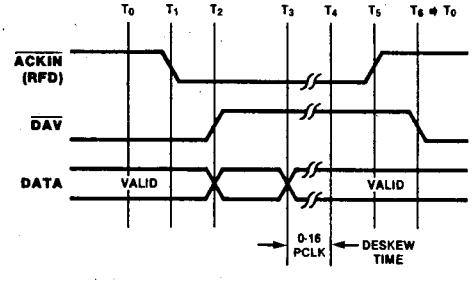


Figure 3-9. Interlocked Output Handshake Timing Diagram

3.4.5.1 REQUEST Line Operation

Operation of the REQUEST line is dependent on the state of the port's Interrupt on Two Bytes (ITB) control bit. When ITB = 0, the REQUEST line goes active as soon as the CIO is ready for a data transfer. If the port is used for the input, the REQUEST line goes High when the Input Data register is full. If the port is used for output, the REQUEST line goes High when the Output Data register is empty. If ITB = 1, REQUEST goes active only if two bytes can be moved. For input, both Input Data and Buffer registers are full, and for output, both Buffer and Output Data registers are empty. REQUEST stays active as long as a byte is available to be read or written. However, if the port is single-buffered or if the Pattern Match Flag is set, REQUEST goes Low when the data is read or written.

In the bidirectional mode, ITB must be 0. Therefore, the REQUEST line reflects the state of the Input or Output Data register, depending on the type of REQUEST line specified.

The DMA-type transfer is facilitated by the use of the Interrupt on Match Only (IMO) control bit in the Port Mode Specification register. In most DMA transfers, the peripheral does not generate an interrupt request. However, the Interrupt on Match Only (IMO) capability of the CIO allows it to interrupt the CPU when there is a specified byte match, such as an end of transfer flag, etc. Except for the specified pattern match, the CPU is not involved in the transfer; the data movement is consequently accomplished much faster. This REQUEST line/IMO pattern match operation can function in all port operating modes.

The SPECIAL REQUEST function is reserved for use with bidirectional ports only. In this case, the REQUEST line indicates the status of the register not being used in the data path at that time. If the IN/$\overline{\text{OUT}}$ line is High (input port), the REQUEST line is High when the Output Data register is empty. If IN/$\overline{\text{OUT}}$ is Low (output port), the REQUEST line goes High when the Input Data register is full. In this mode, both the Input and the Output Data registers can be monitored. The RFD/$\overline{\text{DAV}}$ indicates the state of the register in the data path, and the REQUEST line monitors the register not in the data path.

This line can be used to indicate when to change the CIO direction. For example, if the CIO is a "slave" bidirectional port in the input direction (IN/$\overline{\text{OUT}}$ = High), then when the SPECIAL REQUEST line goes Low (indicating that the Output Data register has a byte to be transferred), the master port can use this as the signal to turn the port around so that the byte can be output.

3.4.5.2 $\overline{\text{WAIT}}$ Line Operation

The REQUEST/$\overline{\text{WAIT}}$ line configured in the $\overline{\text{WAIT}}$ mode is useful to synchronize CPU-to-CIO transactions. For example, when the CPU wants the data transfer to be performed as rapidly as possible, it does not want to wait for an interrupt service routine to tell it that the CIO is ready to receive or supply a byte of data. Rather, the CPU attempts a read or write to the CIO. If $\overline{\text{WAIT}}$ is enabled, and the CIO is not ready for a read or write to it, $\overline{\text{WAIT}}$ is pulled Low and the CPU is forced to wait until the CIO is ready (the Input register becomes full or the Output register becomes empty), signified by the $\overline{\text{WAIT}}$ line going High. The CPU is now released from the $\overline{\text{WAIT}}$ pause and can complete the data transaction.

For an input port, $\overline{\text{WAIT}}$ is pulled Low when an attempt is made to read the Input Data register and the port is empty. For an output port, $\overline{\text{WAIT}}$ is pulled Low when an attempt is made to write to the Output Data register that is still full; the data integrity is maintained in the case of the output port--the data is not overwritten. Action is merely suspended until the write can take place.

In the Z8036, $\overline{\text{WAIT}}$ falling is caused by $\overline{\text{DS}}$ falling. In the Z8536, $\overline{\text{WAIT}}$ is synchronized with either $\overline{\text{RD}}$ or $\overline{\text{WD}}$ falling. $\overline{\text{WAIT}}$, however, may be required to be valid at the CPU prior to this. A practical way to use $\overline{\text{WAIT}}$ with the CIO is to have external logic generate a $\overline{\text{WAIT}}$ cycle automatically, which can then be extended as needed by the CIO.

The release of $\overline{\text{WAIT}}$ in both the Z8036 and the Z8536 is synchronized with the PCLK input. Thus for the Z8036 REQUEST/$\overline{\text{WAIT}}$ function, a PCLK input is required. Also, while the Z8036 is asserting $\overline{\text{WAIT}}$, internal status is updated using PCLK (not $\overline{\text{AS}}$ as it normally does), because $\overline{\text{AS}}$ stops as long as the CPU is $\overline{\text{WAIT}}$ed.

3.4.6 Linked Port Operation

Ports A and B can be linked to form a 16-bit port by programming a 1 in the Port Link Control (PLC) bit of the Master Configuration Control register. In this mode, only Port A's Handshake Specification and Status registers are used. Port B must be specified as a bit port. When linked, only Port A has pattern-match capability. Port B's pattern-match capability must be disabled. Also, when the ports are linked, Port B's Data register must be read or written before Port A's. The PLC bit must be set to 1 before the ports are enabled.

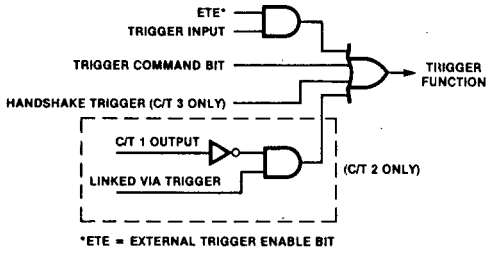


Figure 4-2. Trigger OR-Function Diagram

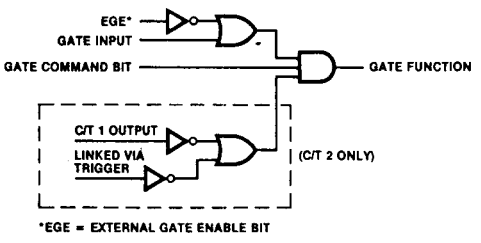


Figure 4-3. Gate AND-Function Diagram

4.2.3 Countdown Sequence

The rate at which the down-counter counts is determined by the mode of the counter/timer. In the Timer mode (the External Count Enable [ECE] bit is 0), the down-counter is clocked internally by a signal that is half the frequency of the PCLK input to the chip. In the Counter mode (ECE is 1), the down-counter is decremented on the rising edge of the counter/timer's counter input.

Once the down-counter is loaded, the countdown sequence continues toward terminal count as long as all of the counter/timers' hardware and software gate inputs are High. The gate inputs are: the Gate Command bit of the Counter/Timer Command and Status register, and the external gate input if enabled in the External Gate Enable bit of the counter/timer Mode Specification register. Also, for Counter/Timer 2 use only, the counter/timer output (inverted) can be used as a gate if linked via the gate in the Counter/Timer Link Controls bits of the Master Configuration Control register. If any of the gate inputs go Low (0), the countdown halts. It resumes when all gate inputs are 1 again. The gate function does not affect the trigger function.

The gate functions as the logical AND of all the potential gates (see Figure 4-3).

NOTE

In order to ensure the enabling or disabling of the counter/timer on a particular rising edge of the clocking signal, sufficient setup time must be allowed. The gate signal must be valid prior to the immediately preceding falling edge of the clocking signal.

The reaction to triggers occurring during a countdown sequence is determined by the state of the Retrigger Enable Bit (REB) in the Mode Specification register. If REB is 0, retriggers are ignored and the countdown continues normally. If REB is 1, each trigger causes the down-counter to be reloaded and the countdown sequence starts over again. If the output is programmed in the Square-Wave mode, a retrigger causes the sequence to start over from the initial load of the time constant.

The state of the down-counter can be determined in two ways: by reading the contents of the down-counter via the Current Count register or by testing the Count In Progress (CIP) status bit in the Command and Status register. The CIP status bit is set when the down-counter is loaded; it is reset when the down-counter reaches 0. The Current Count register is a 16-bit register, accessible as two 8-bit registers, which mirrors the contents of the down-counter. This register can be read anytime. However, reading the register is asynchronous to the counter's counting, and the value returned can be guaranteed as valid only if the counter is stopped. The down-counter can be read reliably while it is counting by first writing a 1 to the Read Counter Control (RCC) bit in the counter/timer's Command and Status register. This freezes the value in the Current Count register until a read of the least-significant byte is performed. A read of RCC indicates if the CCR is holding a value, or if it is following the down-counter.

4.2.4 Ending Condition

The Continuous/$\overline{\text{Single Cycle}}$ (C/$\overline{\text{SC}}$) bit in the Mode Specification register controls operation of the down-counter when it reaches terminal count (the count following the count of 1). If C/$\overline{\text{SC}}$ is 0

reading the vector register returns the unmodified base vector so that it can be verified.

Another register, the Current Vector register, facilitates the use of the CIO in a polled environment. When read, the data returned is the same as the interrupt vector that is output in an Interrupt Acknowledge, based on the highest-priority IP set. If no unmasked IPs are set, the value FF_H is returned. The Current Vector register provides a simple way to poll all IPs in a single read.

The No Vector (NV) control bit of the Master Interrupt Control register, when set to 1, inhibits the outputting of an interrupt vector during an $\overline{INTACK}$ cycle. The NV bit does not affect the setting of the IUS operation. The only thing that the NV does is prevent the vector from being output on the bus.

5.4 Z-BUS INTERRUPT OPERATION

Figure 7-5 displays Interrupt Acknowledge timing. The Z8036 generates an interrupt request by lowering the $\overline{INT}$ line only if:

- Such interrupt requests are enabled (IE is 1, MEI is 1).
- It has an interrupt pending (IP = 1).
- It does not have an interrupt under service (IUS is 0).
- No higher-priority interrupt is being serviced (IEI is 1).

Figure 5-2 shows a typical Z-BUS interrupt arbitration setting.

IEO is not pulled down by the Z8036 at this time; IEO continues to follow IEI until an Interrupt Acknowledge transaction occurs.

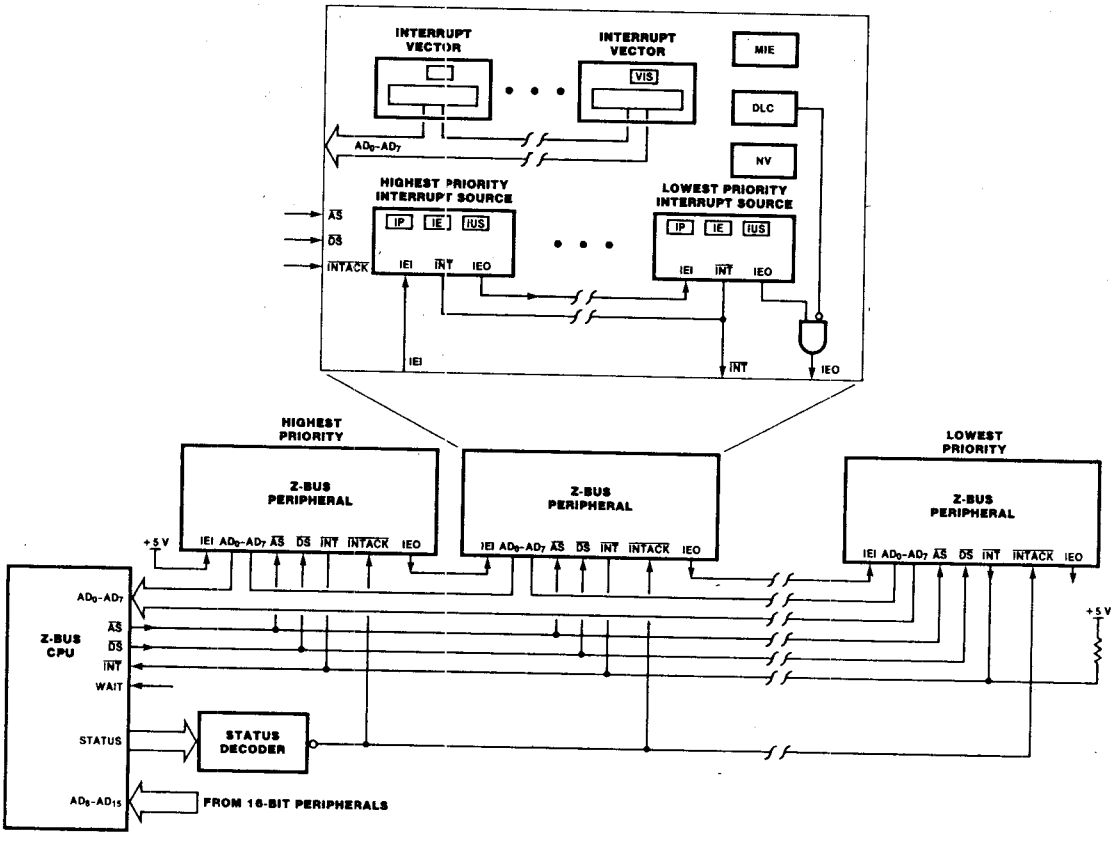


Figure 5-2. Z-BUS Interrupt Arbitration

cleared to 0, the corresponding logic sections are in an initialization mode. All of the registers can be read and written, but the normal operation of the sections is inhibited. The Port A and Port B Enables, when cleared to 0, force their respective I/O lines into a high-impedance state, hold the 1's catchers in a reset condition, inhibit REQUEST/$\overline{\text{WAIT}}$ generation, and prevent the setting of their Interrupt Pending (IP) bits (the states of IP and Interrupt Under Service (IUS) are not affected). Additionally, output data can be written (the first data output is valid when the output drivers go active), but the data direction for these bits must be properly specified before the data is written. The Port C Enable operates in the same way, and, until set to 1, the handshake logic for Ports A and B is forced into an idle state. The Counter/Timer Enables, when set to 0, terminate any countdown sequence in progress, inhibit the counter/timer from being triggered, and force the counter output to 0. While the enable is 0, the Read Counter Control (RCC) bit in the Counter/Timer Command and Status register is forced to 0. Independent enable bits are provided for the different sections of the device so that the individual sections can be reconfigured without disturbing the status of the unchanged sections. By using these enable bits, the device can be initialized in any sequence as long as the desired configuration for a section is specified before its enable bit is set to 1. When ports or counter/timers are to be linked, the bits which specify linking must be programmed before the functions are enabled. In this case two writes are required to the Master Configuration Control register.

6.5 PROGRAMMING

Programming the CIO entails loading control registers with bits to implement the desired operation. As discussed above, individual enable bits are provided for the various major blocks so that erroneous operations do not occur while the port is being initialized. Before the ports are enabled: IPs cannot be set, REQUEST and $\overline{\text{WAIT}}$ cannot be asserted, and all outputs remain high-impedance; the handshake lines are ignored until Port C is enabled; and the counter/timers cannot be triggered until their enable bits are set.

6.5.1 Programming the Z8036

Programming the Z8036 is simple, because every register is directly addressable--a key advantage of the multiplex Address/Data bus.

The Z8036 allows two schemes for register addressing. Both schemes use only six of the eight bits of the Address/Data bus. The scheme used is determined by the Right Justify Address (RJA) bit in the Master Interrupt Control register. When RJA equals 0, Address bus bits 0 and 7 are ignored, and bits 1 through 6 are decoded for the register address (A_0 is derived from AD_1). When RJA equals 1, bits 0 through 5 are decoded for the register address (A_0 is derived from AD_0).

6.5.2 Programming the Z8536

The Data Registers of Ports A, B, and C are directly addressed by pins A_0 and A_1, as shown in Table 6-1.

Table 6-1. Z8536 Data Register Addressing

A_1	A_0	Register
0	0	Port C Data Register
0	1	Port B Data Register
1	0	Port A Data Register
1	1	Control Registers

All other internal registers are accessed by the following two-step sequence (with pins $A_0 = A_1 = 1$). First write the address of the target register to an internal 6-bit Pointer register, then read from or write to the target register. The Data registers can also be accessed by this method.

In the Z8536, an internal state machine determines if access (with pins $A_0 = A_1 = 1$) is to the Pointer register or to an internal control register (See Figure 6-1). Following any control read operation the state machine is in State 0, and the

Chapter 7
Z8036 (Z-CIO) Interfacing

7.1 INTRODUCTION

This section provides information on pin functions and assignments and functional timing diagrams for the Z8036 Z-CIO.

7.2 FEATURES

The following features of the Z8036 are not obvious without reference to the ac timing diagrams in the Z8036 Product Specification, document #00-2014-A0.

- The Address Strobe ($\overline{AS}$) input functions as the clock of the Z8036. If the $\overline{AS}$ stops, then data does not get clocked in or through the device, IPs are not set, etc. Care should be taken in the design of the system to ensure that $\overline{AS}$ to the Z8036 is not blocked.
- The assertion of REQUEST is synchronous with PCLK.
- The release of $\overline{WAIT}$ is sychronous with PCLK.
- PCLK is only used with the counter/timers (in timer mode), the deskew timers, and the REQUEST/$\overline{WAIT}$ logic. If these functions are not used, the PCLK input can be held Low.

7.3 PIN FUNCTIONS AND ASSIGNMENTS

The Z8036 is configured for Z-BUS interface controls and timing. The pin functions and assignments are shown in Figures 7-1 and 7-2. Section 7.4 is a description of the pin functions for the Z8036.

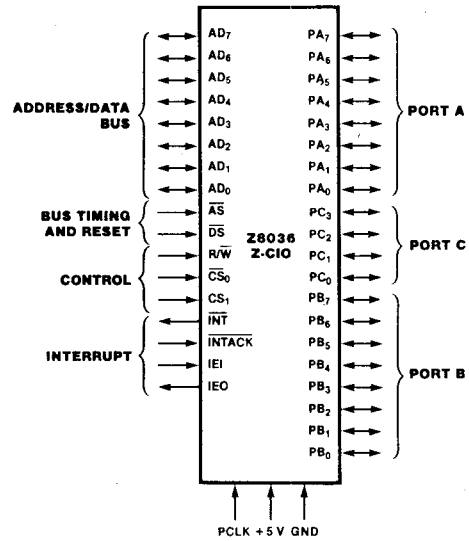


Figure 7-1. Z8036 (Z-CIO) Pin Functions

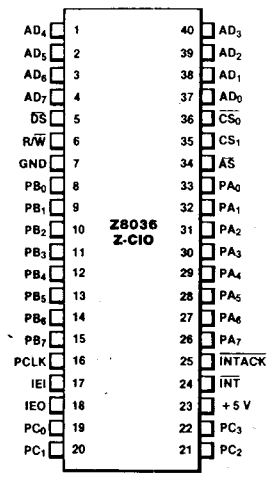


Figure 7-2. Z8036 (Z-CIO) Pin Assignments

7.4 PIN DESCRIPTIONS

AD_0-AD_7. Z-BUS Address/Data lines (bidirectional/3-state). These multiplexed Address/Data

lines are used for transfers between the CPU and Z-CIO.

$\overline{AS}$*. Address Strobe (input, active Low). Addresses, $\overline{INTACK}$, and $\overline{CS_0}$ are sampled while $\overline{AS}$ is Low.

$\overline{CS_0}$ and CS_1. Chip Select 0 (input, active Low) and Chip Select 1 (input, active High). $\overline{CS_0}$ and CS_1 must be Low and High, respectively, in order to select a device. $\overline{CS_0}$ is latched by $\overline{AS}$.

$\overline{DS}$. Data Strobe (input, active Low). $\overline{DS}$ provides timing for the transfer of data into or out of the Z8036.

IEI. Interrupt Enable In (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher-priority device has an interrupt under service or is requesting an interrupt.

IEO. Interrupt Enable Out (output, active High). IEO is High only if IEI is High and either:

(1) the CPU is not servicing an interrupt from the CIO, or

(2) during an Interrupt Acknowledge Cycle, the CIO is not requesting an interrupt.

IEO is connected to the next lower-priority device's IEI input and thus inhibits interrupts from lower-priority devices.

$\overline{INT}$. Interrupt Request (output, open-drain, active Low). This signal is pulled Low when the Z8036 requests an interrupt.

$\overline{INTACK}$. Interrupt Acknowledge (input, active Low). This signal indicates to the Z8036 that an Interrupt Acknowledge cycle is in progress. $\overline{INTACK}$ is sampled while $\overline{AS}$ is Low.

PA_0-PA_7. Port A I/O lines (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the Z8036's Port A and external devices.

PB_0-PB_7. Port B I/O lines (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the Z8036's Port B and external devices. They may also be used to provide external access to Counter/Timers 1 and 2.

PC_0-PC_3. Port C I/O lines (bidirectional, 3-state, or open-drain). These four I/O lines are used to provide handshake, $\overline{WAIT}$, and REQUEST lines for Ports A and B; to provide external access to Counter/Timer 3; or to access Port C of the Z8036.

PCLK. (input, TTL-compatible). This is a peripheral clock that may be, but is not necessarily, the CPU clock. It is used with timers and REQUEST/$\overline{WAIT}$ logic.

R/$\overline{W}$. Read/Write (input). R/$\overline{W}$ indicates that the CPU is reading from (High) or writing to (Low) the Z8036.

* When AS and DS are detected Low at the same time (normally an illegal condition), the Z-CIO is reset.

7.5 Z8036 (Z-CIO) READ CYCLE TIMING

The CPU places an address on the Address/Data bus. The most-significant bits and status information are combined and decoded by external logic to provide two Chip Selects ($\overline{CS_0}$ and CS_1). Six bits of the least-significant byte of the address are latched within the Z8036 and used to specify a Z8036 register. The data from the register specified is strobed onto the Address/Data bus when the CPU issues a $\overline{DS}$. If the register indicated by the address does not exist, the Z8036 remains high-impedance.

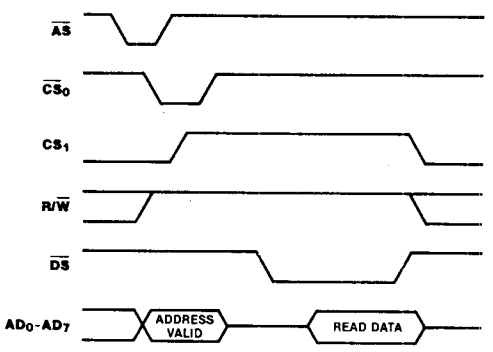


Figure 7-3. Z8036 (Z-CIO) Read Cycle Timing

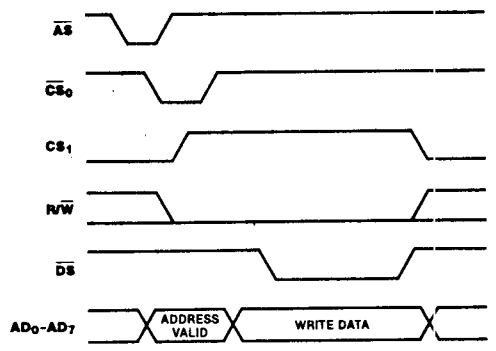


Figure 7-4. Z8036 (Z-CIO) Write Cycle Timing

7.6 Z8036 (Z-CIO) WRITE CYCLE TIMING

The CPU places an address on the Address/Data bus. The most-significant bits and status information are combined and decoded by external logic to provide two Chip Selects ($\overline{CS}_0$ and CS_1). Six bits of the least-significant byte of the address are latched within the Z8036 and used to specify a Z8036 register. The CPU places the data on the Address/Data bus and strobes it into the Z8036 register by issuing a $\overline{DS}$.

7.7 Z8036 (Z-CIO) INTERRUPT ACKNOWLEDGE TIMING

When one of the IP bits in the Z8036 goes High and interrupts are enabled, the Z8036 pulls its $\overline{INT}$ output line Low, requesting an interrupt. The CPU responds with an Interrupt Acknowledge cycle. When $\overline{INTACK}$ goes Low with IP set, the Z8036 pulls its IEO Low, disabling all lower-priority devices on the daisy-chain. The CPU reads the Z8036 interrupt vector by issuing a Low $\overline{DS}$, thereby strobing the interrupt vector onto the Address/Data bus. The IUS that corresponds to the IP is also set, which causes IEO to remain Low.

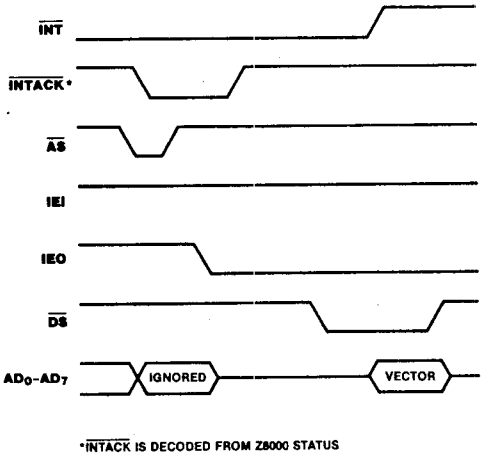


Figure 7-5. Z8036 (Z-CIO) Interrupt Acknowledge Timing

8.4 PIN DESCRIPTIONS

A_0-A_1. Address Lines (input). These two lines are used to select the register involved in the CPU transaction: Port A's Data register, Port B's Data register, Port C's Data register, or a control register.

$\overline{CE}$. Chip Enable (input, active Low). A Low level on this input enables the Z8536 to be read from or written to.

D_0-D_7. Data Bus (bidirectional, 3-state). These eight data lines are used for transfers between the CPU and the CIO.

IEI. Interrupt Enable In (input, active High). IEI is used with IEO to form an interrupt daisy-chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher-priority device has an interrupt under service or is requesting an interrupt.

IEO. Interrupt Enable Out (output, active High). IEO is High only if IEI is High and either:

(1) the CPU is not serving an interrupt from the CIO, or

(2) during an Interrupt Acknowledge cycle, the CIO is not requesting an interrupt.

IEO is connected to the next lower-priority device's IEI input and thus inhibits interrupts from lower-priority devices.

$\overline{INT}$. Interrupt Request (output, open-drain, active Low). This signal is pulled Low when the Z8536 requests an interrupt.

$\overline{INTACK}$. Interrupt Acknowledge (input, active Low). This input indicates to the Z8536 that an Interrupt Acknowledge cycle is in progress. $\overline{INTACK}$ must be synchronized to PCLK, and it must be stable throughout the Interrupt Acknowledge cycle.

PA_0-PA_7. Port A I/O lines (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the CIO's Port A and external devices.

PB_0-PB_7. Port B I/O lines (bidirectional, 3-state, or open-drain). These eight I/O lines transfer information between the Z8536's Port B and external devices. They may also be used to provide external access to Counter/Timers 1 and 2.

PC_0-PC_3. Port C I/O lines (bidirectional, 3-state, or open-drain). These four I/O lines are used to provide handshake, $\overline{WAIT}$, and REQUEST lines for Ports A and B; external access to Counter/Timer 3; or access to the Z8536's Port C.

PCLK. Peripheral Clock (input, TTL-compatible). This is the clock used by the internal control logic and the counter/timers in timer mode. (It does not have to be the CPU clock.)

$\overline{RD}$*. Read (input, active Low). This signal indicates that a CPU is reading from the CIO. During an Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the Data bus if the Z8536 is the highest-priority device requesting an interrupt.

$\overline{WR}$*. Write (input, active Low). This signal indicates a CPU write to the Z8536.

* When $\overline{RD}$ and $\overline{WR}$ are detected Low at the same time (normally an illegal condition), the Z8536 is reset.

8.5 Z8536 (CIO) READ CYCLE TIMING

At the beginning of a read cycle, the CPU places an address on the Address bus. Bits A_0 and A_1 specify a Z8536 register; the remaining address bits and status information are combined and decoded to generate a Chip Enable ($\overline{CE}$) signal that selects the Z8536. When Read ($\overline{RD}$) goes Low, data from the specified register is gated onto the Data bus.

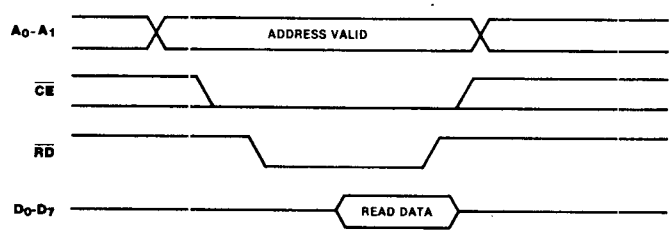


Figure 8-3. Z8536 (CIO) Read Cycle Timing

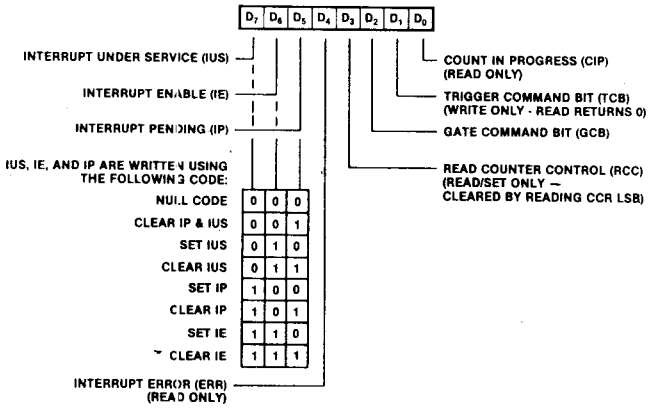
Appendix A

CIO MNEMONICS

$\overline{\text{ACKIN}}$	Acknowledge Input
$\overline{\text{AS}}$	Address Strobe
C/$\overline{\text{SC}}$	Continuous/$\overline{\text{Single Cycle}}$
CIO	Counter/Timer, Parallel Input/Output Unit
CIP	Count In Progress
CInE	Counter/Timer n Enable
CT3E and PCE	Counter/Timer 3 and Port C Enable
CT VIS	Counter/Timer Vector Includes Status
DAC	Data Accepted
$\overline{\text{DAV}}$	Data Available
DCS	Duty Cycle Selects
DD	Data Direction register
DLC	Disable Lower Chain
DMA	Direct Memory Access
DPP	Data Path Polarity register
$\overline{\text{DS}}$	Data Strobe
DTE	Deskew Timer Enable
DTE/LPM	Deskew Timer Enable/Latch on Pattern Match
ECE	External Count Enable
EGE	External Gate Enable
EOE	External Output Enable
ERR	Interrupt Error
ETE	External Trigger Enable
GCB	Gate Command Bit
HTS	Handshake Type Specification bits
IE	Interrupt Enable
IEI	Interrupt Enable In
IEO	Interrupt Enable Out
IMO	Interrupt on Match Only
$\overline{\text{INT}}$	Interrupt
$\overline{\text{INTACK}}$	Interrupt Acknowledge
I/O	Input/Output
IP	Interrupt Pending
IRF	Input Register Full
ITB	Interrupt on Two Bytes
IUS	Interrupt Under Service
LC	Counter/Timer Link Controls
LPM	Latch on Pattern Match
LSB	least-significant bit
MIE	Master Interrupt Enable
MSB	most-significant bit
NV	No Vector
OR-PEV	OR-Priority Encoded Vector
ORE	Output Register Empty
PA	Port A
PA VIS	Port A Vector Includes Status
PAE	Port A Enable
PB	Port B
PB VIS	Port B Vector Includes Status
PBE	Port B Enable
PC	Port C
PCE	Port C Enable
PCLK	Peripheral Clock
PLK	Port Link Control
PM	Pattern Mask registers
PMF	Pattern Match Flag
PMS	Pattern Mode Specification bits
PP	Pattern Polarity registers
PT	Pattern Transition registers
PTS	Port Type Selects
RCC	Read Counter Control
REB	Retrigger Enable Bit
RFD	Ready For Data
RJA	Right Justified Address
R/$\overline{\text{W}}$	Read/Write
RWS	REQUEST/$\overline{\text{WAIT}}$ Specification bits
SB	Single-Buffered
SIO	Special Input/Output
TCB	Trigger Command Bit
VIS	Vector Includes Status
1's Catcher	One's Catcher
3-Wire	3-Wire Handshake (IEEE-488)

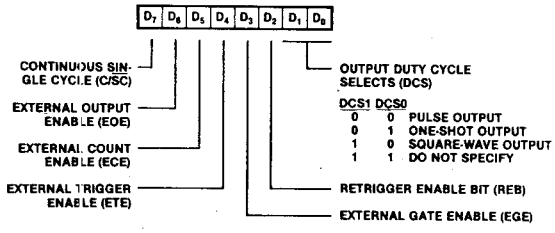
Counter/Timer Command and Status Registers

Addresses: 001010 Counter/Timer 1
001011 Counter/Timer 2
001100 Counter/Timer 3
(Read/Partial Write)



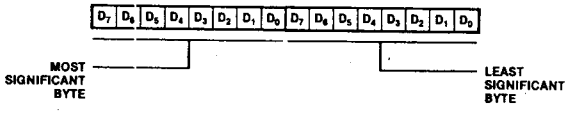
Counter/Timer Mode Specification Registers

Addresses: 011100 Counter/Timer 1
011101 Counter/Timer 2
011110 Counter/Timer 3
(Read/Write)



Counter/Timer Current Count Registers

Addresses: 010000 Counter/Timer 1's MSB
010001 Counter/Timer 1's LSB
010010 Counter/Timer 2's MSB
010011 Counter/Timer 2's LSB
010100 Counter/Timer 3's MSB
010101 Counter/Timer 3's LSB
(Read Only)



Counter/Timer Time Constant Registers

Addresses: 010110 Counter/Timer 1's MSB
010111 Counter/Timer 1's LSB
011000 Counter/Timer 2's MSB
011001 Counter/Timer 2's LSB
011010 Counter/Timer 3's MSB
011011 Counter/Timer 3's LSB
(Read/Write)

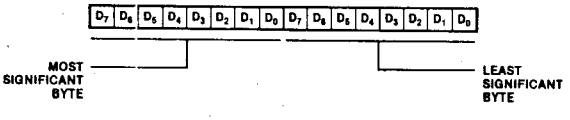


Figure B-6. Counter/Timer Registers

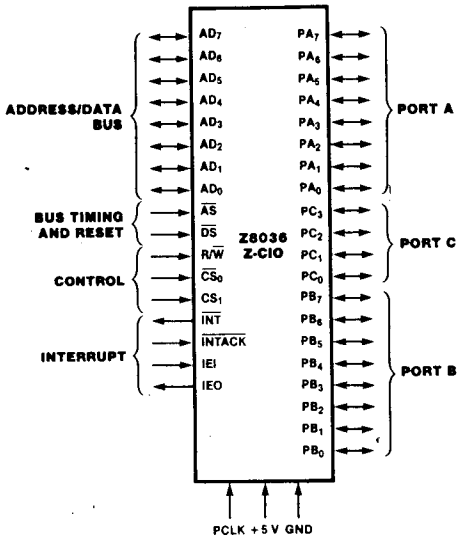


Figure 1. Pin Functions

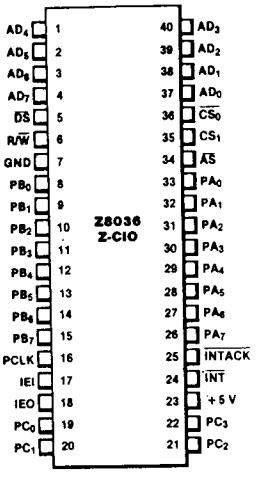


Figure 2. Pin Assignments

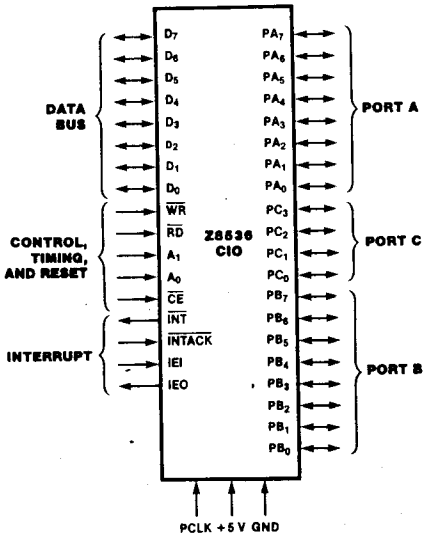


Figure 1. Pin Functions

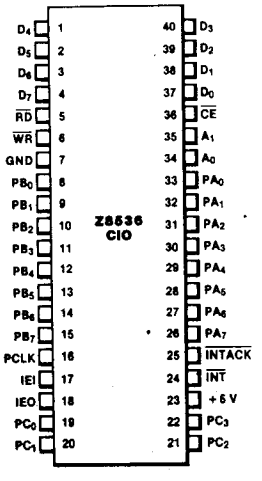


Figure 2. Pin Assignments