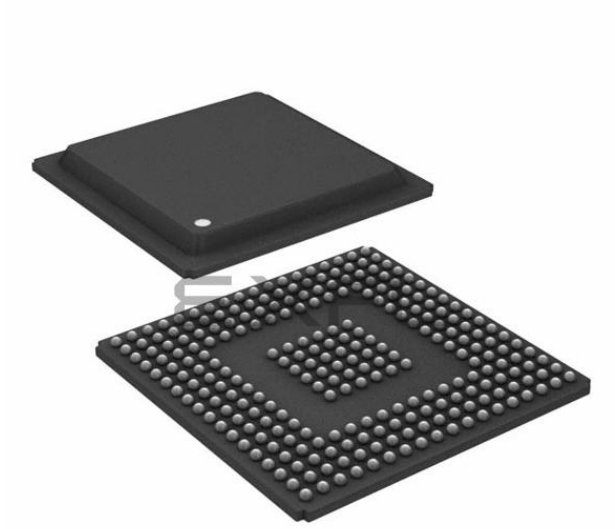

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	PCI, SPI, SSP, UART, USB
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	308kB
Voltage - I/O	3.30V
Voltage - Core	1.50V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	260-BBGA
Supplier Device Package	260-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf535pbb-300

- EE-210: SDRAM Selection and Configuration Guidelines for ADI Processors
- EE-213: Host Communication via the Asynchronous Memory Interface for Blackfin® Processors
- EE-214: Ethernet Network Interface for ADSP-BF535 Blackfin® Processors
- EE-235: An Introduction to Scripting in VisualDSP++®
- EE-242: PWM and Class-D Amplifiers with ADSP-BF535 Blackfin® Processors
- EE-261: Understanding Jitter Requirements of PLL-Based Processors
- EE-269: A Beginner's Guide to Ethernet 802.3
- EE-273: Using the VisualDSP++ Command-Line Installer
- EE-281: Hardware Design Checklist for the Blackfin® Processors
- EE-302: Interfacing ADSP-BF53x Blackfin® Processors to NAND FLASH Memory
- EE-303: Using VisualDSP++® Thread-Safe Libraries with a Third-Party RTOS
- EE-304: Using the Blackfin® Processor SPORT to Emulate a SPI Interface
- EE-306: PGO Linker - A Code Layout Tool for Blackfin Processors
- EE-307: Blackfin® Processor Troubleshooting Tips Using VisualDSP++® Tools
- EE-312: Building Complex VDK/LwIP Applications Using Blackfin® Processors
- EE-323: Implementing Dynamically Loaded Software Modules
- EE-324: System Optimization Techniques for Blackfin® Processors
- EE-325: Interfacing Atmel Fingerprint Sensor AT77C104B with Blackfin® Processors
- EE-326: Blackfin® Processor and SDRAM Technology
- EE-330: Windows Vista Compatibility in VisualDSP++ 5.0 Development Tools
- EE-332: Cycle Counting and Profiling
- EE-333: Interfacing Blackfin® Processors to Winbond W25X16 SPI Flash Devices
- EE-334: Using Blackfin® Processor Hibernate State for Low Standby Power
- EE-336: Putting ADSP-BF54x Blackfin® Processor Booting into Practice
- EE-339: Using External Switching Regulators with Blackfin® Processors
- EE-340: Connecting SHARC® and Blackfin® Processors over SPI
- EE-347: Formatted Print to a UART Terminal with Blackfin® Processors
- EE-350: Seamlessly Interfacing MEMS Microphones with Blackfin Processors
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users
- EE-68: Analog Devices JTAG Emulation Technical Reference

Data Sheet

- ADSP-BF535: Embedded Processor Data Sheet

Emulator Manuals

- HPUSB, USB, and HPPCI Emulator User's Guide
- ICE-1000/ICE-2000 Emulator User's Guide
- ICE-100B Emulator User's Guide

Evaluation Kit Manuals

- Blackfin® USB-LAN EZ-Extender® Manual
- Blackfin®/SHARC® USB EZ-Extender® Manual

Integrated Circuit Anomalies

- ADSP-BF535 Anomaly List for Revision(s) 0.2, 1.0, 1.1, 1.2, 1.3

Processor Manuals

- ADSP-BF535 Blackfin ® Processor Hardware Reference
- ADSP-BF5xx/ADSP-BF60x Blackfin® Processor Programming Reference
- Blackfin Processors: Manuals

Software Manuals

- CrossCore® Embedded Studio 2.5.0 Assembler and Preprocessor Manual
- CrossCore® Embedded Studio 2.5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- CrossCore® Embedded Studio 2.5.0 Linker and Utilities Manual
- CrossCore® Embedded Studio 2.5.0 Loader and Utilities Manual
- CrossCore® Software Licensing Guide
- lwIP for CrossCore® Embedded Studio 1.0.0 User's Guide
- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- VisualDSP++® 5.0 Device Drivers and System Services Manual for Blackfin Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual

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GENERAL DESCRIPTION

The ADSP-BF535 processor is a member of the Blackfin processor family of products, incorporating the Micro Signal Architecture (MSA), jointly developed by Analog Devices, Inc. and Intel Corporation. The architecture combines a dual MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and Single-Instruction, Multiple Data (SIMD) multimedia capabilities into a single instruction set architecture.

By integrating a rich set of industry leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading edge signal processing in one integrated package.

Portable Low Power Architecture

Blackfin processors provide world class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management, the ability to independently vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, by comparison to just varying the frequency of operation. This translates into longer battery life for portable appliances.

System Integration

The ADSP-BF535 Blackfin processor is a highly integrated system-on-a-chip solution for the next generation of digital communication and portable Internet appliances. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The ADSP-BF535 Blackfin processor system peripherals include UARTs, SPIs, SPORTs, general-purpose Timers, a Real-Time

Clock, Programmable Flags, Watchdog Timer, and USB and PCI buses for glueless peripheral expansion.

ADSP-BF535 Peripherals

The ADSP-BF535 Blackfin processor contains a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance. See Functional Block Diagram on Page 1. The base peripherals include general-purpose functions such as UARTs, timers with PWM (Pulse Width Modulation) and pulse measurement capability, general-purpose flag I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the ADSP-BF535 Blackfin processor contains high speed serial ports for interfaces to a variety of audio and modem CODEC functions. It also contains an event handler for flexible management of interrupts from the on-chip peripherals and external sources. And it contains power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The on-chip peripherals can be easily augmented in many system designs with little or no glue logic due to the inclusion of several interfaces providing expansion on industry-standard buses. These include a 32-bit, 33 MHz, V2.2 compliant PCI bus, SPI serial expansion ports, and a device type USB port. These enable the connection of a large variety of peripheral devices to tailor the system design to specific applications with a minimum of design complexity.

All of the peripherals, except for programmable flags, real-time clock, and timers, are supported by a flexible DMA structure with individual DMA channels integrated into the peripherals. There is also a separate memory DMA channel dedicated to data transfers between the various memory spaces including external SDRAM and asynchronous memory, internal Level 1 and Level 2 SRAM, and PCI memory spaces. Multiple on-chip 32-bit buses, running at up to 133 MHz, provide adequate bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

Processor Core

As shown in Figure 1, the Blackfin processor core contains two multiplier/accumulators (MACs), two 40-bit ALUs, four video ALUs, and a single shifter. The computational units process 8-bit, 16-bit, or 32-bit data from the register file.

Each MAC performs a 16-bit by 16-bit multiply in every cycle, with an accumulation to a 40-bit result, providing 8 bits of extended precision.

The ALUs perform a standard set of arithmetic and logical operations. With two ALUs capable of operating on 16- or 32-bit data, the flexibility of the computation units covers the signal processing requirements of a varied set of application needs. Each of the two 32-bit input registers can be regarded as two 16-bit halves, so each ALU can accomplish very flexible single 16-bit arithmetic operations. By viewing the registers as pairs of 16-bit operands, dual 16-bit or single 32-bit operations can be accomplished in a single cycle. Quad 16-bit operations can be accomplished simply, by taking advantage of the second ALU. This accelerates the per cycle throughput.

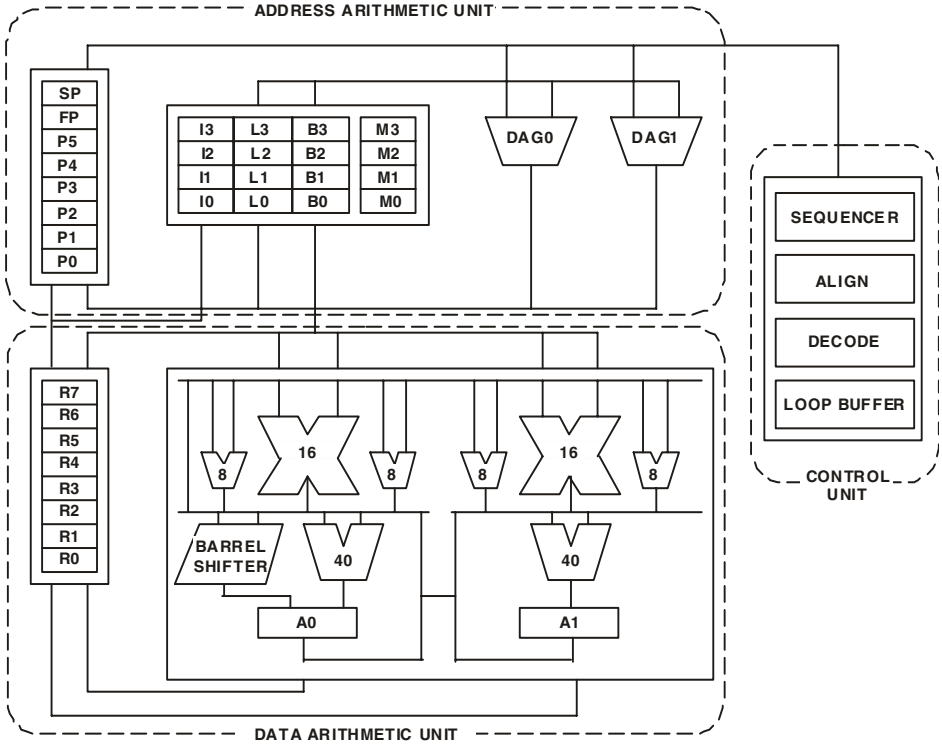


Figure 1. Processor Core

The powerful 40-bit shifter has extensive capabilities for performing shifting, rotating, normalization, extraction, and for depositing data.

The data for the computational units is found in a multiported register file of sixteen 16-bit entries or eight 32-bit entries.

A powerful program sequencer controls the flow of instruction execution, including instruction alignment and decoding. The sequencer supports conditional jumps and subroutine calls, as well as zero-overhead looping. A loop buffer stores instructions locally, eliminating instruction memory accesses for tightly looped code.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from memory. The DAGs share a register file containing four sets of 32-bit Index, Modify, Length, and Base registers. Eight additional 32-bit registers provide pointers for general indexing of variables and stack locations.

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. Level 2 (L2) memories are other memories, on-chip or off-chip, that may take multiple processor cycles to access. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratch pad data memory stores stack and local variable information. At the L2 level, there is a single unified memory space, holding both instructions and data.

In addition, the L1 instruction memory and L1 data memories may be configured as either Static RAMs (SRAMs) or caches. The Memory Management Unit (MMU) provides memory protection for individual tasks that may be operating on the core and may protect system registers from unintended access.

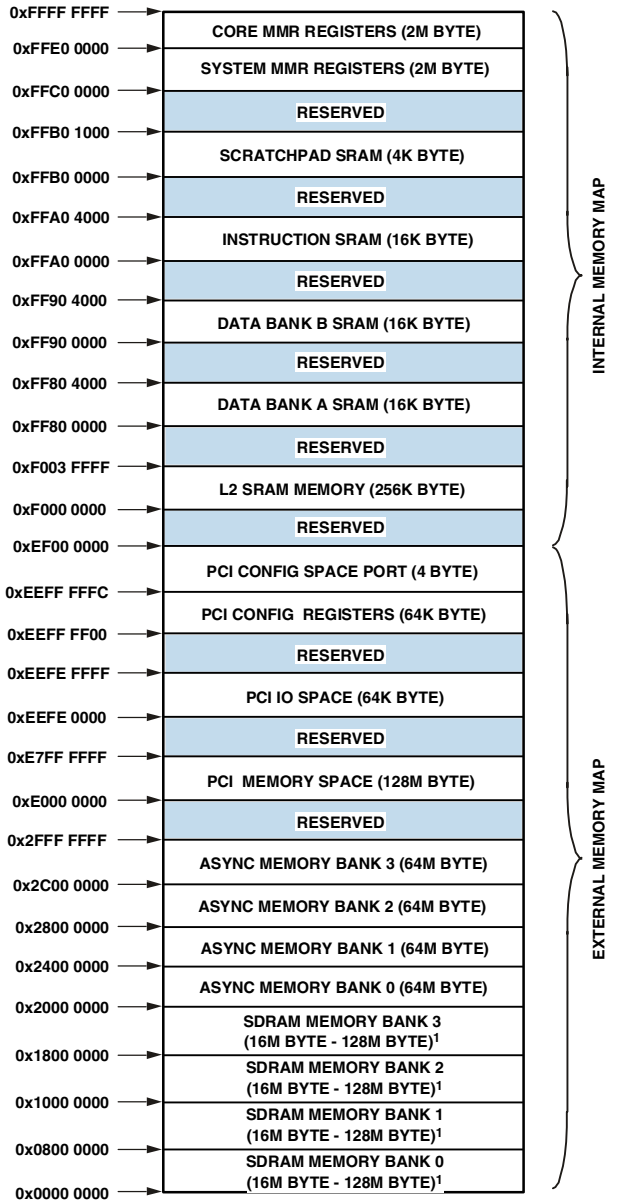
The architecture provides three modes of operation: user mode, supervisor mode, and Emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit op-codes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit op-codes, representing fully featured multifunction instructions. Blackfin processors support a limited multiple issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

Memory Architecture

The ADSP-BF535 Blackfin processor views memory as a single unified 4 Gbyte address space, using 32-bit addresses. All resources, including internal memory, external memory, PCI address spaces, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance with very fast, low latency memory as cache or SRAM very close to the processor; and larger, lower cost, and lower performance memory systems farther away from the processor. See Figure 2.



1 THE ADDRESSES SHOWN FOR THE SDRAM BANKS REFLECT A FULLY POPULATED SDRAM ARRAY WITH 512M BYTES OF MEMORY. IF ANY BANK CONTAINS LESS THAN 128M BYTES OF MEMORY, THAT BANK WOULD EXTEND ONLY TO THE LENGTH OF THE REAL MEMORY SYSTEMS, AND THE END ADDRESS WOULD BECOME THE START ADDRESS OF THE NEXT BANK. THIS WOULD CONTINUE FOR ALL FOUR BANKS, WITH ANY REMAINING SPACE BETWEEN THE END OF MEMORY BANK 3 AND THE BEGINNING OF ASYNC MEMORY BANK 0, AT ADDRESS 0x2000 0000, TREATED AS RESERVED ADDRESS SPACE.

Figure 2. Internal/External Memory Map

The L1 memory system is the primary highest performance memory available to the Blackfin processor core. The L2 memory provides additional capacity with slightly lower performance. Lastly, the off-chip memory system, accessed through the External Bus Interface Unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing more than 768M bytes of external physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal L1/L2 memories and the external memory spaces (including PCI memory space).

Internal (On-Chip) Memory

The ADSP-BF535 Blackfin processor has four blocks of on-chip memory providing high bandwidth access to the core.

The first is the L1 instruction memory consisting of 16K bytes of 4-Way set-associative cache memory. In addition, the memory may be configured as an SRAM. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of two banks of 16K bytes each. Each L1 data memory bank can be configured as one Way of a 2-Way set-associative cache or as an SRAM, and is accessed at full speed by the core.

The third memory block is a 4K byte scratch pad RAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM (it cannot be configured as cache memory and is not accessible via DMA).

The fourth on-chip memory system is the L2 SRAM memory array which provides 256K bytes of high speed SRAM at the full bandwidth of the core, and slightly longer latency than the L1 memory banks. The L2 memory is a unified instruction and data memory and can hold any mixture of code and data required by the system design.

The Blackfin processor core has a dedicated low latency 64-bit wide datapath port into the L2 SRAM memory.

External (Off-Chip) Memory

External memory is accessed via the External Bus Interface Unit (EBIU). This interface provides a glueless connection to up to four banks of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory-mapped I/O devices.

The PC133 compliant SDRAM controller can be programmed to interface to up to four banks of SDRAM, with each bank containing between 16M bytes and 128M bytes providing access to up to 512M bytes of SDRAM. Each bank is independently programmable and is contiguous with adjacent banks regardless of the sizes of the different banks or their placement. This allows flexible configuration and upgradability of system memory while allowing the core to view all SDRAM as a single, contiguous, physical address space.

The asynchronous memory controller can also be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 64 Mbyte segment regardless of the size of the devices used so that these banks will only be contiguous if fully populated with 64M bytes of memory.

PCI

The PCI bus defines three separate address spaces, which are accessed through windows in the ADSP-BF535 Blackfin processor memory space. These spaces are PCI memory, PCI I/O, and PCI configuration.

In addition, the PCI interface can either be used as a bridge from the processor core as the controlling CPU in the system, or as a host port where another CPU in the system is the host and the ADSP-BF535 is functioning as an intelligent I/O device on the PCI bus.

When the ADSP-BF535 Blackfin processor acts as the system controller, it views the PCI address spaces through its mapped windows and can initialize all devices in the system and maintain a map of the topology of the environment.

The PCI memory region is a 4 Gbyte space that appears on the PCI bus and can be used to map memory I/O devices on the bus. The ADSP-BF535 Blackfin processor uses a 128 Mbyte window in memory space to see a portion of the PCI memory space. A base address register is provided to position this window anywhere in the 4 Gbyte PCI memory space while its position with respect to the processor addresses remains fixed.

The PCI I/O region is also a 4 Gbyte space. However, most systems and I/O devices only use a 64 Kbyte subset of this space for I/O mapped addresses. The ADSP-BF535 Blackfin processor implements a 64K byte window into this space along with a base address register which can be used to position it anywhere in the PCI I/O address space, while the window remains at the same address in the processor's address space.

PCI configuration space is a limited address space, which is used for system enumeration and initialization. This address space is a very low performance communication mode between the processor and PCI devices. The ADSP-BF535 Blackfin processor provides a one-value window to access a single data value at any address in PCI configuration space. This window is fixed and receives the address of the value, and the value if the operation is a write. Otherwise, the device returns the value into the same address on a read operation.

I/O Memory Space

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4 Gbyte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The core MMRs are accessible only by the core and only in supervisor mode and appear as reserved space by on-chip peripherals, as well as external devices accessing resources through the PCI bus. The system MMRs are accessible by the core in supervisor mode and can be mapped as either visible or reserved to other devices, depending on the system protection model desired.

DMA controller and interrupt input to minimize processor polling overhead and to enable asynchronous requests for CPU attention only when transfer management is required.

The USB device requires an external 48 MHz oscillator. The value of SCLK must always exceed 48 MHz for proper USB operation.

Real-Time Clock

The ADSP-BF535 Blackfin processor Real-Time Clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF535 Blackfin processor. The RTC peripheral has dedicated power supply pins, so that it can remain powered up and clocked, even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

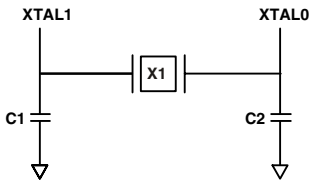
The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 6-bit second counter, a 6-bit minute counter, a 5-bit hours counter, and an 8-bit day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: one is for a time of day, the second is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one minute resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the ADSP-BF535 Blackfin processor from a low power state upon generation of any interrupt.

Connect RTC pins XTALI and XTALO with external components, as shown in Figure 3.



SUGGESTED COMPONENTS:
ECLIPTEK EC38J (THROUGH-HOLE PACKAGE)
EPSON MC405 12pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22pF
C2 = 22pF

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3pF.

Figure 3. External Components for RTC

Watchdog Timer

The ADSP-BF535 Blackfin processor includes a 32-bit timer, which can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, non-maskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running because of external noise conditions or a software error.

After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the timer control register, which is set only upon a watchdog generated reset.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

Timers

There are four programmable timer units in the ADSP-BF535 Blackfin processor. Three general-purpose timers have an external pin that can be configured either as a Pulse-Width Modulator (PWM) or timer output, as an input to clock the timer, or for measuring pulse widths of external events. Each of the three general-purpose timer units can be independently programmed as a PWM, internally or externally clocked timer, or pulse width counter.

The general-purpose timer units can be used in conjunction with the UARTs to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel.

The general-purpose timers can generate interrupts to the processor core providing periodic events for synchronization, either to the processor clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock (CCLK) and is typically used as a system tick clock for the generation of operating system periodic interrupts.

Serial Ports (Sports)

The ADSP-BF535 Blackfin processor incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support these features:

- Bidirectional operation—Each SPORT has independent transmit and receive pins.
- Buffered (8-deep) transmit and receive ports—Each port has a data register for transferring data-words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking—Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131070) Hz to (f_{SCLK}/2) Hz.
- Word length—Each SPORT supports serial data-words from 3 to 16 bits in length transferred in a format of most significant bit first or least significant bit first.

(BYPASS) in the PLL Control register (PLL_CTL). If bypass is disabled, the processor transitions to the full on mode. If bypass is enabled, the processor transitions to the Active mode.

When in Sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode – Maximum Power Savings

The deep sleep mode maximizes power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but will not be able to access internal resources or external memory. This powered down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, assertion of $\overline{\text{RESET}}$ causes the processor to sense the value of the BYPASS pin. If bypass is disabled, the processor will transition to full on mode. If bypass is enabled, the processor will transition to active mode. When in deep sleep mode, assertion of the RTC asynchronous interrupt causes the processor to transition to the full on mode, regardless of the value of the BYPASS pin.

The DEEPSLEEP output is asserted in this mode.

Mode Transitions

The available mode transitions diagrammed in Figure 6 are accomplished either by the interrupt events described in the following sections or by programming the PLLCTL register with the appropriate values and then executing the PLL programming sequence.

This instruction sequence takes the processor to a known idle state with the interrupts disabled. Note that all DMA activity should be disabled during mode transitions.

Table 3. Operating Mode Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)
Full On	Enabled	No	Enabled	Enabled
Active	Enabled	Yes	Enabled	Enabled
Sleep	Enabled	Yes or No	Disabled	Enabled
Deep +	Disabled		Disabled	Disabled

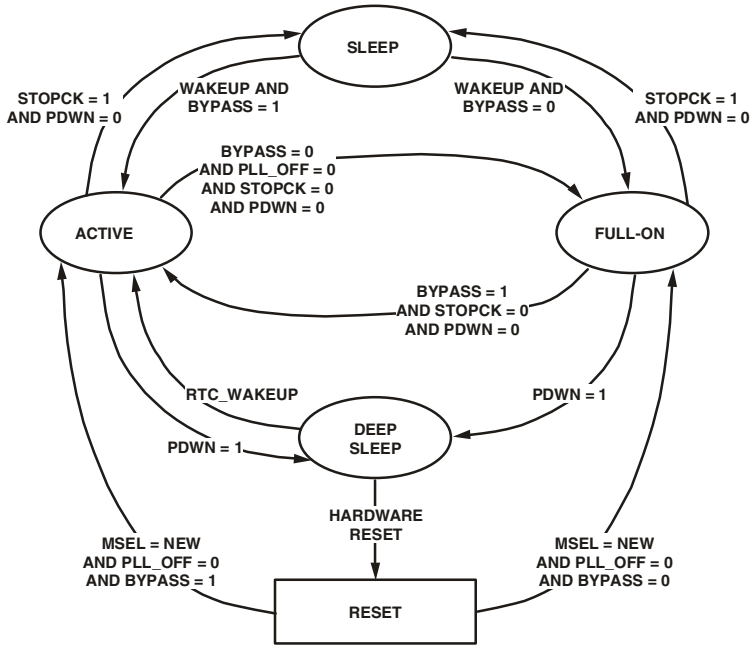


Figure 6. Mode Transitions

Power Savings

As shown in Table 4, the ADSP-BF535 Blackfin processor supports five different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF535 Blackfin processor into its own power domain, separate from the PLL, RTC, PCI, and other I/O, the processor can take advantage of dynamic power management, without affecting the PLL, RTC, or other I/O devices.

Table 4. Power Domains

Power Domain	V_{DD} Range
All internal logic, except PLL and RTC	V_{DDINT}
Analog PLL internal logic	V_{DDPLL}
RTC internal logic and crystal I/O	V_{DDRTC}
PCI I/O	$V_{DDPCIEXT}$
All other I/O	V_{DDEXT}

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the Blackfin processor family. Third Party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

EZ-KIT Lite™ for ADSP-BF535 Blackfin Processor
The EZ-KIT Lite provides developers with a cost-effective method for initial evaluation of the ADSP-BF535 Blackfin processor. The EZ-KIT Lite includes a desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a PC hosted toolset. With the EZ-KIT Lite, users can learn more about Analog Devices hardware and software development tools and prototype applications. The EZ-KIT Lite includes an evaluation suite of the VisualDSP++ development environment with C/C++ compiler, assembler, and linker. The VisualDSP++ software included with the kit is limited in program memory size and limited to use with the EZ-KIT Lite product.

Designing an Emulator Compatible Processor Board (Target)
The Analog Devices family of emulators are tools that every system developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on the ADSP-BF535 Blackfin processor. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the processor system is set running at full speed with no impact on system timing.

To use these emulators, the target's design must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues including single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68". This document is updated regularly to keep pace with improvements to emulator support.

Additional Information
This data sheet provides a general overview of the ADSP-BF535 Blackfin processor architecture and functionality. For detailed information on the Blackfin processor family core architecture and instruction set, refer to the *ADSP-BF535 Blackfin Processor Hardware Reference* and the *Blackfin Processor Instruction Set Reference*.

EZ-KIT Lite is a trademark of Analog Devices, Inc.

Table 7. Pin Descriptions (continued)

Pin	Type	Function
PF4/$\overline{\text{SPI0SEL2}}$/MSEL4	I/O	Programmable flag pin. SPI output select pin. Sensed for configuration state during hardware reset, used to configure the PLL. Selects CK to CLKIN ratio.
PF3/$\overline{\text{SPI1SEL1}}$/MSEL3	I/O	Programmable flag pin. SPI output select pin. Sensed for configuration state during hardware reset, used to configure the PLL. Selects CK to CLKIN ratio.
PF2/$\overline{\text{SPI0SEL1}}$/MSEL2	I/O	Programmable flag pin. SPI output select pin. Sensed for configuration state during hardware reset, used to configure the PLL. Selects CK to CLKIN ratio.
PF1/$\overline{\text{SPISS1}}$/MSEL1	I/O	Programmable flag pin. SPI slave select input pin. Sensed for configuration state during hardware reset, used to configure the PLL. Selects CK to CLKIN ratio.
PF0/$\overline{\text{SPISS0}}$/MSEL0	I/O	Programmable flag pin. SPI slave select input pin. Sensed for configuration state during hardware reset, used to configure the PLL. Selects CK to CLKIN ratio.
RSCLK0	I/O/T	Receive serial clock for SPORT0.
RFS0	I/O/T	Receive frame synchronization for SPORT0.
DR0	I	Serial data receive for SPORT0.
TSCLK0	I/O/T	Transmit serial clock for SPORT0.
TFS0	I/O/T	Transmit frame synchronization for SPORT0.
DT0	O	Serial data transmit for SPORT0.
RSCLK1	I/O/T	Receive serial clock for SPORT1.
RFS1	I/O/T	Receive frame synchronization for SPORT1.
DR1	I	Serial data receive for SPORT1.
TSCLK1	I/O/T	Transmit serial clock for SPORT1.
TFS1	I/O/T	Transmit frame synchronization for SPORT1.
DT1	O	Serial data transmit for SPORT1.
MOSI0	I/O	Master out slave in pin for SPI0. Supplies the output data from the master device and receives the input data to a slave device.
MISO0	I/O	Master in slave out pin for SPI0. Supplies the output data from the slave device and receives the input data to the master device.
SCK0	I/O	Clock line for SPI0. Master device output clock signal. Slave device input clock signal.
MOSI1	I/O	Master out slave in pin for SPI1. Supplies the output data from the master device and receives the input data to a slave device.
MISO1	I/O	Master in slave out pin for SPI1. Supplies the output data from the slave device and receives the input data to the master device.
SCK1	I/O	Clock line for SPI1. Master device output clock signal. Slave device input clock signal.
RX0	I	UART0 receive pin.
TX0	O	UART0 transmit pin.
RX1	I	UART1 receive pin.
TX1	O	UART1 transmit pin.
USB_CLK	I	USB clock.
XVER_DATA	I	Single ended receive data output from USB transceiver to the USBD module.
DPLS	I	Differential D+ receive data output from the USB transceiver to the UBD module.
DMNS	I	Differential D- receive data output from the USB transceiver to the USBD module.
TXDPLS	O	Transmitted D+ from the USBD module to the USB transceiver.
TXDMNS	O	Transmitted D- from the USBD module to the USB transceiver.
$\overline{\text{TXEN}}$	O	Transmit enable from the USBD module to the USB transceiver.
SUSPEND	O	Suspend mode enable output from the USBD module to the USB transceiver.
NMI	I	Non-maskable interrupt.
TCK	I	JTAG clock.
TDO	O/T	JTAG serial data out.
TDI	I	JTAG serial data in.
TMS	I	Test mode select.

Type column symbols: G = Ground, I = Input, O = Output, P = Power supply, T = Three-state

Unused Pins

Table 8 shows recommendations for tying off unused pins. All pins that are not listed in the table should be left floating.

Table 8. Recommendations for Tying Off Unused Pins

Pin	Tie Off
ARDY	V_{DDEXT}
BMODE2–0	V_{DDEXT} or GND
BYPASS	V_{DDEXT} or GND
DMNS	GND
DPLS	GND
DR0	V_{DDEXT} or GND
DR1	V_{DDEXT} or GND
NMI	GND
PCI_AD31–0	V_{DDEXT}
$\overline{\text{PCI\_CB3–0}}$	V_{DDEXT}
PCI_CLK	GND
$\overline{\text{PCI\_DEVSEL}}$	V_{DDEXT}
$\overline{\text{PCI\_FRAME}}$	V_{DDEXT}
$\overline{\text{PCI\_GNT}}$	V_{DDEXT}
PCI_IDSEL	GND
$\overline{\text{PCI\_INTA}}$	V_{DDEXT}
$\overline{\text{PCI\_INTB}}$	V_{DDEXT}
$\overline{\text{PCI\_INTC}}$	V_{DDEXT}
$\overline{\text{PCI\_INTD}}$	V_{DDEXT}
$\overline{\text{PCI\_IRDY}}$	V_{DDEXT}
$\overline{\text{PCI\_LOCK}}$	V_{DDEXT}
PCI_PAR	V_{DDEXT}
$\overline{\text{PCI\_PERR}}$	V_{DDEXT}
$\overline{\text{PCI\_RST}}$	V_{DDEXT}
$\overline{\text{PCI\_STOP}}$	V_{DDEXT}
$\overline{\text{PCI\_SERR}}$	V_{DDEXT}
$\overline{\text{PCI\_TRDY}}$	V_{DDEXT}
PF0/$\overline{\text{SPISS0}}$/MSEL0	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF1/$\overline{\text{SPISS1}}$/MSEL1	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF2/$\overline{\text{SPI0SEL1}}$/MSEL2	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF3/$\overline{\text{SPI1SEL1}}$/MSEL3	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF4/$\overline{\text{SPI0SEL2}}$/MSEL4	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF5/$\overline{\text{SPI1SEL2}}$/MSEL5	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF6/$\overline{\text{SPI0SEL3}}$/MSEL6	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF7/$\overline{\text{SPI1SEL3}}$/DF	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF8/$\overline{\text{SPI0SEL4}}$/SSEL0	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
PF9/$\overline{\text{SPI1SEL4}}$/SSEL1	V_{DDEXT} or GND (10 kΩ pull-up/pull-down required)
RX0	V_{DDEXT} or GND
RX1	V_{DDEXT} or GND
TCK	V_{DDEXT}
TDI	V_{DDEXT}
TMS	V_{DDEXT}
$\overline{\text{TRST}}$	GND
USB_CLK	GND
$V_{DDPCIEXT}$	V_{DDEXT}
V_{DDRTC}	V_{DDEXT}
XTAL1	V_{DDEXT} or GND
XVER_DATA	GND

ABSOLUTE MAXIMUM RATINGS

Internal (Core) Supply Voltage (V_{DDINT})[1] . . . . . −0.3 V to +1.65 V
External (I/O) Supply Voltage (V_{DDEXT})[1] . . . . . −0.3 V to +4.0 V
Input Voltage[1] . . . . . −0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing[1] . . . . . −0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance[1, 2] . . . . . 200 pF
Core Clock: [1]
ADSP-BF535PKB-350 . . . . . 350 MHz
ADSP-BF535PKB-300 . . . . . 300 MHz
ADSP-BF535PBB-300 . . . . . 300 MHz
ADSP-BF535PBB-200 . . . . . 200 MHz
System Clock (SCLK)[1] . . . . . 133 MHz
Storage Temperature Range[1] . . . . . −65°C to +150°C

[1] Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] For proper SDRAM controller operation, the maximum load capacitance is 50 pF for ADDR, DATA, $\overline{ABE3–0}$/SDQM3–0, CLKOUT/SCLK1, SCLK0, SCKE, SA10, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, and $\overline{SMS3\text{-}0}$.

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-BF535 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Table 9 and Table 10 describe the timing requirements for the ADSP-BF535 Blackfin processor clocks. Take care in selecting MSEL and SSEL ratios so as not to exceed the maximum core clock, system clock and Voltage Controlled Oscillator (VCO) operating frequencies, as described in Absolute Maximum Ratings on Page 22. Table 10 describes phase-locked loop operating conditions.

Table 9. Core Clock Requirements

Parameter		Min	Max	Unit
$t_{CCLK1.6}$	Core Cycle Period (V_{DDINT} = 1.6 V–50 mV)	2.86	200	ns
$t_{CCLK1.5}$	Core Cycle Period (V_{DDINT} = 1.5 V–5%)	3.33	200	ns
$t_{CCLK1.4}$	Core Cycle Period (V_{DDINT} = 1.4 V–5%)	3.70	200	ns
$t_{CCLK1.3}$	Core Cycle Period (V_{DDINT} = 1.3 V–5%)	4.17	200	ns
$t_{CCLK1.2}$	Core Cycle Period (V_{DDINT} = 1.2 V–5%)	4.76	200	ns
$t_{CCLK1.1}$	Core Cycle Period (V_{DDINT} = 1.1 V–5%)	5.56	200	ns
$t_{CCLK1.0}$	Core Cycle Period (V_{DDINT} = 1.0 V–5%)	6.67	200	ns

Table 10. Phase-Locked Loop Operating Conditions

Parameter	Min	Nominal	Max	Unit
Operating Voltage	1.425	1.5	1.575	V
Jitter, Rising Edge to Rising Edge, Per Output[1]			120	ps
Jitter, Rising Edge to Falling Edge, Per Output[1]			60	ps
Skew, Rising Edge to Rising Edge, Any Two Outputs[1]			120	ps
Voltage Controlled Oscillator (VCO) Frequency[1]	40		400	MHz
V_{DDPLL} Induced Jitter[1]			1	ps/mV

[1] Guaranteed but not tested.

Clock and Reset Timing

Table 11 and Figure 8 describe clock and reset operations. Per ABSOLUTE MAXIMUM RATINGS on Page 22, combinations of CLKIN and clock multipliers must not select core and system clocks in excess of 350/300/200 MHz and 133 MHz, respectively.

Table 11. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse[1]	10.0		ns
t_{CKINH}	CLKIN High Pulse[1]	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[2]	$11 \times t_{CKIN}$		ns
t_{MSD}	Delay from $\overline{\text{RESET}}$ Asserted to MSELx, SSELx, BYPASS, and DF Valid[3]		15.0	ns
t_{MSS}	MSELx/SSELx/DF/BYPASS Stable Setup Before $\overline{\text{RESET}}$ Deasserted[4]	$2 \times t_{CKIN}$		ns
t_{MSH}	MSELx/SSELx/DF/BYPASS Stable Hold After $\overline{\text{RESET}}$ Deasserted	$2 \times t_{CKIN}$		ns
Switching Characteristics				
t_{PFD}	Flag Output Disable Time After $\overline{\text{RESET}}$ Asserted		15.0	ns

[1] Applies to Bypass mode and Non-bypass mode.
[2] Applies after power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles, while $\overline{\text{RESET}}$ is asserted, assuming stable power supplies and CLKIN (not including start-up time of external clock oscillator).
[3] SSELx, MSELx and DF values can change from this point, but the values must be valid.
[4] SSELx, MSELx and DF values must be held from this time, until the hold time expires.

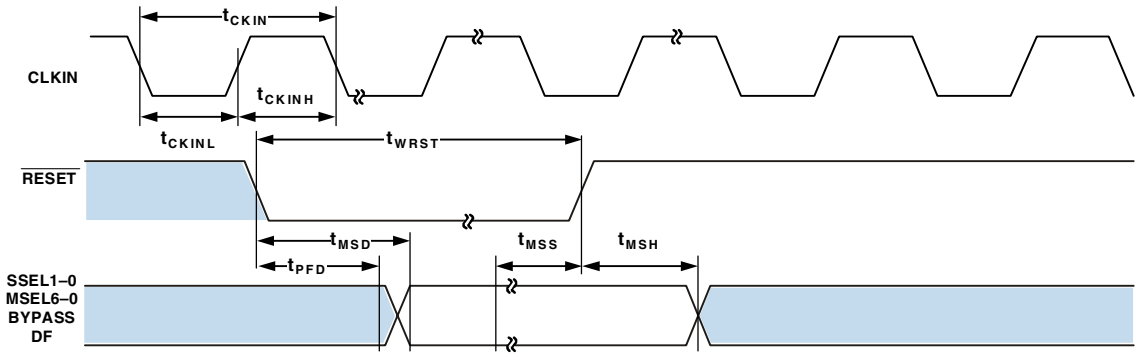


Figure 8. Clock and Reset Timing

Programmable Flags Cycle Timing

Table 12 and Figure 9 describe programmable flag operations.

Table 12. Programmable Flags Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{HFIES}	Edge Sensitive Flag Input Hold is Asynchronous	3.0		ns
t_{HFILS}	Level Sensitive Flag Input Hold	t_{SCLK}+3		ns
Switching Characteristics				
t_{DFO}	Flag Output Delay with Respect to SCLK		6.0	ns
t_{HFO}	Flag Output Hold After SCLK High		6.0	ns

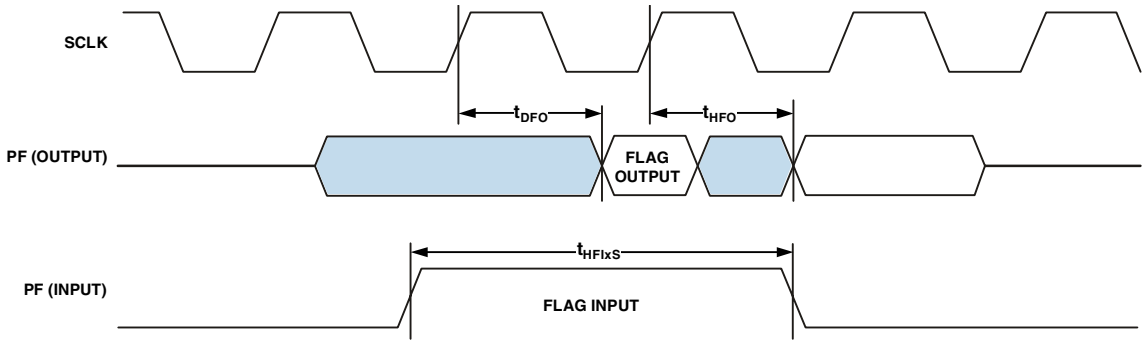


Figure 9. Programmable Flags Cycle Timing

Asynchronous Memory Read Cycle Timing

Table 15 and Figure 12 describe Asynchronous Memory Read Cycle timing.

Table 15. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA31–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA31–0 Hold After CLKOUT	2.6		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	–1.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		7.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3–0}$, $\overline{ABE3–0}$, ADDR25–2, $\overline{AOE}$, $\overline{ARE}$.

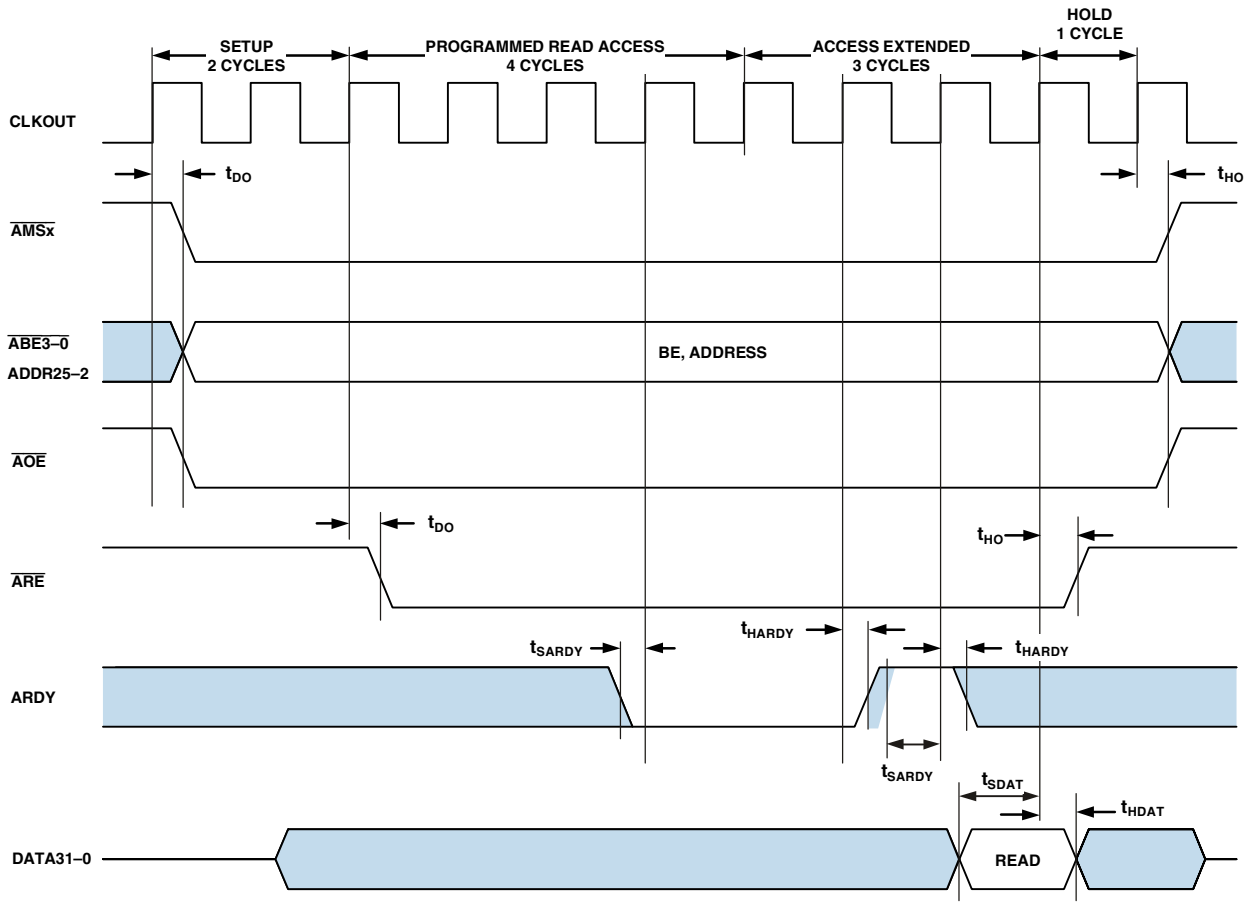


Figure 12. Asynchronous Memory Read Cycle Timing

SDRAM Interface Timing

For proper SDRAM controller operation, the maximum load capacitance is 50 pF for ADDR, DATA, $\overline{ABE3–0}$/SDQM3–0, CLKOUT/SCLK1, SCLK0, SCKE, SA10, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, and $\overline{SMS3-0}$.

Table 16. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before SCLK0/SCLK1	2.1		ns
t_{HSDAT}	DATA Hold After SCLK0/SCLK1	2.8		ns
Switching Characteristics				
t_{SCLK}	SCLK0/SCLK1 Period	7.5		ns
t_{SCLKH}	SCLK0/SCLK1 Width High	2.5		ns
t_{SCLKL}	SCLK0/SCLK1 Width Low	2.5		ns
t_{DCAD}	Command, ADDR, Data Delay After SCLK0/SCLK1[1]		6.0	ns
t_{HCAD}	Command, ADDR, Data Hold After SCLK0/SCLK1[1]	0.8		ns
t_{DSDAT}	Data Disable After SCLK0/SCLK1		6.0	ns
t_{ENSDAT}	Data Enable After SCLK0/SCLK1	1.0		ns

[1] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM3–0, $\overline{SMS}$, SA10, and SCKE.

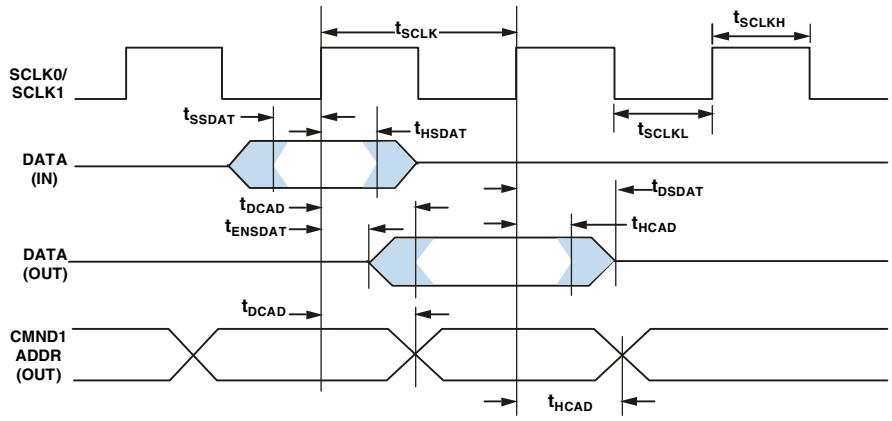


Figure 13. SDRAM Interface Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 17 describes UART port receive and transmit operations. The maximum baud rate is SCLK/16. As shown in Figure 17, there is some latency between the generation of internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

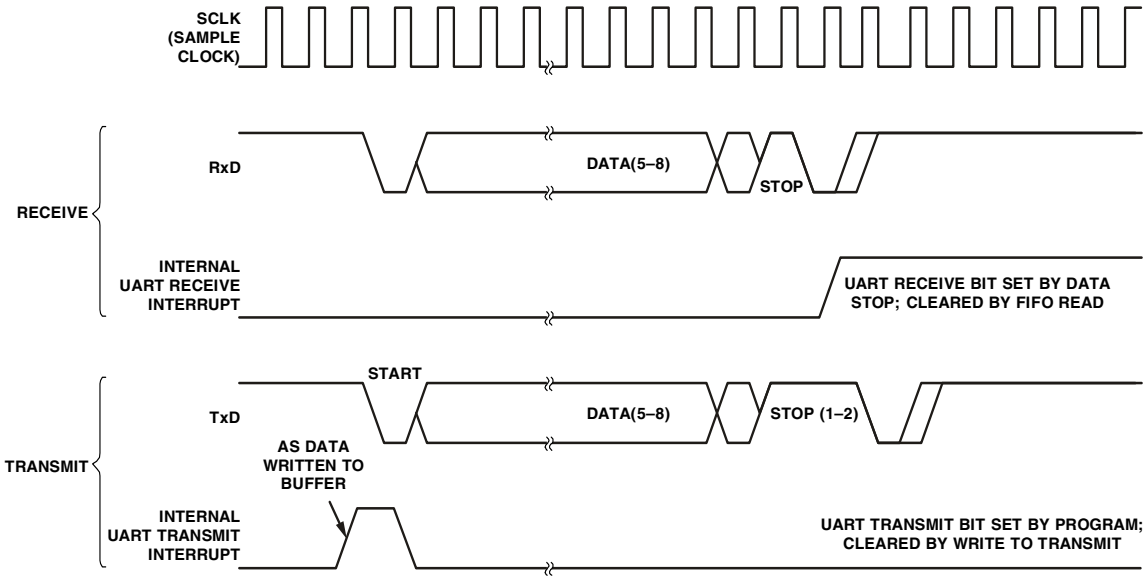


Figure 17. UART Port—Receive and Transmit Timing

Output Drive Currents

Figure 19 through Figure 21 show typical current-voltage characteristics for the output drivers of the ADSP-BF535 Blackfin processor. The curves represent the current drive capability of the output drivers as a function of output voltage. Figure 19 applies to the ABE3–0, SDQM3–0, ADDR25–2, AMS3–0, AOE, ARE, AWE, CLKOUT, SCLK1, DATA31–0, DT1–0, EMU, MISO1–0, MOSI1–0, PF15–0, RFS1–0, RSCLK1–0, SA10, SCAS, SCK1–0, SCKE, SCLK0, DEEPSLEEP, SMS3–0, SRAS, SUSPEND, SWE, TDO, TFS1–0, TMR2–0, TSCLK1–0, TX1–0, TXDMNS, TXDPLS, TXEN, and XTAL0 pins. Figure 20 applies to the PCI_AD31–0, PCI_CBE3–0, PCI_DEVSEL, PCI_FRAME, PCI_INTA, PCI_IRDY, PCI_PAR, PCI_PERR, PCI_RST, PCI_SERR, PCI_STOP, and PCI_TRDY pins. Figure 21 applies to the PCI_REQ pin.

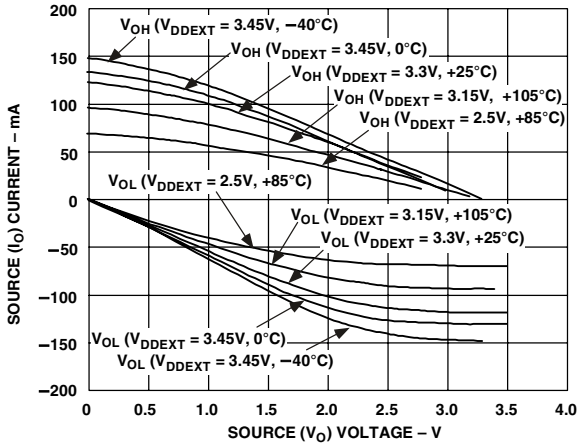


Figure 19. Output Drive Current

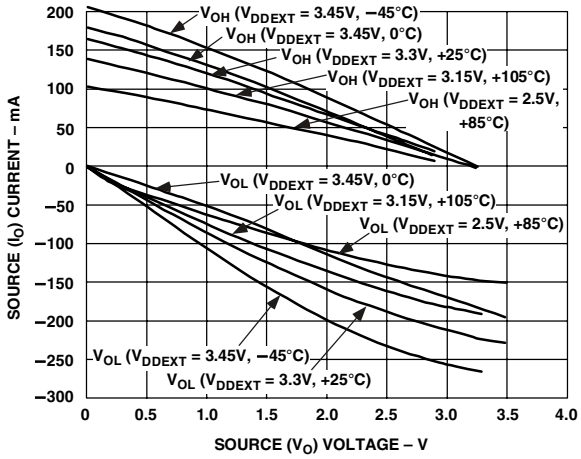


Figure 20. PCI 33 MHz Output Drive Current

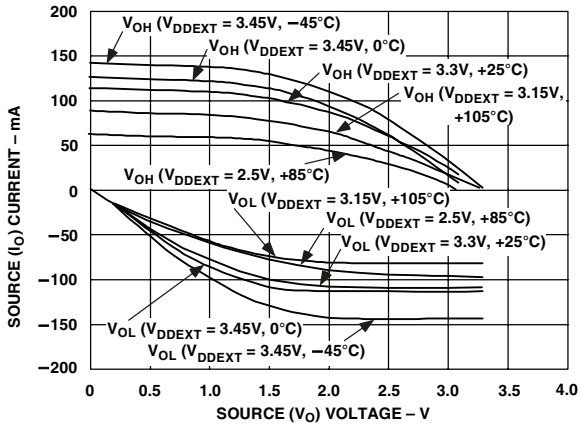


Figure 21. PCI_REQ Output Drive Current

Power Dissipation

Total power dissipation has two components: one due to internal circuitry (P_{INT}) and one due to the switching of external output drivers (P_{EXT}). Table 26 shows the power dissipation for internal circuitry (V_{DDINT}). Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Table 27 shows the power dissipation for the phase-locked loop (PLL) circuitry (V_{DDPLL}).

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- Maximum frequency (f_0) at which all output pins can switch during each cycle
- Their load capacitance (C_0) of all switching pins
- Their voltage swing (V_{DDEXT})

The external component is calculated using:

$$P_{EXT} = V_{DDEXT}^{2} \times \sum C_0 \times f_0$$

Table 26. Internal Power Dissipation

	Test Conditions[1]				
Parameter	**f_{CCLK} = 100 MHz V_{DDINT} = 1.0 V**	**f_{CCLK} = 200 MHz V_{DDINT} = 1.2 V**	**f_{CCLK} = 300 MHz V_{DDINT} = 1.5 V**	**f_{CCLK} = 350 MHz V_{DDINT} = 1.6 V**	**Unit**
I_{DDTYP}[2]	96.0	206.0	387.0	498.0	mA
I_{DDEFR}[3]	114.0	248.0	463.0	579.0	mA
$I_{DDSLEEP}$[4]	15.0	29.0	52.0	62.0	mA
$I_{DDDEEPSLEEP}$[4]	4.0	5.0	8.2	9.8	mA
$I_{DDRESET}$[5]	132.0	255.0	485.3	651.0	mA

[1] I_{DD} data is specified for typical process parameters. All data at 25°C.
[2] Processor executing 75% dual Mac, 25% ADD with moderate data bus activity.
[3] Implementation of Enhanced Full Rate (EFR) GSM algorithm.
[4] See the *ADSP-BF535 Blackfin Processor Hardware Reference Manual* for definitions of Sleep and Deep Sleep operating modes.
[5] I_{DD} is specified for when the device is in the reset state.

Table 27. PLL Power Dissipation

Parameter	Test Conditions	Typical	Unit
I_{DDPLL}	V_{DDPLL} = 1.5 V, 25°C	4.0	mA

The frequency f includes driving the load high and then back low. For example: DATA31–0 pins can drive high and low at a maximum rate of 1/(2 × t_{SCLK}) while in SDRAM burst mode.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DD} \times V_{DDINT})$$

Note that the conditions causing a worst-case P_{EXT} differ from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones (1s) to all zeros (0s). Note, as well, that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Test Conditions

All timing parameters appearing in this data sheet were measured under the conditions described in this section.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown in the Output Enable/Disable diagram (Figure 22). The time $t_{ENA\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage reaches 2.0 V (output high) or 1.0 V (output low). Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the 1.0 V or 2.0 V trip voltage. Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V) / I_L$$

The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown in Figure 22. The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF535 Blackfin processor's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (for example, t_{DSDAT} for an SDRAM write cycle).

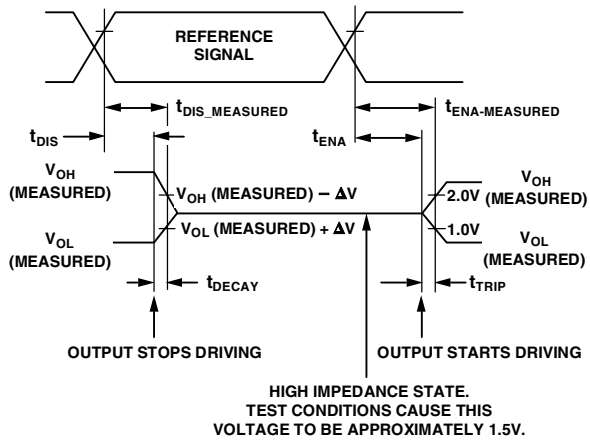


Figure 22. Output Enable/Disable

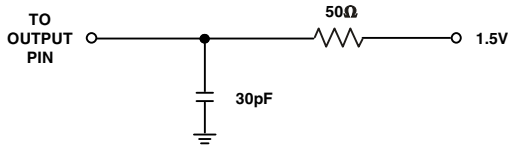


Figure 23. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

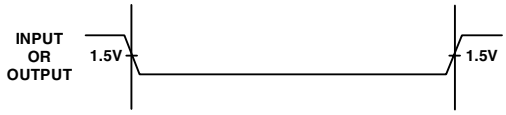


Figure 24. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Environmental Conditions

The ADSP-BF535 is offered in a 260-ball PBGA package.

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 28

P_D = Power dissipation (see Power Dissipation on Page 36 for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 28, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 28. Thermal Characteristics

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	23.8	°C/W
θ_{JMA}	1 linear m/s air flow	20.8	°C/W
θ_{JMA}	2 linear m/s air flow	19.8	°C/W
θ_{JB}		9.95	°C/W
θ_{JC}		9.35	°C/W
Ψ_{JT}	0 linear m/s air flow	0.30	°C/W