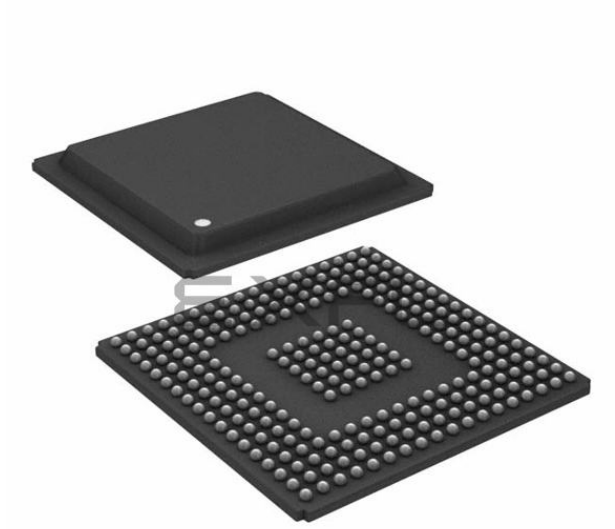

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	PCI, SPI, SSP, UART, USB
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	308kB
Voltage - I/O	3.30V
Voltage - Core	1.50V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	260-BBGA
Supplier Device Package	260-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf535pkb-300

- VisualDSP++® 5.0 Loader and Utilities Manual
- VisualDSP++® 5.0 Product Release Bulletin
- VisualDSP++® 5.0 Quick Installation Reference Card
- VisualDSP++® 5.0 Users Guide

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TOOLS AND SIMULATIONS

- Blackfin Processors Software and Tools

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

DESIGN RESOURCES

- ADSP-BF535 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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External Memory Control
The External Bus Interface Unit (EBIU) on the ADSP-BF535 Blackfin processor provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The controller is made up of two sections: the first is an SDRAM controller for connection of industry-standard synchronous DRAM devices and DIMMs (Dual Inline Memory Module), while the second is an asynchronous memory controller intended to interface to a variety of memory devices.

PC133 SDRAM Controller
The SDRAM controller provides an interface to up to four separate banks of industry-standard SDRAM devices or DIMMs, at speeds up to f_{SCLK}. Fully compliant with the PC133 SDRAM standard, each bank can be configured to contain between 16M bytes and 128M bytes of memory.

The controller maintains all of the banks as a contiguous address space so that the processor sees this as a single address space, even if different size devices are used in the different banks. This enables a system design where the configuration can be upgraded after delivery with either similar or different memories.

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The memory banks can be configured as either 32 bits wide for maximum performance and bandwidth or 16 bits wide for minimum device count and lower system cost.

All four banks share common SDRAM control signals and have their own bank select lines providing a completely glueless interface for most system configurations.

The SDRAM controller address, data, clock, and command pins can drive loads up to 50 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 50 pF.

Asynchronous Controller
The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, ROM, and flash EPROM, as well as I/O devices that interface with standard memory control lines. Each bank occupies a 64 Mbyte window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic. The banks can also be configured as 16-bit wide or 32-bit wide buses for ease of interfacing to a range of memories and I/O devices tailored either to high performance or to low cost and power.

PCI Interface
The ADSP-BF535 Blackfin processor provides a glueless logical and electrical, 33 MHz, 3.3 V, 32-bit PCI (Peripheral Component Interconnect), Revision 2.2 compliant interface. The PCI interface is designed for a 3 V signalling environment. The PCI interface provides a bus bridge function between the processor core and on-chip peripherals and an external PCI bus. The PCI interface of the ADSP-BF535 Blackfin processor supports two PCI functions:

- A host to PCI bridge function, in which the ADSP-BF535 Blackfin processor resources (the processor core, internal and external memory, and the memory DMA controller) provide the necessary hardware components to emulate a host computer PCI interface, from the perspective of a PCI target device.
- A PCI target function, in which an ADSP-BF535 Blackfin processor based intelligent peripheral can be designed to easily interface to a Revision 2.2 compliant PCI bus.

PCI Host Function
As the PCI host, the ADSP-BF535 Blackfin processor provides the necessary PCI host (platform) functions required to support and control a variety of off-the-shelf PCI I/O devices (for example, Ethernet controllers, bus bridges, and so on) in a system in which the ADSP-BF535 Blackfin processor is the host.

Note that the Blackfin processor architecture defines only memory space (no I/O or configuration address spaces). The three address spaces of PCI space (memory, I/O, and configuration space) are mapped into the flat 32-bit memory space of the ADSP-BF535 Blackfin processor. Because the PCI memory space is as large as the ADSP-BF535 Blackfin processor memory address space, a windowed approach is employed, with separate windows in the ADSP-BF535 Blackfin processor address space used for accessing the three PCI address spaces. Base address registers are provided so that these windows can be positioned to view any range in the PCI address spaces while the windows remain fixed in position in the ADSP-BF535 Blackfin processor's address range.

For devices on the PCI bus viewing the ADSP-BF535 Blackfin processor's resources, several mapping registers are provided to enable resources to be viewed in the PCI address space. The ADSP-BF535 Blackfin processor's external memory space, internal L2, and some I/O MMRs can be selectively enabled as memory spaces that devices on the PCI bus can use as targets for PCI memory transactions.

PCI Target Function
As a PCI target device, the PCI host processor can configure the ADSP-BF535 Blackfin processor subsystem during enumeration of the PCI bus system. Once configured, the ADSP-BF535 Blackfin processor subsystem acts as an intelligent I/O device. When configured as a target device, the PCI controller uses the memory DMA controller to perform DMA transfers as required by the PCI host.

USB Device
The ADSP-BF535 Blackfin processor provides a USB 1.1 compliant device type interface to support direct connection to a host system. The USB core interface provides a flexible programmable environment with up to eight endpoints. Each endpoint can support all of the USB data types including control, bulk, interrupt, and isochronous. Each endpoint provides a memory-mapped buffer for transferring data to the application. The ADSP-BF535 Blackfin processor USB port has a dedicated

includes support for 5 to 8 data bits; 1 or 2 stop bits; and none, even, or odd parity. The UART ports support two modes of operation.

- PIO (Programmed I/O)—The processor sends or receives data by writing or reading I/O-mapped UATX or UARX registers, respectively. The data is double-buffered on both transmit and receive.
- DMA (Direct Memory Access)—The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. The DMA channels have lower priority than most DMA channels because of their relatively low service rates.

Each UART port's baud rate (see Figure 5), serial data format, error code generation and status, and interrupts are programmable:

- Bit rates ranging from (f_{SCLK}/1048576) to (f_{SCLK}/16) bits per second
- Data formats from 7 to 12 bits per frame
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times D}$$

Figure 5. UART Clock Rate Calculation

Autobaud detection is supported, in conjunction with the general-purpose timer functions.

The capabilities of UART0 are further extended with support for the Infrared Data Association (IrDA Serial Infrared Physical Layer Link Specification (SIR) protocol.

Programmable Flags (PFX)

The ADSP-BF535 Blackfin processor has 16 bidirectional, general-purpose I/O programmable flag (PF15–0) pins. The programmable flag pins have special functions for clock multiplier selection, SROM boot mode, and SPI port operation. For more information, see Serial Peripheral Interface (SPI) Ports on Page 10 and Clock Signals on Page 13. Each programmable flag can be individually controlled by manipulation of the flag control, status, and interrupt registers.

- Flag Direction Control Register—Specifies the direction of each individual PFx pin as input or output.
- Flag Control and Status Registers—Rather than forcing the software to use a read-modify-write process to control the setting of individual flags, the ADSP-BF535 Blackfin processor employs a "write one to set" and "write one to clear" mechanism that allows any combination of individual flags to be set or cleared in a single instruction, without affecting the level of any other flags. Two control registers are provided, one register is written to in order to set flag values while another register is written to in order to clear flag values. Reading the flag status register allows software to interrogate the sense of the flags.
- Flag Interrupt Mask Registers—The two flag interrupt mask registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two flag control registers that are used to set and clear individual flag values, one flag interrupt mask register sets bits to enable interrupt function, and the other flag interrupt mask register clears bits to disable interrupt function. PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be configured to generate software interrupts.
- Flag Interrupt Sensitivity Registers—The two flag interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify (if edge-sensitive) whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

Dynamic Power Management

The ADSP-BF535 Blackfin processor provides four operating modes, each with a different performance/power dissipation profile. In addition, dynamic power management provides the control functions, with the appropriate external power regulation capability to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the ADSP-BF535 Blackfin processor peripherals also reduces power dissipation. See Table 3 for a summary of the power settings for each mode.

Full On Operating Mode
– Maximum Performance

In the full on mode, the PLL is enabled, and is not bypassed, providing the maximum operational frequency. This is the normal execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode
– Moderate Power Savings

In the active mode, the PLL is enabled, but bypassed. The input clock (CLKIN) is used to generate the clocks for the processor core (CCLK) and peripherals (SCLK). When the PLL is bypassed, CCLK runs at one-half the CLKIN frequency. Significant power savings can be achieved with the processor running at one-half the CLKIN frequency. In this mode, the PLL multiplication ratio can be changed by setting the appropriate values in the SSEL fields of the PLL control register (PLL_CTL).

When in the active mode, system DMA access to appropriately configured L1 memory is supported.

Sleep Operating Mode
– High Power Savings

The sleep mode reduces power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Any interrupt, typically via some external event or RTC activity, will wake up the processor. When in sleep mode, assertion of any interrupt will cause the processor to sense the value of the bypass bit

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in power dissipation, while reducing the voltage by 25% reduces power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and power are both reduced, the power savings are dramatic.

Dynamic Power Management allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically and independently controlled.

As previously explained, the savings in power dissipation can be modeled by the following equation:

$$Power\ Dissipation\ Factor = \left(\frac{f_{CCLKRED}}{f_{CCLKNOM}}\right) \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2$$

where:

$f_{CCLKNOM}$ is the nominal core clock frequency (300 MHz)

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage (1.5 V)

$V_{DDINTRED}$ is the reduced internal supply voltage

As an example of how significant the power savings of Dynamic Power Management are when both frequency and voltage are reduced, consider an example where the frequency is reduced from its nominal value to 50 MHz and the voltage is reduced from its nominal value to 1.2 V. At this reduced frequency and voltage, the processor dissipates about 10% of the power dissipated at nominal frequency and voltage.

Peripheral Power Control

The ADSP-BF535 Blackfin processor provides additional power control capability by allowing dynamic scheduling of clock inputs to each of the peripherals. Clocking to each of the peripherals listed below can be enabled or disabled by appropriately setting the peripheral's control bit in the peripheral clock enable register (PLL_IOCK). The Peripheral Clock Enable Register allows individual control for each of these peripherals:

- PCI
- EBIU controller
- Programmable flags
- MemDMA controller
- SPORT 0
- SPORT 1
- SPI 0
- SPI 1
- UART 0
- UART 1
- Timer 0, Timer 1, Timer 2
- USB CLK

Clock Signals

The ADSP-BF535 Blackfin processor can be clocked by a sine wave input or a buffered shaped clock derived from an external clock oscillator.

If a buffered, shaped clock is used, this external clock connects to the processor CLKIN pin. The CLKIN input cannot be halted, changed, or operated below the specified frequency during normal operation. This clock signal should be a 3.3 V LVTTL compatible signal. The processor provides a user-programmable 1× to 31× multiplication of the input clock to support external-to-internal clock ratios. The MSEL6–0, BYPASS, and DF pins decide the PLL multiplication factor at reset. At run time, the multiplication factor can be controlled in software. The combination of pull-up and pull-down resistors in Figure 7 sets up a core clock ratio of 6:1, which, for example, produces a 150 MHz core clock from the 25 MHz input. For other clock multiplier settings, see the *ADSP-BF535 Blackfin Processor Hardware Reference*.

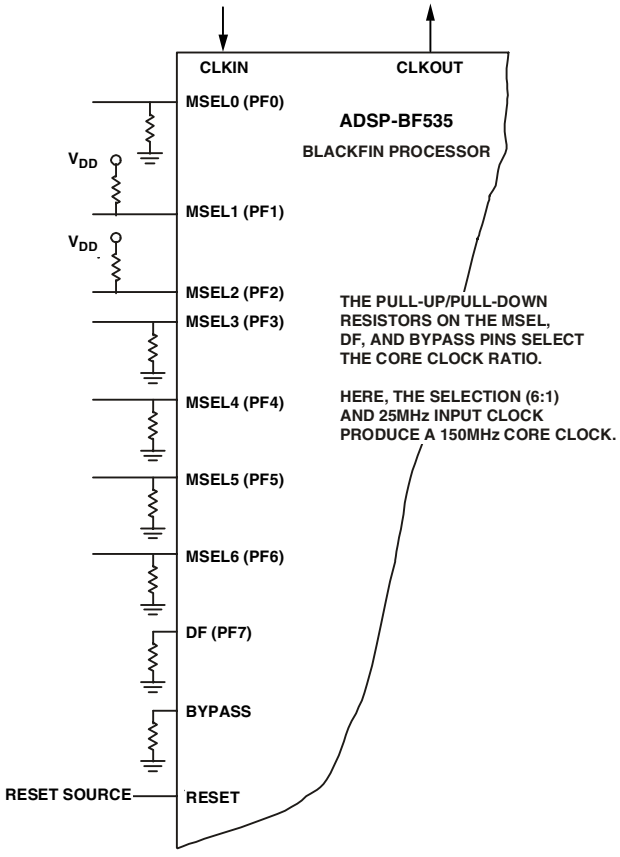

Figure 7. Clock Ratio Example

All on-chip peripherals operate at the rate set by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL pins. At run time the system clock frequency can be controlled in software by writing to the SSEL fields in the PLL control register (PLL_CTL). The values programmed into the

SSEL fields define a divide ratio between the core clock (CCLK) and the system clock. Table 5 illustrates the system clock ratios. The system clock is supplied to the CLKOUT_SCLK0 pin.

Table 5. System Clock Ratios

Signal Name	Divider Ratio	Example Frequency Ratios (MHz)	
SSEL1–0	CCLK/SCLK	CCLK	SCLK
00	2:1	266	133
01	2.5:1	275	110
10	3:1	300	100
11	4:1	300	75

The maximum frequency of the system clock is f_{SCLK}. Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The reset value of the SSEL1–0 is determined by sampling the SSEL1 and SSEL0 pins during reset. The SSEL value can be changed dynamically by writing the appropriate values to the PLL control register (PLL_CTL), as described in the *ADSP-BF535 Blackfin Processor Hardware Reference*.

Booting Modes

The ADSP-BF535 has three mechanisms (listed in Table 6) for automatically loading internal L2 memory after a reset. A fourth mode is provided to execute from external memory, bypassing the boot sequence.

Table 6. Booting Modes

BMODE2–0	Description
000	Execute from 16-bit external memory (Bypass Boot ROM)
001	Boot from 8-bit flash
010	Boot from SPI0 serial ROM (8-bit address range)
011	Boot from SPI0 serial ROM (16-bit address range)
100–111	Reserved

The BMODE pins of the reset configuration register, sampled during power-on resets and software initiated resets, implement these modes:

- Execute from 16-bit external memory—Execution starts from address 0x2000000 with 16-bit packing. The boot ROM is bypassed in this mode.
- Boot from 8-bit external flash memory—The 8-bit flash boot routine located in boot ROM memory space is set up using asynchronous Memory Bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from SPI serial EEPROM (8-bit addressable)—The SPI0 uses PF10 output pin to select a single SPI EPROM device, submits a read command at address 0x00, and begins clocking data into the beginning of L2 memory. An 8-bit addressable SPI compatible EPROM must be used.
- Boot from SPI serial EEPROM (16-bit addressable)—The SPI0 uses PF10 output pin to select a single SPI EPROM device, submits a read command at address 0x0000, and begins clocking data into the beginning of L2 memory. A 16-bit addressable SPI compatible EPROM must be used.

For each of the boot modes described above, a four-byte value is first read from the memory device. This value is used to specify a subsequent number of bytes to be read into the beginning of L2 memory space. Once each of the loads is complete, the processor jumps to the beginning of L2 space and begins execution.

In addition, the reset configuration register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L2 memory space.

To augment the boot modes, a secondary software loader is provided that adds additional booting mechanisms. This secondary loader provides the capability to boot from PCI, 16-bit flash memory, fast flash, variable baud rate, and so on.

Instruction Set Description

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both a user (algorithm/application code) and a supervisor (O/S kernel, device drivers, debuggers, ISRs) mode of operations, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/CPU features are optimized for both 8-bit and 16-bit operations.
- A super pipelined multi issue load/store modified Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4 Gbyte memory space providing a simplified programming model.

- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and kernel stack pointers.
- Code density enhancements, which include intermixing of 16- and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded as 16-bits.

Development Tools

The ADSP-BF535 Blackfin processor is supported with a complete set of software and hardware development tools, including Analog Devices emulators and the VisualDSP++™ development environment. The same emulator hardware that supports other Analog Devices JTAG processors, also fully emulates the ADSP-BF535 Blackfin processor.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ run-time library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to Blackfin processor assembly. The Blackfin processor has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- View the internal pipeline to further optimize peripherals
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDDE lets programmers define and manage software development. Its dialog boxes and property pages let programmers configure and manage all development tools, including color syntax highlighting in the VisualDSP++ editor. These capabilities permit programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of embedded, real-time programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK based objects, and visualizing the system state, when debugging an application that uses the VDK.

VCSE is Analog Devices technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. Download components from the Web and drop them into the application. Publish component archives from within VisualDSP++. VCSE supports component implementation in C/C++ or assembly language.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the processor or external memory with the drag of the mouse, examine run-time stack and heap usage. The Expert Linker is fully compatible with existing Linker Definition File (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices emulators use the IEEE 1149.1 JTAG test access port of the ADSP-BF535 Blackfin processor to monitor and control the target board processor during emulation. The emulator provides full speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusively in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

VisualDSP++ is a trademark of Analog Devices, Inc.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the Blackfin processor family. Third Party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

EZ-KIT Lite™ for ADSP-BF535 Blackfin Processor
The EZ-KIT Lite provides developers with a cost-effective method for initial evaluation of the ADSP-BF535 Blackfin processor. The EZ-KIT Lite includes a desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a PC hosted toolset. With the EZ-KIT Lite, users can learn more about Analog Devices hardware and software development tools and prototype applications. The EZ-KIT Lite includes an evaluation suite of the VisualDSP++ development environment with C/C++ compiler, assembler, and linker. The VisualDSP++ software included with the kit is limited in program memory size and limited to use with the EZ-KIT Lite product.

Designing an Emulator Compatible Processor Board (Target)
The Analog Devices family of emulators are tools that every system developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on the ADSP-BF535 Blackfin processor. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the processor system is set running at full speed with no impact on system timing.

To use these emulators, the target's design must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues including single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68". This document is updated regularly to keep pace with improvements to emulator support.

Additional Information
This data sheet provides a general overview of the ADSP-BF535 Blackfin processor architecture and functionality. For detailed information on the Blackfin processor family core architecture and instruction set, refer to the *ADSP-BF535 Blackfin Processor Hardware Reference* and the *Blackfin Processor Instruction Set Reference*.

EZ-KIT Lite is a trademark of Analog Devices, Inc.

Table 7. Pin Descriptions (continued)

Pin	Type	Function
$\overline{\text{TRST}}$	I	JTAG reset.
$\overline{\text{RESET}}$	I	When this pin is asserted to logic zero level for at least 10 CLKIN cycles, a hardware reset is initiated. The minimum pulse width for power-on reset is 40 µs.
CLKIN1	I	Clock in.
BYPASS	I	Dedicated mode pin. May be permanently strapped to V_{DD} or V_{SS}. Bypasses the on-chip PLL.
DEEPSLEEP	O	Denotes that the Blackfin processor core is in Deep Sleep mode.
BMODE2–0	I	Dedicated mode pin. May be permanently strapped to V_{DD} or V_{SS}. Configures the boot mode that is employed following hardware reset or software reset.
PCI_AD31–0	I/O/T	PCI address and data bus.
$\overline{\text{PCI\_CBE3–0}}$	I/O/T	PCI byte enables.
$\overline{\text{PCI\_FRAME}}$	I/O/T	PCI frame signal. Used by PCI initiators for signalling the beginning and end of a PCI transaction.
$\overline{\text{PCI\_IRDY}}$	I/O/T	PCI initiator ready signal.
$\overline{\text{PCI\_TRDY}}$	I/O/T	PCI target ready signal.
$\overline{\text{PCI\_DEVSEL}}$	I/O/T	PCI device select signal. Asserted by targets of PCI transactions to claim the transaction.
$\overline{\text{PCI\_STOP}}$	I/O/T	PCI stop signal.
$\overline{\text{PCI\_PERR}}$	I/O/T	PCI parity error signal.
PCI_PAR	I/O/T	PCI parity signal.
$\overline{\text{PCI\_REQ}}$	O	PCI request signal. Used for requesting the use of the PCI bus.
$\overline{\text{PCI\_SERR}}$	I/O/T	PCI system error signal. Requires a pull-up on the system board.
$\overline{\text{PCI\_RST}}$	I/O/T	PCI reset signal.
$\overline{\text{PCI\_GNT}}$	I	PCI grant signal. Used for granting access to the PCI bus.
PCI_IDSEL	I	PCI initialization device select signal. Individual device selects for targets of PCI configuration transactions.
$\overline{\text{PCI\_LOCK}}$	I	PCI lock signal. Used to lock a target or the entire PCI bus for use by the master that asserts the lock.
PCI_CLK	I	PCI clock.
$\overline{\text{PCI\_INTA}}$	I/O/T	PCI interrupt A line on PCI bus. Asserted by the ADSP-BF535 Blackfin processor as a device-to-signal an interrupt to the system processor. Monitored by the ADSP-BF535 when acting as the system processor.
$\overline{\text{PCI\_INTB}}$	I	PCI interrupt B line. Monitored by ADSP-BF535 Blackfin processor when acting as the system processor.
$\overline{\text{PCI\_INTC}}$	I	PCI interrupt C line. Monitored by the ADSP-BF535 Blackfin processor when acting as the system processor.
$\overline{\text{PCI\_INTD}}$	I	PCI interrupt D line. Monitored by the ADSP-BF535 Blackfin processor when acting as the system processor.
XTAL1	I	Real-Time Clock oscillator input.
XTAL0	O	Real-Time Clock oscillator output.
$\overline{\text{EMU}}$	O	Emulator acknowledge, open drain. Must be connected to the ADSP-BF535 Blackfin processor emulator target board connector only.
V_{DDPLL}	P	PLL power supply (1.5 V nominal).
V_{DDRTC}	P	Real-Time Clock power supply (3.3 V nominal).
V_{DDEXT}	P	I/O (except PCI) power supply (3.3 V nominal).
$V_{DDPCIEXT}$	P	PCI I/O power supply (3.3 V nominal).
V_{DDINT}	P	Internal power supply (1.5 V nominal).
GND	G	Power supply return.

Type column symbols: G = Ground, I = Input, O = Output, P = Power supply, T = Three-state

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Min	Nominal	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage[1]				
	ADSP-BF535PKB-350	0.95	1.6	1.65	V
	ADSP-BF535PKB-300	0.95	1.5	1.575	V
	ADSP-BF535PBB-300	0.95	1.5	1.575	V
	ADSP-BF535PBB-200	0.95	1.5	1.575	V
V_{DDEXT}	External (I/O) Supply Voltage[1]	3.15	3.3	3.45	V
V_{DDPLL}	PLL Power Supply Voltage[1]	1.425	1.5	1.575	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage[1]	2.60	3.3	3.45	V
$V_{DDPCIEXT}$	PCI I/O Power Supply Voltage[1]	3.15	3.3	3.45	V
V_{IH}	High Level Input Voltage[2], @ V_{DDEXT} = max	2.2		V_{DDEXT} + 0.5	V
V_{IL}	Low Level Input Voltage[2], @ V_{DDEXT} = min	–0.3		+0.6	V
$V_{IHUSBCLK}$	High Level Input Voltage[3], @ V_{DDEXT} = max	2.4		V_{DDEXT} + 0.5	V
V_{IHPCI}	High Level Input Voltage[4], @ $V_{DDPCIEXT}$ = max	0.5 × $V_{DDPCIEXT}$		$V_{DDPCIEXT}$ + 0.5	V
V_{ILPCI}	Low Level Input Voltage[4], @ $V_{DDPCIINT}$ = min	–0.5		+0.3 × $V_{DDPCIEXT}$	V
T_A	Ambient Operating Temperature				°C
	Commercial	0		70	°C
	Industrial	–40		+85	°C

Specifications subject to change without notice.

[1] There is no requirement for sequencing of the voltage supplies on powerup, however, the supply regulators must be able to provide the required current $I_{DDRESET}$ at all times. See Table 26.
[2] Applies to input and bidirectional pins, except PCI and USB_CLK.
[3] Applies to USB_CLK.
[4] Applies to PCI input and bidirectional pins: PCI_AD31–0, $\overline{\text{PCI\_CBE3–0}}$, $\overline{\text{PCI\_FRAME}}$, $\overline{\text{PCI\_IRDY}}$, $\overline{\text{PCI\_TRDY}}$, $\overline{\text{PCI\_DEVSEL}}$, $\overline{\text{PCI\_STOP}}$, $\overline{\text{PCI\_PERR}}$, $\overline{\text{PCI\_PAR}}$, $\overline{\text{PCI\_SERR}}$, $\overline{\text{PCI\_RST}}$, $\overline{\text{PCI\_GNT}}$, PCI_IDSEL, $\overline{\text{PCI\_LOCK}}$, PCI_CLK, $\overline{\text{PCI\_INTA}}$, $\overline{\text{PCI\_INTB}}$, $\overline{\text{PCI\_INTC}}$, $\overline{\text{PCI\_INTD}}$.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = min, I_{OH} = –0.5 mA	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = max, I_{OL} = 2.0 mA		0.4	V
V_{OHPCI}	PCI High Level Output Voltage[2]	@ $V_{DDPCIEXT}$ = min, I_{OH} = –0.5 mA	0.9 × $V_{DDPCIEXT}$		V
V_{OLPCI}	PCI Low Level Output Voltage[2]	@ $V_{DDPCIEXT}$ = max, I_{OL} = 2.0 mA		0.1 × $V_{DDPCIEXT}$	V
I_{IH}	High Level Input Current[3]	@ V_{DDEXT} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Three-State Leakage Current[4]	@ V_{DDEXT} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Three-State Leakage Current[4]	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
C_{IN}	Input Capacitance[5, 6]	f_{IN} = 1 MHz, T_A = 25°C, V_{IN} = 2.5 V		5	pF

Specifications subject to change without notice.

[1] Applies to output and bidirectional pins, except PCI.
[2] Applies to PCI output and bidirectional pins: PCI_AD31–0, $\overline{\text{PCI\_CBE3–0}}$, $\overline{\text{PCI\_FRAME}}$, $\overline{\text{PCI\_IRDY}}$, $\overline{\text{PCI\_TRDY}}$, $\overline{\text{PCI\_DEVSEL}}$, $\overline{\text{PCI\_STOP}}$, $\overline{\text{PCI\_PERR}}$, PCI_PAR, $\overline{\text{PCI\_REQ}}$, $\overline{\text{PCI\_SERR}}$, $\overline{\text{PCI\_RST}}$, $\overline{\text{PCI\_INTA}}$.
[3] Applies to input pins.
[4] Applies to three-statable pins.
[5] Applies to all signal pins.
[6] Guaranteed but not tested.

TIMING SPECIFICATIONS

Table 9 and Table 10 describe the timing requirements for the ADSP-BF535 Blackfin processor clocks. Take care in selecting MSEL and SSEL ratios so as not to exceed the maximum core clock, system clock and Voltage Controlled Oscillator (VCO) operating frequencies, as described in Absolute Maximum Ratings on Page 22. Table 10 describes phase-locked loop operating conditions.

Table 9. Core Clock Requirements

Parameter		Min	Max	Unit
$t_{CCLK1.6}$	Core Cycle Period (V_{DDINT} = 1.6 V–50 mV)	2.86	200	ns
$t_{CCLK1.5}$	Core Cycle Period (V_{DDINT} = 1.5 V–5%)	3.33	200	ns
$t_{CCLK1.4}$	Core Cycle Period (V_{DDINT} = 1.4 V–5%)	3.70	200	ns
$t_{CCLK1.3}$	Core Cycle Period (V_{DDINT} = 1.3 V–5%)	4.17	200	ns
$t_{CCLK1.2}$	Core Cycle Period (V_{DDINT} = 1.2 V–5%)	4.76	200	ns
$t_{CCLK1.1}$	Core Cycle Period (V_{DDINT} = 1.1 V–5%)	5.56	200	ns
$t_{CCLK1.0}$	Core Cycle Period (V_{DDINT} = 1.0 V–5%)	6.67	200	ns

Table 10. Phase-Locked Loop Operating Conditions

Parameter	Min	Nominal	Max	Unit
Operating Voltage	1.425	1.5	1.575	V
Jitter, Rising Edge to Rising Edge, Per Output[1]			120	ps
Jitter, Rising Edge to Falling Edge, Per Output[1]			60	ps
Skew, Rising Edge to Rising Edge, Any Two Outputs[1]			120	ps
Voltage Controlled Oscillator (VCO) Frequency[1]	40		400	MHz
V_{DDPLL} Induced Jitter[1]			1	ps/mV

[1] Guaranteed but not tested.

Clock and Reset Timing

Table 11 and Figure 8 describe clock and reset operations. Per ABSOLUTE MAXIMUM RATINGS on Page 22, combinations of CLKIN and clock multipliers must not select core and system clocks in excess of 350/300/200 MHz and 133 MHz, respectively.

Table 11. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse[1]	10.0		ns
t_{CKINH}	CLKIN High Pulse[1]	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[2]	$11 \times t_{CKIN}$		ns
t_{MSD}	Delay from $\overline{\text{RESET}}$ Asserted to MSELx, SSELx, BYPASS, and DF Valid[3]		15.0	ns
t_{MSS}	MSELx/SSELx/DF/BYPASS Stable Setup Before $\overline{\text{RESET}}$ Deasserted[4]	$2 \times t_{CKIN}$		ns
t_{MSH}	MSELx/SSELx/DF/BYPASS Stable Hold After $\overline{\text{RESET}}$ Deasserted	$2 \times t_{CKIN}$		ns
Switching Characteristics				
t_{PFD}	Flag Output Disable Time After $\overline{\text{RESET}}$ Asserted		15.0	ns

[1] Applies to Bypass mode and Non-bypass mode.
[2] Applies after power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles, while $\overline{\text{RESET}}$ is asserted, assuming stable power supplies and CLKIN (not including start-up time of external clock oscillator).
[3] SSELx, MSELx and DF values can change from this point, but the values must be valid.
[4] SSELx, MSELx and DF values must be held from this time, until the hold time expires.

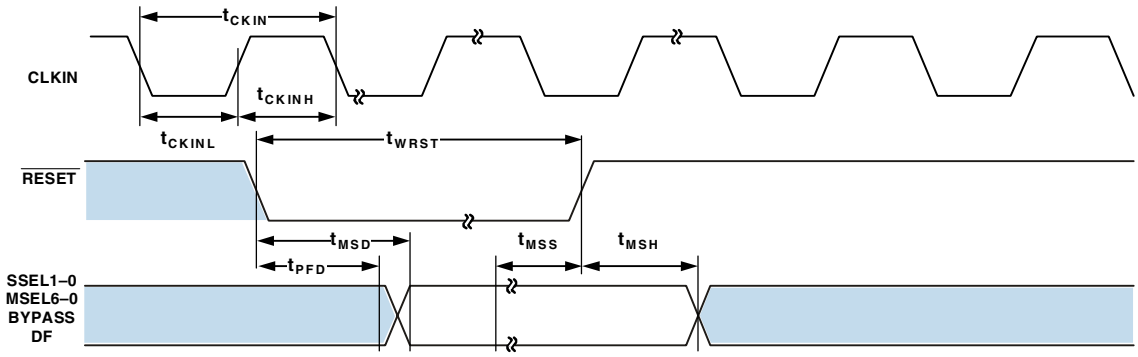

Figure 8. Clock and Reset Timing

Timer PWM_OUT Cycle Timing

Table 13 and Figure 10 describe timer expired operations. The input signal is asynchronous in "width capture mode" and has an absolute maximum input frequency of $f_{SCLK} \div 2$.

Table 13. Timer PWM_OUT Cycle Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output[1]	7.5	$(2^{32}–1)$ cycles	ns

[1] The minimum time for t_{HTO} is one cycle, and the maximum time for t_{HTO} equals $(2^{32}–1)$ cycles.

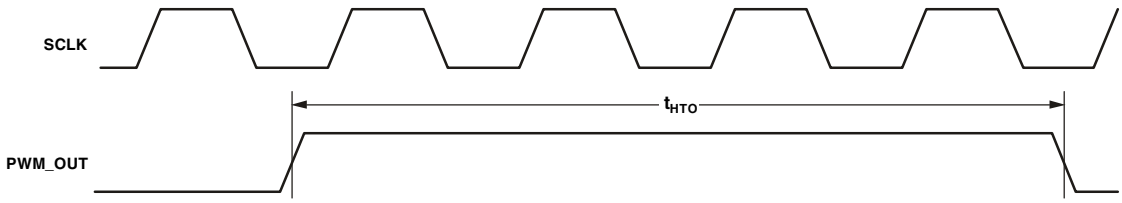

Figure 10. Timer PWM_OUT Cycle Timing

Asynchronous Memory Read Cycle Timing

Table 15 and Figure 12 describe Asynchronous Memory Read Cycle timing.

Table 15. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA31–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA31–0 Hold After CLKOUT	2.6		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	–1.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		7.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3–0}$, $\overline{ABE3–0}$, ADDR25–2, $\overline{AOE}$, $\overline{ARE}$.

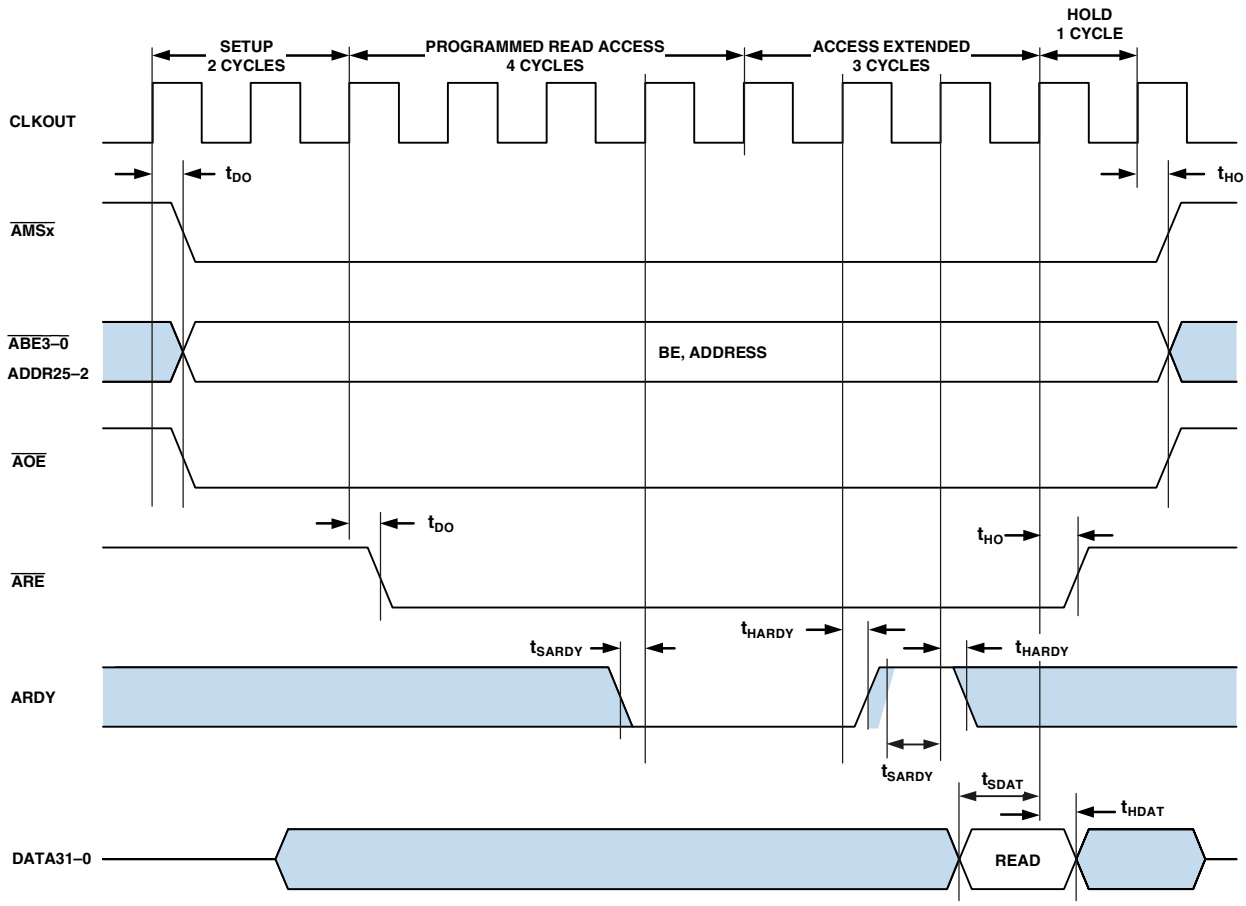

Figure 12. Asynchronous Memory Read Cycle Timing

Serial Peripheral Interface (SPI) Port —Master Timing

Table 23 and Figure 15 describe SPI port master operations.

Table 23. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	6.5		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{\text{SPIxSEL}}$ Low to First SCK Edge (x=0 or 1)	$(2 \times t_{SCLK}) - 3$		ns
t_{SPICHM}	Serial Clock High Period	$(2 \times t_{SCLK}) - 3$		ns
t_{SPICLM}	Serial Clock Low Period	$(2 \times t_{SCLK}) - 3$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDSM}	Last SCK Edge to $\overline{\text{SPIxSEL}}$ High (x=0 or 1)	$(2 \times t_{SCLK}) - 3$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK}$		ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)	0.0	6.0	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0.0	5.0	ns

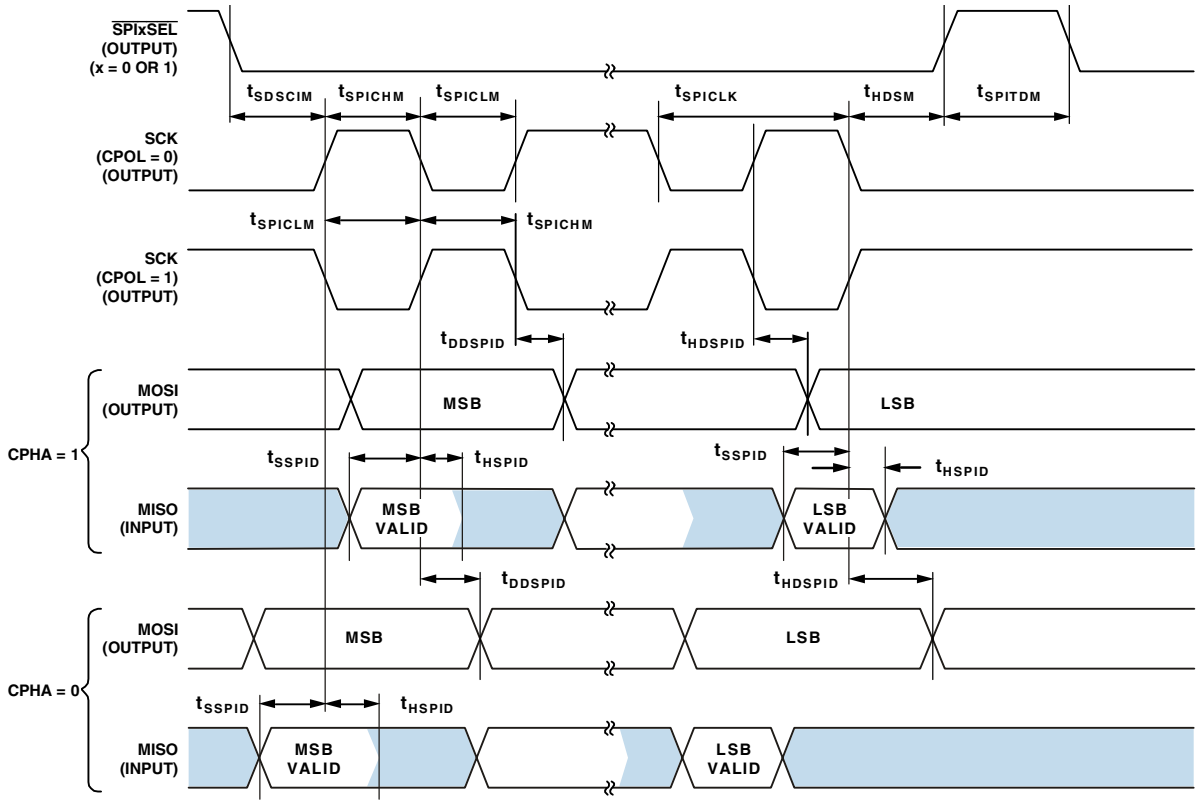

Figure 15. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port —Slave Timing

Table 24 and Figure 16 describe SPI port slave operations.

Table 24. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2t_{SCLK}$		ns
t_{SPICLS}	Serial Clock Low Period	$2t_{SCLK}$		ns
t_{SPICLK}	Serial Clock Period	$4t_{SCLK}$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPISS}$ Not Asserted	$2t_{SCLK}$		ns
t_{SPITDS}	Sequential Transfer Delay	$2t_{SCLK}$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2t_{SCLK}$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0.0	6.0	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0.0	6.5	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)	0.0	7.0	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0.0	6.5	ns

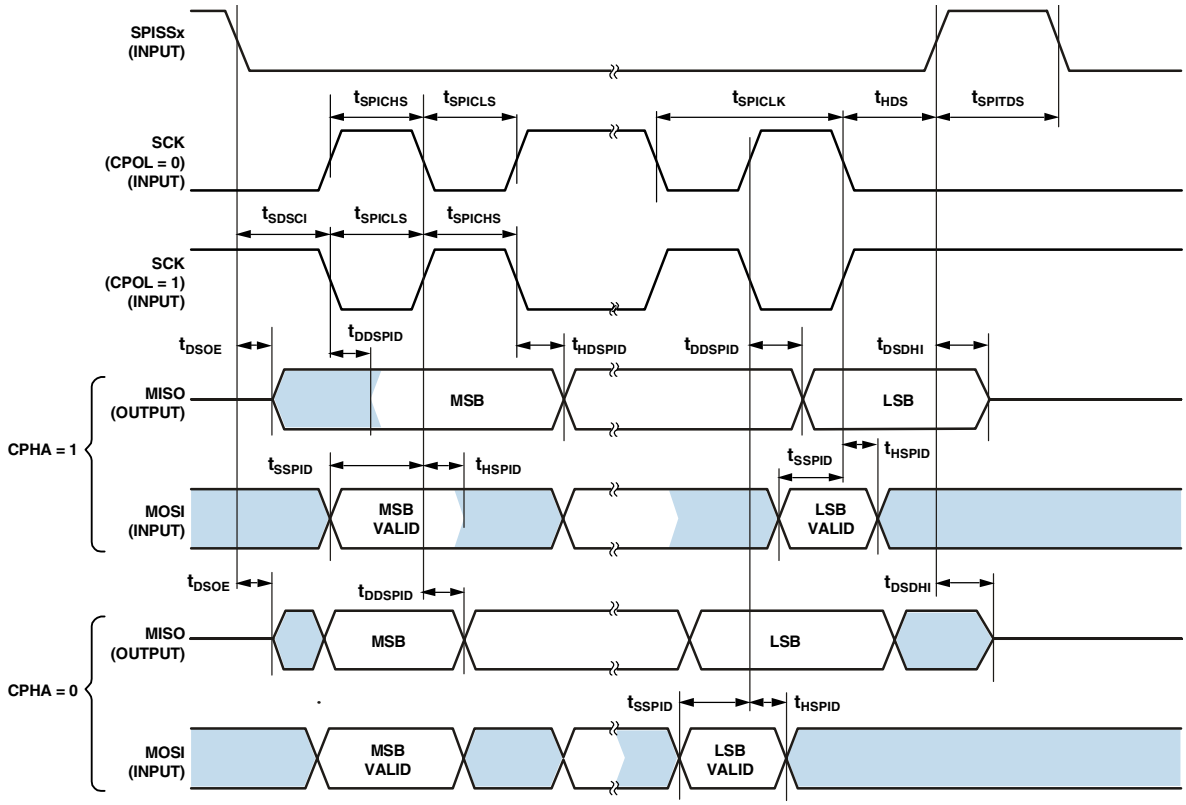

Figure 16. Serial Peripheral Interface (SPI) Port—Slave Timing

JTAG Test and Emulation Port Timing

Table 25 and Figure 18 describe JTAG port operations.

Table 25. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20.0		ns
t_{STAP}	TDI, TMS Setup Before TCK High		4.0	ns
t_{HTAP}	TDI, TMS Hold After TCK High		4.0	ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]		4.0	ns
t_{HSYS}	System Inputs Hold After TCK Low[1]		5.0	ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2]	4.0		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7.0	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0.0	15.0	ns

[1] System Inputs=DATA31-0, ADDR25-2, ARDY, TMR2-0, PF15-0, RSCLK0, RFS0, DR0, TSCLK0, TFS0, RSCLK1, RFS1, DR1, TSCLK1, TFS1, MOSI0, MISO0, SCK0, MOSI1, MISO1, SCK1, RX0, RX1, USB_CLK, XVER_DATA, DPLS, DMNS, NMI, $\overline{\text{RESET}}$, BYPASS, BMODE2-0, PCI_AD31-0, $\overline{\text{PCI\_CBE3-0}}$, $\overline{\text{PCI\_FRAME}}$, $\overline{\text{PCI\_IRDY}}$, $\overline{\text{PCI\_TRDY}}$, $\overline{\text{PCI\_DEVSEL}}$, $\overline{\text{PCI\_STOP}}$, $\overline{\text{PCI\_PERR}}$, PCI_PAR, $\overline{\text{PCI\_SERR}}$, $\overline{\text{PCI\_RST}}$, $\overline{\text{PCI\_GNT}}$, PCI_IDSEL, $\overline{\text{PCI\_LOCK}}$, PCI_CLK, $\overline{\text{PCI\_INTA}}$, $\overline{\text{PCI\_INTB}}$, $\overline{\text{PCI\_INTC}}$, $\overline{\text{PCI\_INTD}}$.

[2] 50 MHz max.

[3] System Outputs=DATA31-0, ADDR25-2, $\overline{\text{ABE3-0}}$/SDQM3-0, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{SCAS}}$, CLKOUT/SCLK1, SCLK0, SCKE, SA10, $\overline{\text{SWE}}$, $\overline{\text{SMS3-0}}$, $\overline{\text{SRAS}}$, TMR2-0, PF15-0, RSCLK0, RFS0, TSCLK0, TFS0, DT0, RSCLK1, RFS1, TSCLK1, TFS1, DT1, MOSI0, MISO0, SCK0, MOSI1, MISO1, SCK1, TX0, TX1, TXDPLS, TXDMNS, $\overline{\text{TXEN}}$, SUSPEND, DEEPSLEEP, PCI_AD31-0, $\overline{\text{PCI\_CBE3-0}}$, $\overline{\text{PCI\_FRAME}}$, $\overline{\text{PCI\_IRDY}}$, $\overline{\text{PCI\_TRDY}}$, $\overline{\text{PCI\_DEVSEL}}$, $\overline{\text{PCI\_STOP}}$, $\overline{\text{PCI\_PERR}}$, PCI_PAR, $\overline{\text{PCI\_REQ}}$, $\overline{\text{PCI\_SERR}}$, $\overline{\text{PCI\_RST}}$, $\overline{\text{PCI\_INTA}}$, $\overline{\text{EMU}}$.

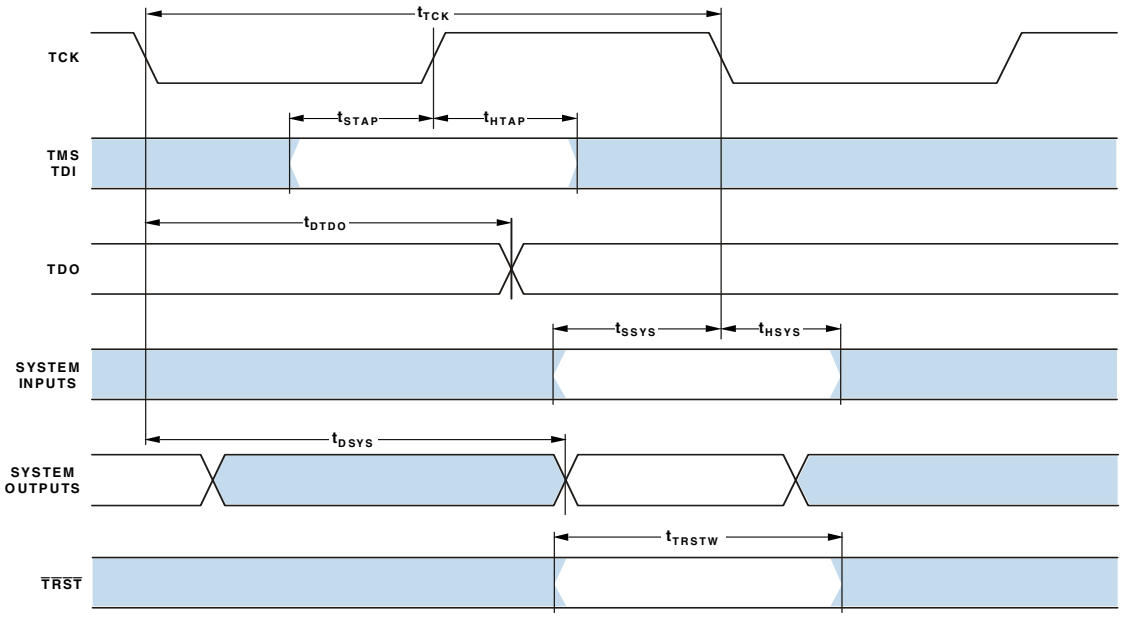

Figure 18. JTAG Port Timing

Table 27. PLL Power Dissipation

Parameter	Test Conditions	Typical	Unit
I_{DDPLL}	V_{DDPLL} = 1.5 V, 25°C	4.0	mA

The frequency f includes driving the load high and then back low. For example: DATA31–0 pins can drive high and low at a maximum rate of 1/(2 × t_{SCLK}) while in SDRAM burst mode.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DD} \times V_{DDINT})$$

Note that the conditions causing a worst-case P_{EXT} differ from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones (1s) to all zeros (0s). Note, as well, that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Test Conditions

All timing parameters appearing in this data sheet were measured under the conditions described in this section.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown in the Output Enable/Disable diagram (Figure 22). The time $t_{ENA\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage reaches 2.0 V (output high) or 1.0 V (output low). Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the 1.0 V or 2.0 V trip voltage. Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V) / I_L$$

The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown in Figure 22. The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF535 Blackfin processor's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (for example, t_{DSDAT} for an SDRAM write cycle).

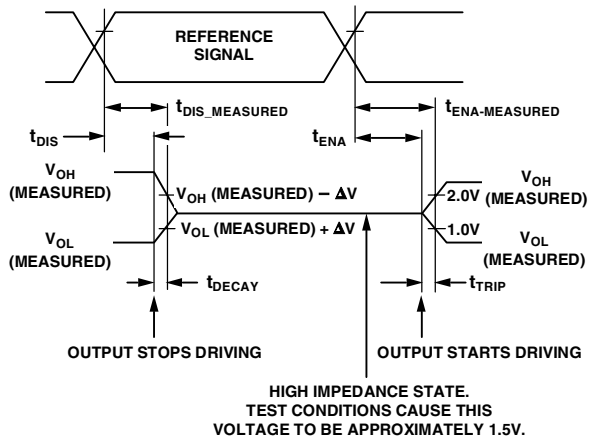

Figure 22. Output Enable/Disable

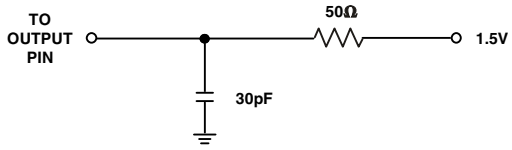

Figure 23. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

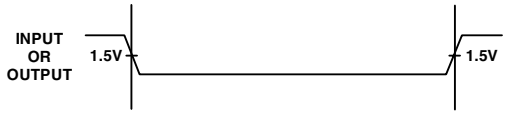

Figure 24. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

260-Ball PBGA Pinout

Table 29 lists the PBGA pinout by signal name. Table 30 on Page 41 lists the pinout by pin number.

Table 29. 260-Ball PBGA Pin Assignment (Alphabetically by Signal)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ABE0/SDQM0	E02	DATA5	R02	GND	K08	PCI_AD25	M16
ABE1/SDQM1	B01	DATA6	P03	GND	K09	PCI_AD26	N17
ABE2/SDQM2	G03	DATA7	U01	GND	K10	PCI_AD27	P17
ABE3/SDQM3	H07	DATA8	U02	GND	K11	PCI_AD28	P15
ADDR2	A06	DATA9	T02	GND	K12	PCI_AD29	N16
ADDR3	B06	DATA10	V02	GND	L07	PCI_AD30	R17
ADDR4	D06	DATA11	V03	GND	L08	PCI_AD31	P16
ADDR5	C06	DATA12	R04	GND	L09	PCI_CBE0	F16
ADDR6	A05	DATA13	U03	GND	L10	PCI_CBE1	F15
ADDR7	B05	DATA14	T03	GND	L11	PCI_CBE2	E16
ADDR8	A04	DATA15	T04	GND	M07	PCI_CBE3	D17
ADDR9	C05	DATA16	U04	GND	M09	PCI_CLK	D14
ADDR10	D05	DATA17	V04	GND	M10	PCI_DEVSEL	C16
ADDR11	B04	DATA18	V05	MISO0	T16	PCI_FRAME	C17
ADDR12	A01	DATA19	R05	MISO1	U18	PCI_GNT	C18
ADDR13	C04	DATA20	T05	MOSI0	U16	PCI_IDSEL	B18
ADDR14	D04	DATA21	U05	MOSI1	T17	PCI_INTA	C14
ADDR15	A03	DATA22	V06	N/C	A18	PCI_INTB	B15
ADDR16	B03	DATA23	R06	N/C	R03	PCI_INTC	A15
ADDR17	A02	DATA24	U06	N/C	V01	PCI_INTD	D13
ADDR18	C03	DATA25	T06	N/C	V18	PCI_IRDY	E15
ADDR19	D03	DATA26	V07	NMI	B11	PCI_LOCK	A16
ADDR20	B02	DATA27	V08	PCI_AD0	E17	PCI_PAR	C15
ADDR21	C02	DATA28	U07	PCI_AD1	E18	PCI_PERR	D15
ADDR22	E03	DATA29	R07	PCI_AD2	G16	PCI_REQ	D16
ADDR23	C01	DATA30	T07	PCI_AD3	F17	PCI_RST	D18
ADDR24	F03	DATA31	V09	PCI_AD4	F18	PCI_SERR	B16
ADDR25	D02	DMNS	D08	PCI_AD5	G18	PCI_STOP	A17
AMS0	F02	DPLS	C09	PCI_AD6	G17	PCI_TRDY	B17
AMS1	D01	DR0	V14	PCI_AD7	H18	PF0/SPISS0/MSEL0	U08
AMS2	H03	DR1	U15	PCI_AD8	J18	PF1/SPISS1/MSEL1	R08
AMS3	G02	DT0	R14	PCI_AD9	H17	PF2/SPI0SEL1/MSEL2	T08
AOE	E01	DT1	V17	PCI_AD10	K18	PF3/SPI1SEL1/MSEL3	V10
ARDY	R01	EMU	A13	PCI_AD11	H16	PF4/SPI0SEL2/MSEL4	U09
ARE	F01	GND	C13	PCI_AD12	L18	PF5/SPI1SEL2/MSEL5	R09
AWE	G01	GND	H02	PCI_AD13	J17	PF6/SPI0SEL3/MSEL6	T09
BMODE0	B14	GND	H08	PCI_AD14	M18	PF7/SPI1SEL3/DF	R11
BMODE1	A14	GND	H10	PCI_AD15	K17	PF8/SPI0SEL4/SSEL0	T11
BMODE2	B13	GND	H11	PCI_AD16	J16	PF9/SPI1SEL4/SSEL1	U11
BYPASS	C12	GND	J07	PCI_AD17	K16	PF10/SPI0SEL5	V12
CLKIN1	D09	GND	J08	PCI_AD18	N18	PF11/SPI1SEL5	T12
CLKOUT/SCLK1	H01	GND	J09	PCI_AD19	P18	PF12/SPI0SEL6	R12
DATA0	N02	GND	J10	PCI_AD20	L17	PF13/SPI1SEL6	U12
DATA1	M03	GND	J11	PCI_AD21	L16	PF14/SPI0SEL7	V13
DATA2	T01	GND	J12	PCI_AD22	R18	PF15/SPI1SEL7	T13
DATA3	P02	GND	K02	PCI_AD23	T18	RESET	B09
DATA4	N03	GND	K07	PCI_AD24	M17	RFS0	U13

Table 30. 260-Ball PBGA Pin Assignment (Numerically by Pin Number)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	ADDR12	D12	DEEPSLEEP	K01	SCLK0	R08	PF1/$\overline{\text{SPISS1}}$/MSEL1
A02	ADDR17	D13	$\overline{\text{PCI\_INTD}}$	K02	GND	R09	PF5/$\overline{\text{SPI1SEL2}}$/MSEL5
A03	ADDR15	D14	PCI_CLK	K03	$\overline{\text{SMS3}}$	R10	XTAL1
A04	ADDR8	D15	$\overline{\text{PCI\_PERR}}$	K04	V_{DDEXT}	R11	PF7/$\overline{\text{SPI1SEL3}}$/DF
A05	ADDR6	D16	$\overline{\text{PCI\_REQ}}$	K07	GND	R12	PF12/$\overline{\text{SPI0SEL6}}$
A06	ADDR2	D17	$\overline{\text{PCI\_CBE3}}$	K08	GND	R13	RSCLK0
A07	RX0	D18	$\overline{\text{PCI\_RST}}$	K09	GND	R14	DT0
A08	TX0	E01	$\overline{\text{AOE}}$	K10	GND	R15	TFS1
A09	XVER_DATA	E02	$\overline{\text{ABE0}}$/SDQM0	K11	GND	R16	SCK1
A10	V_{SSPLL}	E03	ADDR22	K12	GND	R17	PCI_AD30
A11	SUSPEND	E04	V_{DDEXT}	K15	$V_{DDPCIEXT}$	R18	PCI_AD22
A12	TMS	E15	$\overline{\text{PCI\_IRDY}}$	K16	PCI_AD17	T01	DATA2
A13	$\overline{\text{EMU}}$	E16	$\overline{\text{PCI\_CBE2}}$	K17	PCI_AD15	T02	DATA9
A14	BMODE1	E17	PCI_AD0	K18	PCI_AD10	T03	DATA14
A15	$\overline{\text{PCI\_INTC}}$	E18	PCI_AD1	L01	SCKE	T04	DATA15
A16	$\overline{\text{PCI\_LOCK}}$	F01	$\overline{\text{ARE}}$	L02	$\overline{\text{SRAS}}$	T05	DATA20
A17	$\overline{\text{PCI\_STOP}}$	F02	$\overline{\text{AMS0}}$	L03	$\overline{\text{SCAS}}$	T06	DATA25
A18	N/C	F03	ADDR24	L04	V_{DDEXT}	T07	DATA30
B01	$\overline{\text{ABE1}}$/SDQM1	F04	V_{DDINT}	L07	GND	T08	PF2/$\overline{\text{SPI0SEL1}}$/MSEL2
B02	ADDR20	F15	$\overline{\text{PCI\_CBE1}}$	L08	GND	T09	PF6/$\overline{\text{SPI0SEL3}}$/MSEL6
B03	ADDR16	F16	$\overline{\text{PCI\_CBE0}}$	L09	GND	T10	XTAL0
B04	ADDR11	F17	PCI_AD3	L10	GND	T11	PF8/$\overline{\text{SPI0SEL4}}$/SSEL0
B05	ADDR7	F18	PCI_AD4	L11	GND	T12	PF11/$\overline{\text{SPI1SEL5}}$
B06	ADDR3	G01	$\overline{\text{AWE}}$	L12	V_{DDINT}	T13	PF15/$\overline{\text{SPI1SEL7}}$
B07	TMR0	G02	$\overline{\text{AMS3}}$	L15	$V_{DDPCIEXT}$	T14	TFS0
B08	RX1	G03	$\overline{\text{ABE2}}$/SDQM2	L16	PCI_AD21	T15	TSCLK1
B09	$\overline{\text{RESET}}$	G04	V_{DDEXT}	L17	PCI_AD20	T16	MISO0
B10	TXDPLS	G07	USB_CLK	L18	PCI_AD12	T17	MOSI1
B11	NMI	G08	V_{DDEXT}	M01	SA10	T18	PCI_AD23
B12	$\overline{\text{TRST}}$	G09	V_{DDPLL}	M02	$\overline{\text{SMS0}}$	U01	DATA7
B13	BMODE2	G10	TXDMNS	M03	DATA1	U02	DATA8
B14	BMODE0	G11	V_{DDINT}	M04	V_{DDEXT}	U03	DATA13
B15	$\overline{\text{PCI\_INTB}}$	G12	V_{DDINT}	M07	GND	U04	DATA16
B16	$\overline{\text{PCI\_SERR}}$	G15	V_{DDINT}	M08	V_{DDINT}	U05	DATA21
B17	$\overline{\text{PCI\_TRDY}}$	G16	PCI_AD2	M09	GND	U06	DATA24
B18	PCI_IDSEL	G17	PCI_AD6	M10	GND	U07	DATA28
C01	ADDR23	G18	PCI_AD5	M11	V_{DDINT}	U08	PF0/$\overline{\text{SPISS0}}$/MSEL0
C02	ADDR21	H01	CLKOUT/SCLK1	M12	V_{DDINT}	U09	PF4/$\overline{\text{SPI0SEL2}}$/MSEL4
C03	ADDR18	H02	GND	M15	$V_{DDPCIEXT}$	U10	V_{DDRTC}
C04	ADDR13	H03	$\overline{\text{AMS2}}$	M16	PCI_AD25	U11	PF9/$\overline{\text{SPI1SEL4}}$/SSEL1
C05	ADDR9	H04	V_{DDINT}	M17	PCI_AD24	U12	PF13/$\overline{\text{SPI1SEL6}}$
C06	ADDR5	H07	$\overline{\text{ABE3}}$/SDQM3	M18	PCI_AD14	U13	RFS0
C07	TMR1	H08	GND	N01	$\overline{\text{SMS2}}$	U14	RSCLK1
C08	TX1	H09	V_{DDINT}	N02	DATA0	U15	DR1
C09	DPLS	H10	GND	N03	DATA4	U16	MOSI0
C10	$\overline{\text{TXEN}}$	H11	GND	N04	V_{DDINT}	U17	SCK0
C11	TDI	H12	V_{DDINT}	N15	V_{DDINT}	U18	MISO1
C12	BYPASS	H15	$V_{DDPCIEXT}$	N16	PCI_AD29	V01	N/C
C13	GND	H16	PCI_AD11	N17	PCI_AD26	V02	DATA10

OUTLINE DIMENSIONS

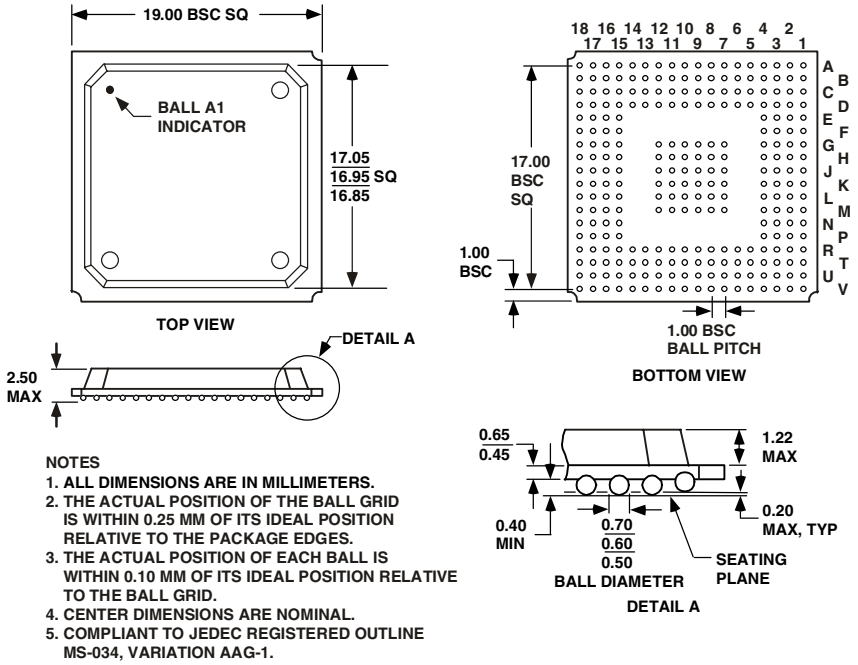

Figure 27. 260-Ball Metric Plastic Ball Grid Array (PBGA) (B-260)

ORDERING GUIDE

Part Number	Temperature Range (Ambient)	Instruction Rate	Operating Voltage (V)
ADSP-BF535PKB-350	0°C to +70°C	350 MHz	1.0 V to 1.6 V internal, 3.3 V I/O
ADSP-BF535PKB-300	0°C to +70°C	300 MHz	1.0 V to 1.5 V internal, 3.3 V I/O
ADSP-BF535PBB-300	–40°C to +85°C	300 MHz	1.0 V to 1.5 V internal, 3.3 V I/O
ADSP-BF535PBB-200	–40°C to +85°C	200 MHz	1.0 V to 1.5 V internal, 3.3 V I/O

Revision History

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