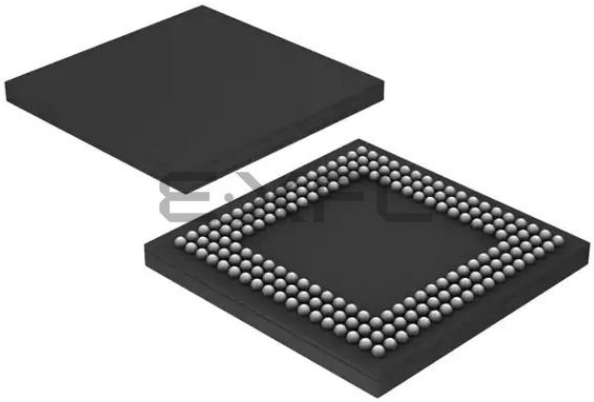

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, UART/USART, USB
Peripherals	DMA, I²S, LCD, WDT
Number of I/O	85
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 5x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2880fet180-551

Table 3. Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
13	-	14	-	15	-	16	A3/P0[19]
17	A4/P0[20]	18	A5/P0[21]		-		-
Row E							
1	$V_{DD1(IO3V3)}$	2	LD6/P4[10]	3	LD7/P4[11]	4	-
13	-	14	-	15	-	16	A0/P0[16]
17	A1/P0[17]	18	A2/P0[18]		-		-
Row F							
1	$V_{SS1(IO)}$	2	LER/P4[3]	3	LRS/P4[1]	4	-
13	-	14	-	15	-	16	DCLKO/P3[3]
17	DATO/P3[6]	18	WSO		-		-
Row G							
1	$V_{SS1(CORE)}$	2	LRW/P4[2]	3	MCLK/P5[0]	4	-
13	-	14	-	15	-	16	DATI/P3[0]
17	WSI/P3[2]	18	BCKO/P3[5]		-		-
Row H							
1	$V_{DD1(CORE1V8)}$	2	MCMD/P5[1]	3	MD0/P5[5]	4	-
13	-	14	-	15	-	16	SCL
17	BCKI/P3[1]	18	$V_{SS4(IO)}$		-		-
Row J							
1	MD2/P5[3]	2	MD1/P5[4]	3	MD3/P5[2]	4	-
13	-	14	-	15	-	16	MODE2/P2[3]
17	SDA	18	$V_{DD4(IO3V3)}$		-		-
Row K							
1	$\overline{RTS}$/P6[3]	2	$\overline{CTS}$/P6[2]	3	RXD/P6[0]	4	-
13	-	14	-	15	-	16	P2[0]
17	P2[1]	18	MODE1/P2[2]		-		-
Row L							
1	$V_{DD(DAC3V3)}$	2	VREFP(DAC)	3	TXD/P6[1]	4	-
13	-	14	-	15	-	16	DCDC_GND
17	START	18	STOP		-		-
Row M							
1	VREFN(DAC)	2	AOUTL	3	AOUTR	4	-
13	-	14	-	15	-	16	$DCDC\_V_{DDI(3V3)}$
17	$DCDC\_V_{BAT}$	18	DCDC_CLEAN		-		-
Row N							
1	i.c.[1]	2	i.c.[1]	3	i.c.[1]	4	-
13	-	14	-	15	-	16	$DCDC\_V_{SS2}$
17	DCDC_LX2	18	$DCDC\_V_{DDO(1V8)}$		-		-
Row P							
1	$V_{SS6(IO)}$	2	$V_{SS5(IO)}$	3	i.c.[1]	4	-
13	-	14	-	15	-	16	RREF

Table 4. Pin description *...continued*

Symbol	Ball #	Type[1]	Description
CKE/P1[9]	B10	FO	clock enable; active HIGH for SDRAM; GPIO pin
DQM0/P1[10]	C12	FO	data mask output for D[7:0], active HIGH for SDRAM; GPIO pin
DQM1/P1[11]	A11	FO	data mask output for D[15:8], active HIGH for SDRAM; GPIO pin
$\overline{\text{DYCS}}$/P1[8]	B9	FO	chip select, active LOW for SDRAM; GPIO pin
MCLKO/P1[14]	A10	FO	clock for SDRAM and SyncFlash memory; GPIO pin
$\overline{\text{OE}}$/P1[18]	A17	FO	output enable, active LOW for static memory; GPIO pin
$\overline{\text{RAS}}$/P1[17]	A9	FO	row address strobe, active LOW for SDRAM; GPIO pin
$\overline{\text{RPO}}$/P1[19]	B1	FO	reset power-down, active LOW for SyncFlash memory; GPIO pin
$\overline{\text{STCS0}}$/P1[5]	C9	FO	chip select, active LOW for static memory bank 0; GPIO pin
$\overline{\text{STCS1}}$/P1[6]	A8	FO	chip select, active LOW for static memory bank 1; GPIO pin
$\overline{\text{STCS2}}$/P1[7]	B11	FO	chip select, active LOW for static memory bank 2; GPIO pin
$\overline{\text{WE}}$/P1[15]	C11	FO	write enable, active LOW for SDRAM and static memory; GPIO pin
GPIO and mode control			
MODE1/P2[2]	K18	FI	start-up mode pin 1 (pull-down); 5 V tolerant GPIO pin
MODE2/P2[3]	J16	FI	start-up mode pin 2 (pull-down); 5 V tolerant GPIO pin
P2[0]	K16	FI	5 V tolerant GPIO pin
P2[1]	K17	FI	5 V tolerant GPIO pin
I^2C-bus interface			
SCL	H16	I/O	serial clock (input/open-drain output); 5 V tolerant pin
SDA	J17	I/O	serial data (input/open-drain output); 5 V tolerant pin
JTAG interface			
JTAG_SEL	U4	I	JTAG selection (pull-down); 5 V tolerant pin
JTAG_TCK	V4	I	JTAG reset input (pull-down); 5 V tolerant pin
JTAG_TDI	T5	I	JTAG data input (pull-up); 5 V tolerant pin
JTAG_TMS	U12	I	JTAG mode select input (pull-up); 5 V tolerant pin
$\overline{\text{JTAG\_TRST}}$	T13	I	JTAG reset input (pull-down); 5 V tolerant pin
JTAG_TDO	U13	O	JTAG data output; 5 V tolerant pin
LCD interface			
LCS/P4[0]	B3	FO	chip select to LCD device, programmable polarity; 5 V tolerant GPIO pin
LD0/P4[4]	C2	FO	data bus to/from LCD (I/O) or 5 V tolerant GPIO pins
LD1/P4[5]	C1	FO	
LD2/P4[6]	C3	FO	
LD3/P4[7]	D2	FO	
LD4/P4[8]	D1	FO	
LD5/P4[9]	D3	FO	
LD6/P4[10]	E2	FO	
LD7/P4[11]	E3	FO	
LER/P4[3]	F2	FO	6800 E or 8080 $\overline{\text{RD}}$ or 5 V tolerant GPIO pin
LRS/P4[1]	F3	FO	'HIGH' data register select, 'LOW' instruction register select, or 5 V tolerant GPIO pin
LRW/P4[2]	G2	FO	6800 W/$\overline{\text{R}}$ or 8080 $\overline{\text{WR}}$ or 5 V tolerant GPIO pin

Table 4. Pin description *...continued*

Symbol	Ball #	Type[1]	Description
Memory card interface			
MCMD/P5[1]	H2	FI	command (I/O); 5 V tolerant GPIO pin
MD0/P5[5]	H3	FI	data bus from/to SD/MCI card (I/O); 5 V tolerant GPIO pin
MD1/P5[4]	J2	FI	data bus from/to SD/MCI card (I/O); 5 V tolerant GPIO pin
MD2/P5[3]	J1	FI	data bus from/to SD/MCI card (I/O); 5 V tolerant GPIO pin
MD3/P5[2]	J3	FI	data bus from/to SD/MCI card (I/O); 5 V tolerant GPIO pin
MCLK/P5[0]	G3	FO	MCI clock output; 5 V tolerant GPIO pin
Oscillator (32.768 kHz)			
X32I	V7	I	32.768 kHz oscillator input
X32O	T8	O	32.768 kHz oscillator output
$V_{DD(OSC321V8)}$	U8	P	1.8 V
$V_{SS(OSC32)}$	V8	P	ground
Oscillator (main)			
XTALI	T10	I	main oscillator input
XTALO	V9	O	main oscillator output
$V_{DD(OSC1V8)}$	U9	P	1.8 V
$V_{SS(OSC)}$	T9	P	ground
Reset			
$\overline{RESET}$	T14	I	master reset, active LOW; 5 V tolerant pin
UART			
$\overline{CTS}$/P6[2]	K2	FI	clear to send or transmit flow control, active LOW; 5 V tolerant GPIO pin
RXD/P6[0]	K3	FI	serial input; 5 V tolerant GPIO pin
$\overline{RTS}$/P6[3]	K1	FO	request to send or receive flow control, active LOW; 5 V tolerant GPIO pin
TXD/P6[1]	L3	FO	serial output; 5 V tolerant GPIO pin
USB interface			
CONNECT	T15	P	used for signalling speed capability; for high-speed USB, connect an external 1.5 kΩ resistor to 3.3 V
DM	T17	I/O	negative USB data line
DP	U17	I/O	positive USB data line
RREF	P16	P	transceiver reference; connect an external 12 kΩ 1 % resistor to ground
VBUS/P7[0]	U14	FI	USB supply detection; 5 V tolerant GPIO pin
$V_{DD1(USB1V8)}$	U15	P	analog 1.8 V
$V_{DD2(USB1V8)}$	U16	P	analog 1.8 V
$V_{DD3(USB3V3)}$	U18	P	analog 3.3 V
$V_{DD4(USB3V3)}$	V18	P	analog 3.3 V
$V_{SS1(USB)}$	R17	P	analog ground
$V_{SS2(USB)}$	R16	P	analog ground
$V_{SS3(USB)}$	T16	P	analog ground

Table 4. Pin description *...continued*

Symbol	Ball #	Type[1]	Description
Digital power and ground			
$V_{DD1(CORE1V8)}$	H1	P	1.8 V for internal RAM and ROM
$V_{DD1(FLASH1V8)}$	V15	P	1.8 V for internal flash memory
$V_{DD1(EMC)}$	A16	P	1.8 V or 3.3 V for external memory controller
$V_{DD1(IO3V3)}$	E1	P	3.3 V for peripherals
$V_{DD2(CORE1V8)}$	V11	P	1.8 V for core
$V_{DD2(EMC)}$	A7	P	1.8 V or 3.3 V for external memory controller
$V_{DD2(FLASH1V8)}$	V16	P	1.8 V for internal flash memory
$V_{DD2(IO3V3)}$	V5	P	3.3 V for peripherals
$V_{DD3(IO3V3)}$	V14	P	3.3 V for peripherals
$V_{DD4(IO3V3)}$	J18	P	3.3 V for peripherals
$V_{DD5(IO3V3)}$	R1	P	3.3 V for peripherals
$V_{DD6(IO3V3)}$	R2	P	3.3 V for peripherals
$V_{SS1(CORE)}$	G1	P	ground for internal RAM and ROM
$V_{SS1(EMC)}$	A15	P	ground for external memory controller
$V_{SS1(INT)}$	T12	P	ground for other internal blocks
$V_{SS1(IO)}$	F1	P	ground for peripherals
$V_{SS2(CORE)}$	V12	P	ground for core
$V_{SS2(EMC)}$	A6	P	ground for external memory controller
$V_{SS2(INT)}$	U11	P	ground for other internal blocks
$V_{SS2(IO)}$	V6	P	ground for peripherals
$V_{SS3(CORE)}$	V17	P	ground for core, substrate, flash
$V_{SS3(INT)}$	T11	P	ground for other internal blocks
$V_{SS3(IO)}$	V13	P	ground for peripherals
$V_{SS4(IO)}$	H18	P	ground for peripherals
$V_{SS5(IO)}$	P2	P	ground for peripherals
$V_{SS6(IO)}$	P1	P	ground for peripherals

[1] I = input; O = output; I/O = input/output; RV = reference voltage; FI = functional input; FO = functional output; P = power or ground

6. Functional description

6.1 Architectural overview

The LPC2880/2888 includes an ARM7TDMI CPU with an 8 kB cache, an AMBA AHB interfacing to high-speed on-chip peripherals and internal and external memory, and four AMBA APBs for connection to other on-chip peripheral functions.

The LPC2880/2888 includes a multi-layer AHB and four separate APBs, in order to minimize interference between the USB controller, other DMA operations, and processor activity. Bus masters include the ARM7 itself, the USB block, and the general purpose DMA controller.

The boot code in this ROM reads the state of the mode inputs and accordingly does one of the following:

- Starts execution in internal flash
- Starts execution in external memory
- Performs a hardware self-test, or
- Downloads code from the USB interface into on-chip RAM and transfers control to the downloaded code

6.2 Memory map

The LPC2880/2888 memory map incorporates several distinct regions, as shown in Figure 3. When an application is running, the CPU interrupt vectors are remapped to allow them to reside in on-chip SRAM.

6.9 Event router

88 external and 11 internal LPC2880/2888 signals are connected to the Event Router block. GPIO input pins, functional input pins, and even functional outputs can be monitored by the Event Router.

Each signal can act as an interrupt source or a clock-enable for LPC2880/2888 modules, with individual options for high- or low-level sensitivity or rising- or falling-edge sensitivity. The outputs of the polarity and sensitivity logic can be read from Raw Status Registers 0 to 3.

Each active state is next masked/enabled by a “global” mask bit for that signal. The results can be read from Pending Registers 0 to 3.

All 99 Pending signals are presented to each of the five output logic blocks. Each output logic block includes a set of four Interrupt Output Mask Registers, each set totalling 99 bits, that control whether each signal applies to that output. These are logically ANDed with the corresponding Pending signals, and the 99 results in each logic block are logically ORed to make the output of the block. The 496 results can be read in the Interrupt Output Pending Registers.

Outputs 0 to 3 are routed to the Interrupt Controller, in which each can be individually enabled to cause an interrupt. Output 4 is routed to the Clock Generation Unit, in which it can serve to enable clocking for selected clock domains. The five outputs can be read in the Output Register.

6.10 General purpose timers

The LPC2880/2888 contains two fully independent general purpose timers. Each timer is a 32 bit wide down counter with a selectable prescaler. The prescaler allows either the system clock to be used directly, or the clock to be divided by 16 or 256.

Two modes of operation are available, free-running and periodic timer. In periodic timer mode, the counter will generate an interrupt at a constant interval. In free-running mode the timer will overflow after reaching its zero value and continue to count down from the maximum value.

6.10.1 Features

- Two independent 32-bit timers.
- Free-running or periodic operating modes.
- Generate timed interrupts.

6.11 Watchdog timer

The purpose of the watchdog timer is to interrupt and/or reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate an interrupt or a system reset if the user program fails to reset the watchdog within a predetermined amount of time. Alternatively, it can be used as an additional general purpose Timer.

- The GPDMA supports a subset of the flow control signals supported by ARM DMA channels, specifically ‘single’ but not ‘burst’ operation.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Rotating channel priority. Each DMA channel has equal opportunity to perform transfers.
- The GPDMA is one of three AHB masters in the LPC2880/2888, the others being the ARM7 processor and the USB interface.
- Incrementing or non-incrementing addressing for source and destination.
- Supports 8 bit, 16 bit, and 32 bit wide transactions.
- GPDMA channels can be programmed to swap data between big- and little-endian formats during a transfer.
- An interrupt to the processor can be generated on DMA completion, when a DMA channel is halfway to completion, or when a DMA error has occurred.

6.14 UART and IrDA

The LPC2880/2888 contains one UART with baud rate generator and IrDA support.

6.14.1 Features

- 32-Byte Receive and Transmit FIFOs.
- Register locations conform to the 16C650 industry standard.
- Receiver FIFO trigger points at 1 B, 16 B, 24 B, and 28 B.
- Built-in baud rate generator.
- CGU generates UART clock including fractional divider capability.
- Auto baud capability.
- Optional hardware flow control.
- IrDA mode for infrared communication.

6.15 I^2C-bus interface

The LPC2880/2888 I^2C-bus interface is byte oriented and has four operating modes: master Transmit mode, master Receive mode, slave Transmit mode and slave Receive mode. The interface complies with the entire *I^2C-bus specification*, and allows turning power off to the LPC2880/2888 without causing a problem with other devices on the same I^2C-bus.

6.15.1 Features

- Standard I^2C-bus interface, configurable as Master, Slave, or Master/Slave.
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock allows adjustment of I^2C-bus transfer rates.
- Bidirectional data transfer between masters and slaves.

6.21.6 APBs

Most peripheral functions are accessed by on-chip APBs that are attached to the higher speed AHB. The APBs perform reads and writes to peripheral registers in three peripheral clocks.

6.22 Emulation and debugging

The LPC2880/2888 supports emulation via a dedicated JTAG serial port. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. The EmbeddedICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)			–0.5	+1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)			–0.5	+4.6	V
$V_{DD(EMC)}$	external memory controller supply voltage	in 1.8 V range		–0.5	+1.95	V
		in 3.3 V range		–0.5	+3.6	V
V_{IA}	analog input voltage			–0.5	$V_{DD(ADC3V3)}$	V
V_I	input voltage	5 V tolerant pins	[2][4]	–0.5	+6.0	V
	input voltage	other pins	[2][3][4]	–0.5	V_{DD} + 0.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
T_{stg}	storage temperature			–40	+125	°C
$P_{tot(pack)}$	total power dissipation (per package)		[5]	-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[6]			
		all pins		–1000	+1000	V

[1] The following applies to Table 5:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] All inputs are 5 V tolerant except external memory bus and USB pins.

[3] Referenced to the applicable V_{DD} for the pin. Not to exceed 4.6 V.

[4] Including voltage on outputs in 3-state mode.

[5] Based on package heat transfer, not device power consumption.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage	on pins XTALI and X32I		0	-	1.8	V
$V_{o(xtal)}$	crystal output voltage	on pins XTALO and X32O		0	-	1.8	V
DC-to-DC converter							
V_{BAT}	battery supply voltage			0.9	1.2	1.6	V
$V_{O(DCDC1)}$	DC-to-DC converter 1 output voltage	V_{BAT} = 1.2 V; $I_{L(DCDC1)(max)}$ = 100 mA		-	3.2	-	V
$I_{L(DCDC1)(max)}$	maximum DC-to-DC converter 1 load current			-	100	-	mA
$f_{i(clk)(DCDC1)}$	DC-to-DC converter 1 clock input frequency			-	12	-	MHz
$V_{O(DCDC2)}$	DC-to-DC converter 2 output voltage	V_{BAT} = 1.2 V; $I_{L(DCDC2)(max)}$ = 90 mA		-	1.83	-	V
$I_{L(DCDC2)(max)}$	maximum DC-to-DC converter 2 load current			-	90	-	mA
$f_{i(clk)(DCDC2)}$	DC-to-DC converter 2 clock input frequency			-	12	-	MHz
V_{USB}	USB supply voltage			4.0	5.0	5.5	V
$V_{O(LDO1)}$	LDO1 output voltage	V_{USB} = 5.0 V; $I_{L(LDO1)(max)}$ = 150 mA		-	3.4	-	V
$I_{L(LDO1)(max)}$	maximum LDO1 load current			-	150	-	mA
$V_{O(LDO2)}$	LDO2 output voltage	V_{USB} = 5.0 V; $I_{L(LDO2)(max)}$ = 100 mA		-	1.88	-	V
$I_{L(LDO2)(max)}$	maximum LDO2 load current			-	100	-	mA
Power consumption							
$I_{DD(CORE)}$	core supply current	V_{DD} = 1.8 V	[13]	-	60	-	mA
$I_{DD(EMC)}$	external memory controller supply current	$V_{DD(EMC)}$ = 1.8 V; HCLK = 18 MHz	[14]	-	1.2	-	mA
		$V_{DD(EMC)}$ = 3.3 V; HCLK = 36 MHz	[14]	-	2.2	-	mA
I_{BAT}	battery supply current	V_{DCDC_VBAT} = 1.2 V		-	130	-	mA
		powered down		-	18	-	µA
$I_{CC(osc)}$	oscillator supply current	oscillator running	[15]	-	300	-	µA
		oscillator powered down	[15]	-	-	10	µA
$I_{DD(RTC)}$	RTC supply current	oscillator running	[16]	-	300	-	µA
		oscillator powered down	[16]	-	-	10	µA
$I_{DD(ADC)}$	ADC supply current	normal	[17]	-	-	400	µA
		powered down	[17]	-	-	< 1	µA
I_{DDIA}	analog input supply current	normal	[18]	-	6	-	mA
		powered down	[18]	-	10	-	µA
$I_{DDO(DAC)}$	DAC output supply current	normal	[19]	-	0.7	-	mA
		powered down	[19]	-	10	-	µA

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	32.768 kHz oscillator stops; 12 MHz oscillator runs; external DC-to-DC converter supplies 1.8 V	[20]	-	0.97	-	mA
I_{DD}	supply current	32.768 kHz oscillator runs; 12 MHz oscillator stops; external DC-to-DC converter supplies 3.3 V	[20]	-	1.27	-	mA
I_{DD}	supply current	32.768 kHz oscillator stops; 12 MHz oscillator runs; external DC-to-DC converter supplies 3.3 V	[20]	-	1.27	-	mA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 ˚C), nominal supply voltages.

[2] Applies to pins $V_{DD1(CORE1V8)}$, $V_{DD2(CORE1V8)}$, $V_{DD(DADC1V8)}$, $V_{DD1(FLASH1V8)}$, $V_{DD2(FLASH1V8)}$, $V_{DD(OSC1V8)}$, $V_{DD(OSC321V8)}$, $V_{DD1(USB1V8)}$, $V_{DD2(USB1V8)}$.

[3] External supply voltage; applies to pins $V_{DD3(USB3V3)}$, $V_{DD4(USB3V3)}$, $V_{DD1(IO3V3)}$, $V_{DD2(IO3V3)}$, $V_{DD3(IO3V3)}$, $V_{DD4(IO3V3)}$.

[4] Applies to pins $V_{DD(DADC3V3)}$, $V_{DD(ADC3V3)}$, $V_{DD(DAC3V3)}$, $V_{DD5(IO3V3)}$, $V_{DD6(IO3V3)}$.

[5] External supply voltage; applies to pins $V_{DD1(EMC)}$, $V_{DD2(EMC)}$.

[6] Referenced to the applicable V_{DD} for the pin, which must be present.

[7] Including voltage on outputs in 3-state mode.

[8] Applies to pins with a V_{DD} supply of 1.8 V.

[9] Applies to pins with a V_{DD} supply of 3.3 V.

[10] Applies to 5 V tolerant pins.

[11] Accounts for 100 mV voltage drop in all supply lines.

[12] Only allowed for a short time period.

[13] Applies to pins $V_{DD1(CORE1V8)}$, $V_{DD2(CORE1V8)}$, $V_{DD1(FLASH1V8)}$, $V_{DD2(FLASH1V8)}$

[14] Applies to pins $V_{DD1(EMC)}$, $V_{DD2(EMC)}$.

[15] Applies to pin $V_{DD(OSC1V8)}$.

[16] Applies to pin $V_{DD(OSC321V8)}$.

[17] Applies to pin $V_{DD(ADC3V3)}$.

[18] Applies to pins $V_{DD(DADC1V8)}$, $V_{DD(DADC3V3)}$.

[19] Applies to pin $V_{DD(DAC3V3)}$.

[20] All the above tests were done on the Icetech LPC288x evaluation board. Here are the different configurations that need to be done to achieve the above numbers:

a) Resistors R7 and R8 on the board should be removed to reduce the power consumption on the LED's D2 and D3.

b) The Analog-to-Digital Converter (ADC), the Dual-channel 16-bit Analog-to-Digital Converter and the Dual-channel 16-bit Digital-to-Analog Converter are powered down.

c) The USB device controller is suspended.

d) All power control registers in the Clock Generation Unit have a value of 7h, and the Power Mode register in the Clock Generation Unit has a value of 3h such that the output clocks of all spreading stages are disabled.

e) The floating pins are set to output state.

f) The Event Router is configured in such a way that it will generate its wake-up output to the Clock Generation Unit with a rising-edge signal on the MODE1/P2[2] or the MODE2/P2[3].

9. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
External clock							
f_{ext}	external clock frequency		[2]	1	12	20	MHz
Port pins							
t_r	rise time			-	5	-	ns
t_f	fall time			-	5	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Supplied by an external crystal.

Table 9. Dynamic characteristics: dynamic external memory interface

C_L = 25 pF, T_{amb} = 20 °C, $V_{DD1(EMC)}$ = $V_{DD2(EMC)}$ = 3.3 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Read cycle parameters[1]						
t_{CHCX}	clock HIGH time		-	11.1	-	ns
t_{CLCX}	clock LOW time		-	11.1	-	ns
T_{CLCL}	clock cycle time		-	27.8	-	ns
$t_{su(S)}$	chip select set-up time		-	7.5	-	ns
$t_{h(S)}$	chip select hold time		-	3.5	-	ns
$t_{su(RAS)}$	row address strobe set-up time		-	7.5	-	ns
$t_{h(RAS)}$	row address strobe hold time		-	3.5	-	ns
$t_{su(CAS)}$	column address strobe set-up time		-	7.5	-	ns
$t_{h(CAS)}$	column address strobe hold time		-	3.5	-	ns
$t_{su(G)}$	output enable set-up time		-	7.5	-	ns
$t_{h(G)}$	output enable hold time		-	3.5	-	ns
$t_{su(A)}$	address set-up time		-	7.5	-	ns
$t_{h(A)}$	address hold time		-	3.5	-	ns
$t_{su(DQ)}$	data input/output set-up time		-	23.5	-	ns
$t_{h(DQ)}$	data input/output hold time		-	3.5	-	ns
Write cycle parameters[2]						
t_{CHCX}	clock HIGH time		-	11.1	-	ns
t_{CLCX}	clock LOW time		-	11.1	-	ns
T_{CLCL}	clock cycle time		-	27.8	-	ns
$t_{su(S)}$	chip select set-up time		-	7.5	-	ns
$t_{h(S)}$	chip select hold time		-	3.5	-	ns
$t_{su(RAS)}$	row address strobe set-up time		-	7.5	-	ns
$t_{h(RAS)}$	row address strobe hold time		-	3.5	-	ns
$t_{su(CAS)}$	column address strobe set-up time		-	7.5	-	ns
$t_{h(CAS)}$	column address strobe hold time		-	3.5	-	ns
$t_{su(W)}$	write set-up time		-	7.5	-	ns
$t_{h(W)}$	write hold time		-	3.5	-	ns
$t_{su(DQM)}$	DQM set-up time		-	7.5	-	ns
$t_{h(DQM)}$	DQM hold time		-	3.5	-	ns
$t_{su(A)}$	address set-up time		-	7.5	-	ns
$t_{h(A)}$	address hold time		-	3.5	-	ns
$t_{su(DQ)}$	data input/output set-up time		-	16.5	-	ns
$t_{h(DQ)}$	data input/output hold time		-	10.5	-	ns

[1] CKE is HIGH during the read cycle.

[2] CKE is HIGH during the write cycle

Table 10. Dynamic characteristics: dynamic external memory interface

C_L = 25 pF, T_{amb} = 20 °C, $V_{DD1(EMC)}$ = $V_{DD2(EMC)}$ = 1.8 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Read cycle parameters[1]						
t_{CHCX}	clock HIGH time		-	23	-	ns
t_{CLCX}	clock LOW time		-	23	-	ns
T_{CLCL}	clock cycle time		-	55.6	-	ns
$t_{su(S)}$	chip select set-up time		-	40	-	ns
$t_{h(S)}$	chip select hold time		-	3.5	-	ns
$t_{su(RAS)}$	row address strobe set-up time		-	40	-	ns
$t_{h(RAS)}$	row address strobe hold time		-	3.5	-	ns
$t_{su(CAS)}$	column address strobe set-up time		-	40	-	ns
$t_{h(CAS)}$	column address strobe hold time		-	3.5	-	ns
$t_{su(G)}$	output enable set-up time		-	40	-	ns
$t_{h(G)}$	output enable hold time		-	3.5	-	ns
$t_{su(A)}$	address set-up time		-	36	-	ns
$t_{h(A)}$	address hold time		-	19.5	-	ns
$t_{su(DQ)}$	data input/output set-up time		-	51.5	-	ns
$t_{h(DQ)}$	data input/output hold time		-	4	-	ns
Write cycle parameters[2]						
t_{CHCX}	clock HIGH time		-	23	-	ns
t_{CLCX}	clock LOW time		-	23	-	ns
T_{CLCL}	clock cycle time		-	55.6	-	ns
$t_{su(S)}$	chip select set-up time		-	40	-	ns
$t_{h(S)}$	chip select hold time		-	3.5	-	ns
$t_{su(RAS)}$	row address strobe set-up time		-	40	-	ns
$t_{h(RAS)}$	row address strobe hold time		-	3.5	-	ns
$t_{su(CAS)}$	column address strobe set-up time		-	40	-	ns
$t_{h(CAS)}$	column address strobe hold time		-	3.5	-	ns
$t_{su(W)}$	write set-up time		-	40	-	ns
$t_{h(W)}$	write hold time		-	3.5	-	ns
$t_{su(DQM)}$	DQM set-up time		-	40	-	ns
$t_{h(DQM)}$	DQM hold time		-	3.5	-	ns
$t_{su(A)}$	address set-up time		-	36	-	ns
$t_{h(A)}$	address hold time		-	19.5	-	ns
$t_{su(DQ)}$	data input/output set-up time		-	31	-	ns
$t_{h(DQ)}$	data input/output hold time		-	24.5	-	ns

[1] CKE is HIGH during the read cycle.

[2] CKE is HIGH during the write cycle.

9.1 Timing

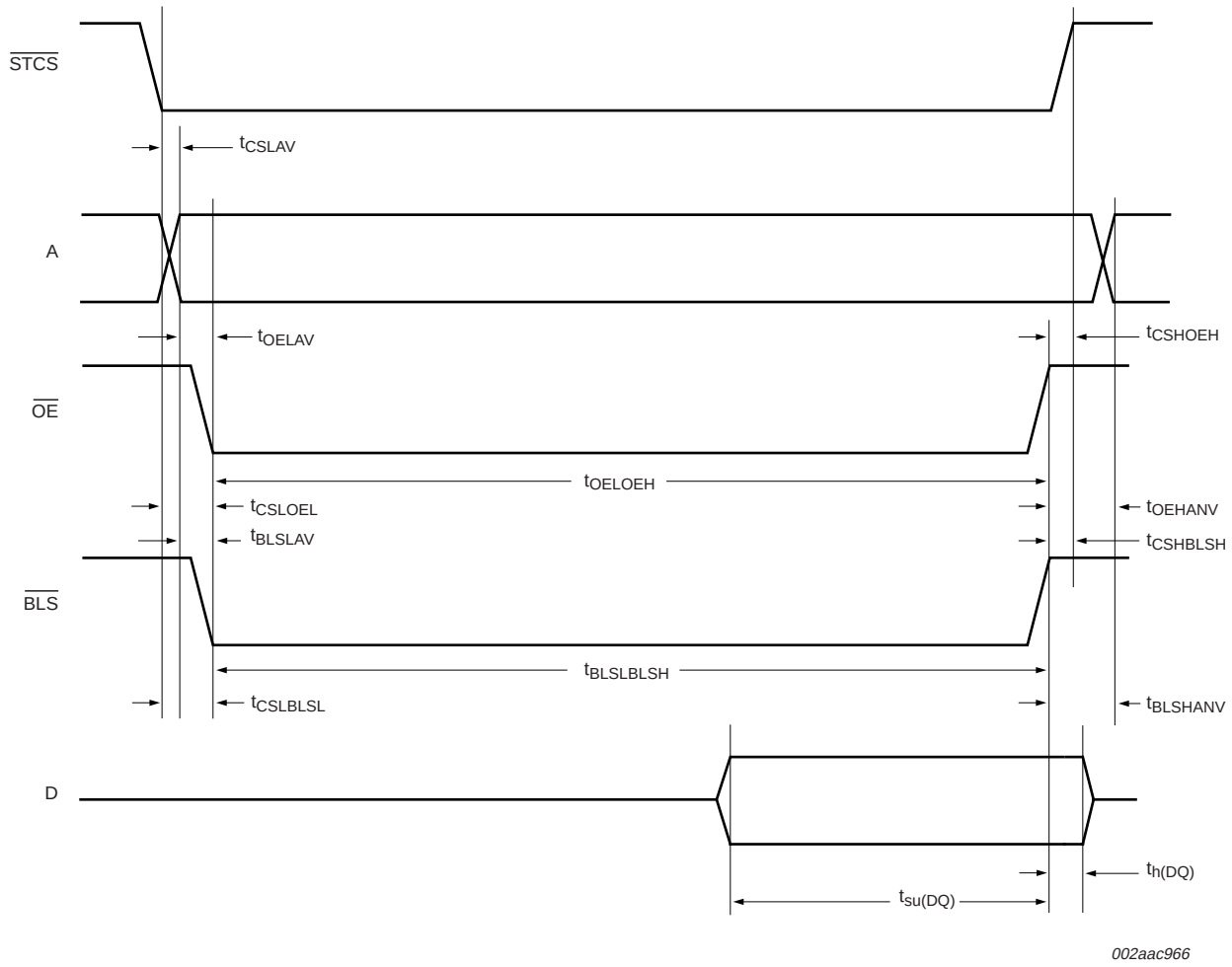

Fig 4. External memory read access to static memory

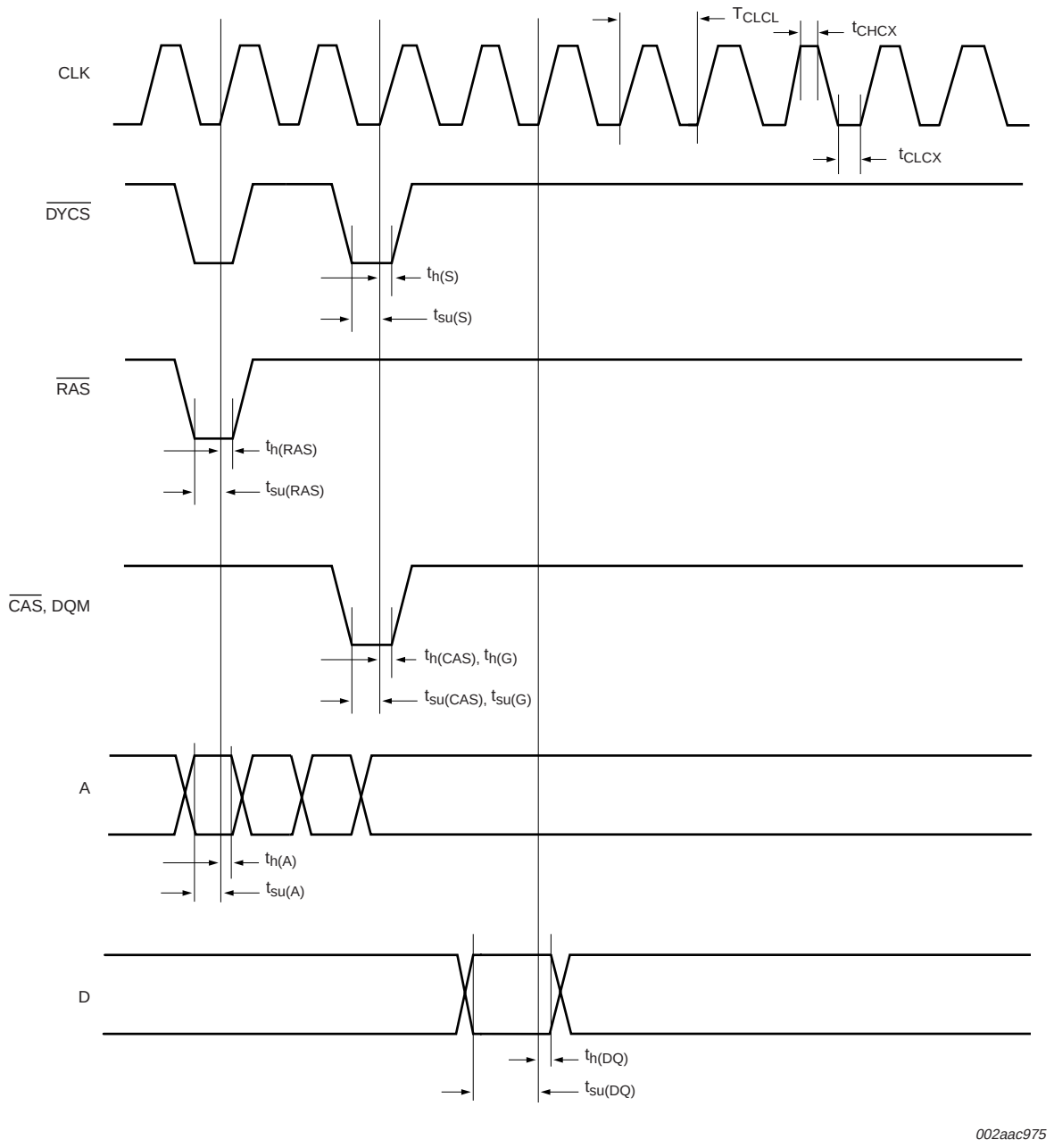

Fig 6. External memory read access to dynamic memory

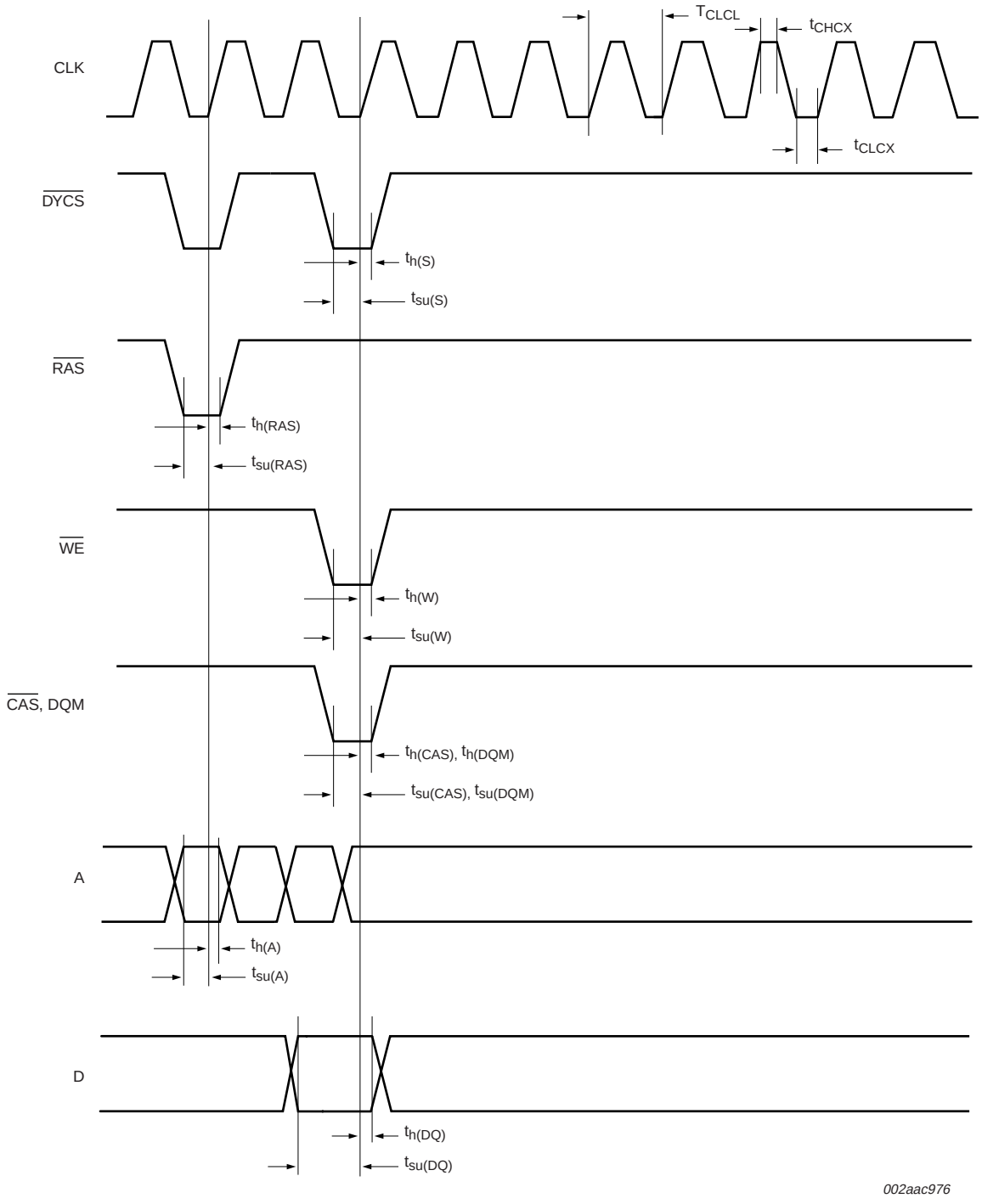

Fig 7. External memory write access to dynamic memory

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2880_LPC2888_3	20080417	Preliminary data sheet	-	LPC2880_2888_2
Modifications:	• Table 1 “Ordering information”; added /01 and /D1 parts. • Table 2 “Ordering options”; added JTAG interface column to show the difference between /01 and /D1 devices. • Table 5; ESD specification added. • Table 6; DC-to-DC converter and power consumption characteristics added. • Table 8, Table 9, Table 10; external memory interface dynamic characteristics added. • Figure 1, changed ‘ARM7TDMI-S’ to ‘ARM7TDMI’. • Figure 4, Figure 5, Figure 6, Figure 7; external memory interface timing diagrams added.			
LPC2880_LPC2888_2	20061121	Preliminary data sheet	-	LPC2880_LPC2888_1
LPC2880_LPC2888_1	20060622	Preliminary data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 17 April 2008
Document identifier: LPC2880_LPC2888_3