Rohm Semiconductor - ML630Q466-NNNTBZWAX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, SSIO, UART/USART, USB
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (32K x 32)
Program Memory Type	FLASH
EEPROM Size	512 x 32
RAM Size	4K x 32
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml630q466-nnntbzwax

- Timers (TMR)
  – 8 bits × 8 channels
    (Timer0-7: 16-bit x 4 configuration available by using Timer0-1 or Timer2-3, Timer4-5, Timer6-7)
  – Selection of one shot timer mode is possible
  – External clock can be selected as timer clock.

- Function Timers (FTM)
  – 16-bit × 4 channels
  – Equipped with the timer/capture/PWM functions using a 16-bit counter
  – An event trigger (external pin input interrupt or timer interrupt request) can control start/stop/clear of the timer (however, the minimum pulse width of pin input is timer clock 3ϕ)
  – 1 to 64 dividing of LSCLK/OSCLK/HSCLK/external input selectable as timer clock
  – Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output.

- Real Time Clock (RTC)
  – 1 channels (99 years calendar, alarm, revision of the clock)

- Watchdog timer (WDT)
  – Non-maskable interrupt and reset
  – Free running
  – Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)

- Synchronous serial port (SSIOF/SSIO)
  – without FIFOs (SSIO) : 1 channel
  – with 16-byte transmits and receives FIFOs (SSIOF) : 1 channel
  – Master/slave selectable
  – LSB first/MSB first selectable
  – Clock polarity (data out at rising edge and data in at falling edge/data out at falling edge and data in at rising edge) selectable
  – 8-bit length/16-bit length selectable
  – Initial clock level (High start/Low start) selectable
  – supports slave-select signal (only SSIOF)

- UART (UARTF/UART)
  – without FIFOs (UART) : 1channel
  – with 16-byte transmits and receives FIFOs (UARTF) :1 channels
  – Full duplex buffer system
  – Communication speed: Settable within the range of 2400bps to 115200bps.
  – Programmable interface (data length, parity, stop bits selectable)

- I^2C bus interface (I^2CF/I^2C)
  – without FIFOs(I^2C) :1 channel
  – with 16-byte transmits and receives FIFOs (I^2CF) : 1 channels
  – Master/slave function (only I2CF)
  – Fast mode (400 kHz), standard mode (100 kHz)

- USB full-speed device
  – Compliant with Universal Serial Bus (USB)
  – Full speed (12 Mbps) 1 port.
  – End points: 5 or 6
  – Supports all data transfer types (control transfer, bulk transfer, interrupt transfer, isochronous transfer).
  – Built-in SOF generation and CRC5/16 generation functions
  – Access size to data transfer FIFOs: 8 bits/16 bits/32 bits

- General-purpose ports (PORT)
  – Input/output port × 38 channels (including secondary or tertiary or quaternary or quinary functions).
    (ML630Q464 and ML630Q466: including LCD com/seg ports (each 20 ports))

- RC oscillation type A/D converter (RC-ADC)
  - Time division × 2 channels
  - Starting by trigger of Timer/FTM function.
  - 24-bit counter

- Successive approximation type A/D converter (SA-ADC)
  - Input × 12 channels
  - 12-bit A/D converter
  - Starting by trigger of Timer/FTM function.
  - Capacitive touch sense function

- Analog Comparator (CMP)
  - Input × 2ch
  - Common mode input voltage: 0.2V to V_{DD}−0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection

- Voltage Level Supervisor (VLS)
  - Threshold voltages: One of 64 levels
  - Acuraccy: ±3%
  - Interrupt or Reset generation are slectable
  - Voltage measurement with voltage input pin or V_{DD} pin

- Low Level Detector(LLD)
  - Judgment Voltage: 1.8V±0.2V
  - Can be used as low level detection reset.

- LCD driver
  - Maximun 400 dots (50 segment x 8 common)
  - 1/1 to 1/8 duty
  - 1/2, 1/3 bias (built-in bias generation circuit)
  - Frame frequency selecable
  - Bias voltage multiplying clock selectable (5 types)
  - Contrast adjustment (32 steps)
  - 4 operating mode: LCD drive stop, LCD display, all LCDs on, all LCDs off
  - Programmable display allocation function

- Random number generator (RANDOM)
  - Generates 8-bit random numbers

- AES
  - 128-bit Common key
  - Supports key sizes of 128, 192, and 256 bits
  - Supports ECB, CBC, and CTR modes

- Reset
  - Reset by the RESET_N pin input
  - Reset by power-on detection
  - Reset by overflow of watchdog timer (WDT)
  - Reset by threshold detection in Voltage Level Supervisor(VLS)
  - Reset by low level detection in Low Level Detector(LLD)
  - Reset by the low-speed crystal oscillation stop detection
  - Reset by SYSRESETREQ of Cortex™-M0+ (software reset)

- Clock
  - Low-speed clock:
    - Crystal oscillation (32.768 kHz)
    - Built-in RC oscillation (32.768kHz)
  - High-speed clock:
    - PLL (24 MHz) generated from Crystal oscillation (32.768 kHz)
    - Built-in RC oscillation (16MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
  - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits can keep in operating states.
  - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states.
  - ULTRA-DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states, at V_{DD}>2.5V.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8,1/16,1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Guaranteed operating range
  - Operating temperature (ambient) : –40°C to +85°C
  - Operating voltage: V_{DD} = 1.8V to 3.6V

- Supply current (Typ)
  - High-speed operation (24 MHz) : 250uA/MHz
  - ULTRA-DEEP-HALT : 0.80uA

- Package
  - 100-pin plastic TQFP
    - Tray
      ML630Q464-xxxTBZWAX
      ML630Q466-xxxTBZWAX

■ PIN CONFIGURATION

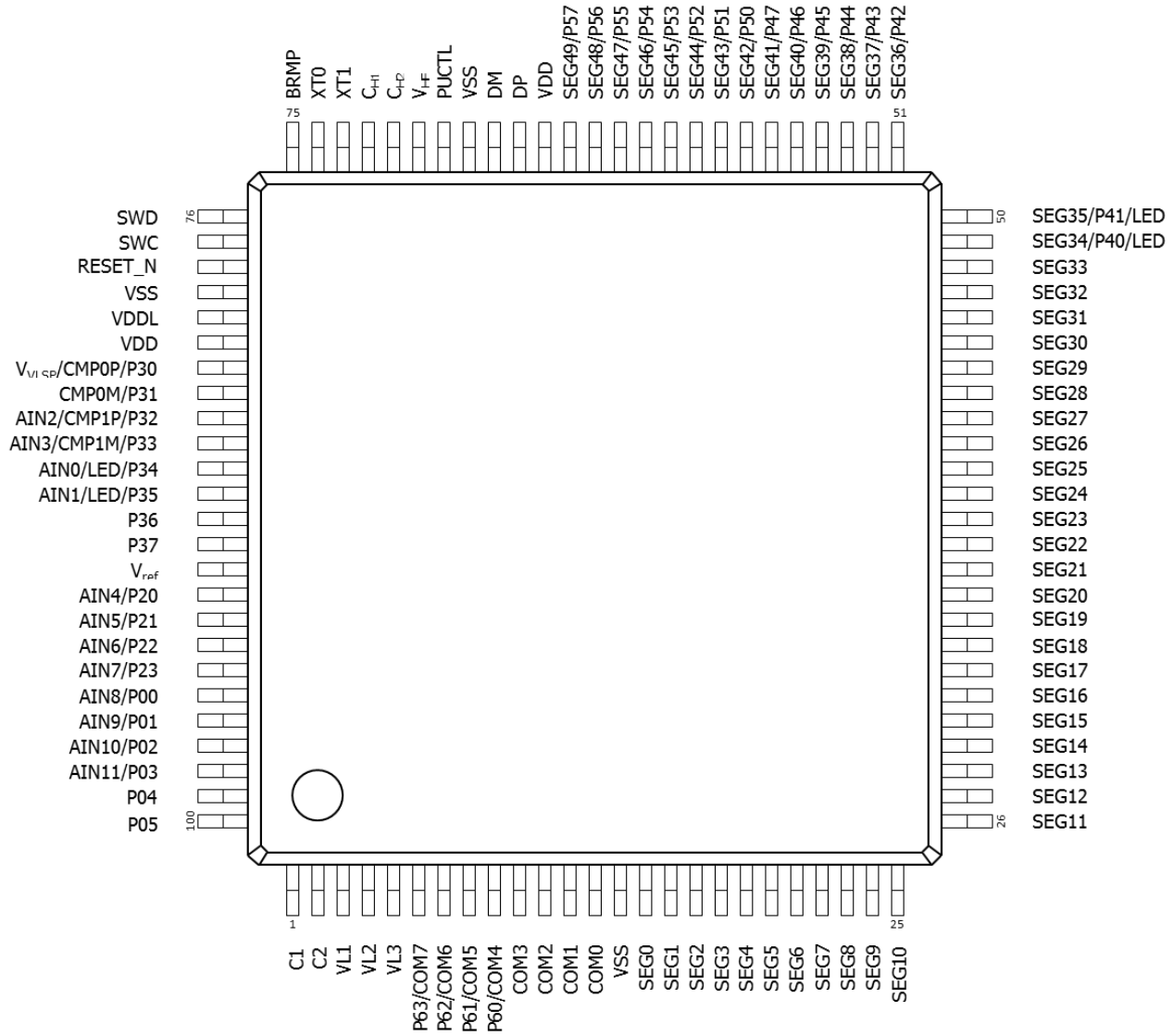


Figure 2. Pin Layout of ML630Q464/Q466

■ PIN LIST

PIN No.	.Reset State	Primary Function		Secondary Function		Tertiary Function		Quaternary Function		Quinary Function	
		Pin name	I/O	Pin name	I/O	pin name	I/O	pin name	I/O	pin name	I/O
14 68 79	–	V_{SS}	–	–	–	–	–	–	–	–	–
65 81	–	V_{DD}	–	–	–	–	–	–	–	–	–
80	–	V_{DDL}	–	–	–	–	–	–	–	–	–
70	–	V_{HF}	–	–	–	–	–	–	–	–	–
90	–	V_{REF}	–	–	–	–	–	–	–	–	–
74	–	XT0	–	–	–	–	–	–	–	–	–
73	–	XT1	–	–	–	–	–	–	–	–	–
78	Pull-up Input	RESET_N	I	–	–	–	–	–	–	–	–
77	Pull-up Input	SWC	I	–	–	–	–	–	–	–	–
76	Pull-up Input	SWD	I/O	–	–	–	–	–	–	–	–
75	Pull-down Input	BRMP	I	–	–	–	–	–	–	–	–
95	Hi-Z output	P00/ EXI00/ AIN8	I/O	IN0	I	SOUT0	O	RXDF0	I	–	–
96	Hi-Z output	P01/ EXI01/ AIN9	I/O	CS0	O	SIN0	I	TXDF0	O	–	–
97	Hi-Z output	P02/ EXI02/ AIN10	I/O	RCT0	O	SCK0	I/O	TMOUT0	O	–	–
98	Hi-Z output	P03/ EXI03/ AIN11	I/O	RS0	O	–	–	TMOUT1	O	–	–
99	Hi-Z output	P04/ EXI04	I/O	RT0	O	–	–	–	–	–	–
100	Hi-Z output	P05/ EXI05	I/O	RCM	O	–	–	–	–	–	–
91	Hi-Z output	P20/ EXI20/ AIN4	I/O	IN1	I	SOUTF0	O	–	–	–	–
92	Hi-Z output	P21/ EXI21/ AIN5	I/O	CS1	O	SINF0	I	–	–	–	–
93	Hi-Z output	P22/ EXI22/ AIN6	I/O	RS1	O	SCKF0	I/O	TMOUT2	O	–	–
94	Hi-Z output	P23/ EXI23/ AIN7	I/O	RT1	O	SSF0	I/O	TMOUT3	O	–	–
82	Hi-Z output	P30/ EXI30/ CMP0P V_{VLSP}	I/O	SDAF0	I/O	SOUT0	O	–	–	–	–
83	Hi-Z output	P31/ EXI31/ CMP0M	I/O	SCLF0	I/O	SIN0	I	–	–	–	–
84	Hi-Z output	P32/ EXI32/ CMP1P/ AIN2	I/O	RXDF0	I	SCK0	I/O	TMOUT4	O	–	–
85	Hi-Z output	P33/ EXI33/ CMP1M/ AIN3	I/O	TXDF0	O	32kCLKO	O	TMOUT5	O	–	–
86	Hi-Z output	P34/ EXI34/ AIN0 LED	I/O	SDA1	I/O	SOUTF0	O	–	–	–	–
87	Hi-Z output	P35/ EXI35/ AIN1 LED	I/O	SCL1	O	SINF0	I	–	–	–	–
88	Hi-Z output	P36/ EXI36/ TMCKI4	I/O	RXD0	I	SCKF0	I/O	TMOUT6	O	–	–
89	Hi-Z output	P37/ EXI37/ TMCKI5	I/O	TXD0	O	SSF0	I/O	TMOUT7	O	–	–
13 to 10	Low Level Output	COM0 to COM3	O	–	–	–	–	–	–	–	–
9	Hi-Z output	P60/ EXI60	I/O	COM4	O	–	–	–	–	–	–
8	Hi-Z output	P61/ EXI61	I/O	COM5	O	–	–	–	–	–	–
7	Hi-Z output	P62/ EXI62	I/O	COM6	O	–	–	–	–	–	–
6	Hi-Z output	P63/ EXI63	I/O	COM7	O	–	–	–	–	–	–
15 to 48	Low Level Output	SEG0 to SEG33	O	–	–	–	–	–	–	–	–
49	Hi-Z output	P40/ EXI40/ LED	I/O	SDAF0	I/O	SOUT0	O	–	–	SEG34	O

■ PIN DESCRIPTION

In the table below indicates the functional pin description.
The pin name represents the function pin name of the primary function of each terminal, The pin mode represents the set of mode register of Port Control.
(1st:primary function, 2nd:secondary function, 3rd: tertiary function, 4th: quaternary function, 5th:quinary function)

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
System					
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	RESET_N	–	L
BRMP	I	Remapping control input (for firmware update) Based on the BRMP pin setting at the time of the reset release, Bank0 is remapped.	BRMP	–	H
XT0	I	Crystal connection pin for low-speed clock. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS} as required.	XT0	–	–
XT1	O		XT1	–	–
32kCLKO	O	Low-speed clock output pin	P33,P43,P53	2nd	
General-purpose input/output port					
P00-P05	I/O	General-purpose input/output port.	P00-P05	1st	–
P20-P23	I/O	General-purpose input/output port.	P20-P23	1st	–
P30-P37	I/O	General-purpose input/output port.	P30-P37	1st	–
P40-P47	I/O	General-purpose input/output port.	P40-P47	1st	–
P50-P57	I/O	General-purpose input/output port.	P50-P57	1st	–
P60-P63	I/O	General-purpose input/output port.	P60-P63	1st	–
External interrupt					
EXI00-05 EXI20-23 EXI30-37 EXI40-47 EXI50-57 EXI60-63	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software.	P00-P05 P20-P23 P30-P37 P40-P47 P50-P57 P60-P63	1st	H/L
LED					
LED	O	N-channel open drain output pins to drive LED.	P34,P35,P40,P41	1st	–
UART					
TXD0	O	UART data output pin.	P37,P47,P57	2nd	–
RXD0	I	UART data input pin.	P36,P46,P56	2nd	–
TXDF0	O	UARTF with FIFO data output pin.	P01,P33,P43,P53	2nd	–
RXDF0	I	UARTF with FIFO data input pin.	P00,P32,P42,P52	2nd	–
I^2C bus interface					
SDA1	I/O	I2C1 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P34,P44,P54	2nd	–
SCL1	O	I2C1 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P35,P45,P55	2nd	–
SDAF0	I/O	I2CF0 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P30,P40,P50	2nd	–
SCLF0	I/O	I2CF0 clock input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P31,P41,P51	2nd	–

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
Synchronous serial					
SCK0	I/O	Synchronous serial (SSIO) clock input/output pin.	P02,P32,P42,P52	3rd	–
SIN0	I	Synchronous serial (SSIO) data input pin.	P01,P31,P41,P51	3rd	–
SOUT0	O	Synchronous serial (SSIO) data output pin.	P00,P30,P40,P50	3rd	–
SCKF0	I/O	Synchronous serial with FIFO (SSIOF) clock input/output pin.	P22,P36,P46,P56	3rd	–
SINF0	I	Synchronous serial with FIFO (SSIOF) data input pin.	P21,P35,P45,P55	3rd	–
SOUTF0	O	Synchronous serial with FIFO (SSIOF) data output pin.	P20,P34,P44,P54	3rd	–
SSF0	I/O	Synchronous serial with FIFO (SSIOF) select input/output pin.	P23,P37,P47,P57	3rd	L
FTM					
TMOUT0-9 TMOUTA-F	O	FTM output pin.	P02,P03,P22,P23 P32,P33,P36,P37 P42,P43,P46,P47 P52,P53,P56,P57	4th	–
TMCKI0-7	I	External clock input pin for FTM.	P42,P43,P46,P47 P36,P37,P56,P57	1st	–
RC oscillation type A/D converter					
IN0	I	Oscillation input pin of Channel 0.	P00	2nd	–
CS0	O	Reference capacitor connection pin of Channel 0.	P01	2nd	–
RS0	O	Reference resistor connection pin of Channel 0.	P03	2nd	–
RT0	O	Resistor sensor connection pin for measurement of Channel 0.	P04	2nd	–
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement.	P02	2nd	–
RCM	O	RC oscillation monitor pin.	P05	2nd	–
IN1	I	Oscillation input pin of Channel 1.	P20	2nd	–
CS1	O	Reference capacitor connection pin of Channel 1.	P21	2nd	–
RS1	O	Reference resistor connection pin of Channel 1.	P22	2nd	–
RT1	O	Resistor sensor connection pin for measurement of Channel 1.	P23	2nd	–
Successive approximation type A/D converter					
V_{REF}	I	Reference power supply pin for successive approximation type A/D converter.	V_{REF}	–	–
AIN0-11	I	Analog input for successive approximation type A/D converter.	(AIN0-3) P32-35, (AIN4-7) P20-23, (AIN8-11) P00-03	1st	–
Analog comparator					
CMP0P	I	Comparator0 Non-inverted input pin.	P30	1st	–
CMP0M	I	Comparator0 Inverted input pin.	P31	1st	–
CMP1P	I	Comparator1 Non-inverted input pin.	P32	1st	–
CMP1M	I	Comparator1 Inverted input pin.	P33	1st	–
USB FS Device					
DP	I/O	USB dev D+ pin.	DP	–	–
DM	I/O	USB dev D- pin.	DM	–	–
PUCTL	O	USB dev pull-up control	PUCTL	–	–
DEBUG Interface					
SWC	I	Serial clock of Serial Wire Debug Port	SWC	–	–
SWD	I/O	Serial I/O data of Serial Wire Debug Port	SWD	–	–

■ TERMINATION OF UNUSED PINS

Table 1 shows methods of terminating the unused pins.

Table 1 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	open
BRMP	Connect a pull-down resistor.
SWC	Connect a pull-up resistor.
SWD	Connect a pull-up resistor.
V_{REF}	Connect to V_{DD}
P00 to P05	open
P20 to P23	open
P30 to P37	open
P40 to P47	open
P50 to P57	open
P60 to P63	open
COM0 to COM3	open
SEG0 to SEG33	open
DP, DM, PUCTL	open
V_{L1}, V_{L2}, V_{L3}	open
C_1, C_2	open

[Note]
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

		VLSLV[5:0] = 2DH	Typ. -3%	2.650	Typ. +3%	V	1
		VLSLV[5:0] = 2EH		2.700			
		VLSLV[5:0] = 2FH		2.750			
		VLSLV[5:0] =30H		2.800			
		VLSLV[5:0] = 31H		2.850			
		VLSLV[5:0] = 32H		2.900			
		VLSLV[5:0] = 33H		2.950			
		VLSLV[5:0] = 34H		3.000			
		VLSLV[5:0] = 35H		3.050			
		VLSLV[5:0] = 36H		3.100			
		VLSLV[5:0] = 37H		3.150			
		VLSLV[5:0] = 38H		3.200			
		VLSLV[5:0] = 39H		3.250			
		VLSLV[5:0] = 3AH		3.300			
		VLSLV[5:0] = 3BH		3.350			
		VLSLV[5:0] = 3CH		3.400			
		VLSLV[5:0] = 3DH		3.450			
		VLSLV[5:0] = 3EH		3.500			
		VLSLV[5:0] = 3FH		3.550			
V_{VLS} Hysteresis width (V_{DD}=rise)	H_{VLS}	–	V_{VLS} x 1.0%	V_{VLS} x 2.7%	V_{VLS} x 4.5%	V	

VLSLV[3:0] are bits of the VLSCON register to change detection voltage level.
*1: Setable only at the time of select to V_{VLSP} pin.

● DC characteristics (LLD)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
LLD judge Voltage	VLLR	–	1.60	1.80	2.00	V	1

● DC/AC characteristics (Analog comparator)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Common Input voltage range	V_{CMPIN}	–	0.2	–	V_{DD} -0.2	V	1
Input offset voltage	V_{CMPOF}	–	-30	–	30	mV	
Comparator judge time	T_{CMP}	CMPP- CMPM =40mV	–	–	2	μs	

● DC characteristics (VOHL, IOHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57,, P60-P63, SWD,PUCTL)	VOH1	IOH=-1.0mA	V_{DD} -0.5	–	–	V	2
	VOL1	IOL=+0.5mA	–	–	0.4		
Output voltage 2 (P34, P35, P40, P41) (LED mode is selected)	VOL2	2.7V ≤V_{DD} ≤3.6V IOL=+5.0mA	–	–	0.6		
		IOL=+2.0mA	–	–	0.4		
Output voltage 3 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) (I^2C mode is selected)	VOL3	IOL3= +3mA (I^2Cspec) (V_{DD} ≥2V)	–	–	0.4		
Output voltage 4 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) (I^2C mode is selected)	VOL4	IOL4= +2mA(I^2Cspec) (V_{DD} < 2V)	–	–	V_{DD} ×0.2		
Output voltage 5 (COM0～7) (SEG00～49) (LCD mode is selected)	VOH5	1/3bias, IOH5=-0.02mA, VL1=1.2V	V_{L3} -0.2	–	–		
	VOM5	1/3bias, IOM5=+0.02mA, VL1=1.2V	–	–	V_{L2} +0.2		
	VOM5S	1/3bias, IOM5S=-0.02mA, VL1=1.2V	V_{L2} -0.2	–	–		
	VOML5	1/3bias, IOML5=+0.02mA, VL1=1.2V	–	–	V_{L1} +0.2		
	VOML5S	1/3bias, IOML5S=-0.02mA, VL1=1.2V	V_{L1} -0.2	–	–		
	VOL5	1/3bias, IOL5=+0.02mA, VL1=1.2V	–	–	0.2		
Output voltage 5 (COM0～7) (SEG00～49) (LCD mode is selected)	VOH5	1/2bias, IOH5=-0.01mA, VL1=1.4V	V_{L3} -0.3	—	—		
	VOM5	1/2bias, IOM5=+0.01mA, VL1=1.4V	—	—	V_{L2} +0.3		
	VOM5S	1/2bias, IOM5S=-0.01mA, VL1=1.4V	V_{L2} -0.3	—	—		
	VOML5	1/2bias, IOML5=+0.01mA, VL1=1.4V	—	—	V_{L1} +0.3		
	VOML5S	1/2bias, IOML5S=-0.01mA, VL1=1.4V	V_{L1} -0.3	—	—		
	VOL5	1/2bias, IOL5=+0.01mA, VL1=1.4V	—	—	0.3		

Output leak 1 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63, SWD,PUCTL)	IOOH1	VOH=V_{DD} (at high impedance)	–	–	+1	μA	3
	IOOL1	VOL=V_{SS} (at high impedance)	-1	–	–		

● DC characteristics (IIHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input current 1 (RESET_N)	IIH1	VIH1=V_{DD}	–	–	1	μA	4
	IIL1	VIL1=V_{SS}	-900	-300	-20		
Input current 3 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63, SWC, SWD, BRMP)	IIH3	VIH3=V_{DD} (at pull down)	1	15	200		
	IIL3	VIL3=V_{SS} (at pull up)	-200	-15	-1		
	IIH3Z	VIH3=V_{DD} (at high impedance)	–	–	1		
	IIL3Z	VIL3=V_{SS} (at high impedance)	-1	–	–		
Input current 4 (P36, P37, P40-P47, P50-P57, P60-P63)	IIH4Z	VIH4=5.0V (at high impedance)	–	–	1		

*1 : typ.rating is V_{DD}=3.0V, Ta=25°C

● DC characteristics (VIHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N, SWD, SWC, BRMP, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63)	VIH1	–	0.7 ×V_{DD}	–	V_{DD}	V	5
	VIL1	–	0	–	0.3 ×V_{DD}		
Input terminal capacitance (RESET_N, SWD, SWC, BRMP, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	–	–	10	pF	–

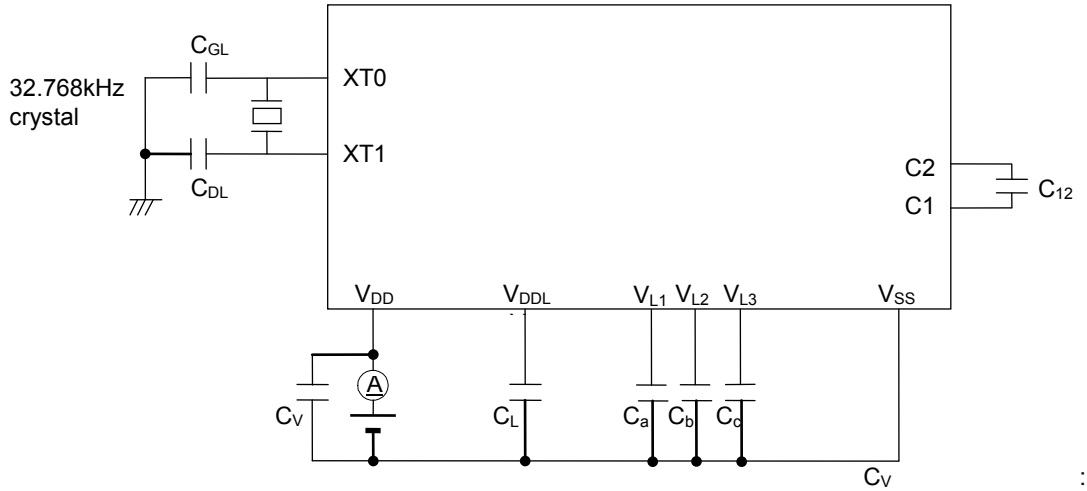
● DC characteristics (USB)

(V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating[*1]			Unit	Measuring circuit
			Min.	Typ.	Max.		
Differential input sensitivity	V_{DI}	Absolute value of the difference between the DP and DM pins	0.2	-	-	V	
Differential common mode range	V_{CM}	Includes VDI range	0.8	-	2.5	V	
Single end input threshold voltage	V_{SE}	-	0.8	-	2.0	V	
High level output voltage	V_{OH}	15k W RL is connected to GND	2.8	-	-	V	
Low level output voltage	V_{OL}	1.5k W RL to 3.6 V	-	-	0.3	V	
Hi-Z state input/output leakage current	I_{LO}	0 V < VIN < 3.3 V	-10		10	uA	
Driver output resistance	Z_{DRV}	Steady state	28		44	Ω	

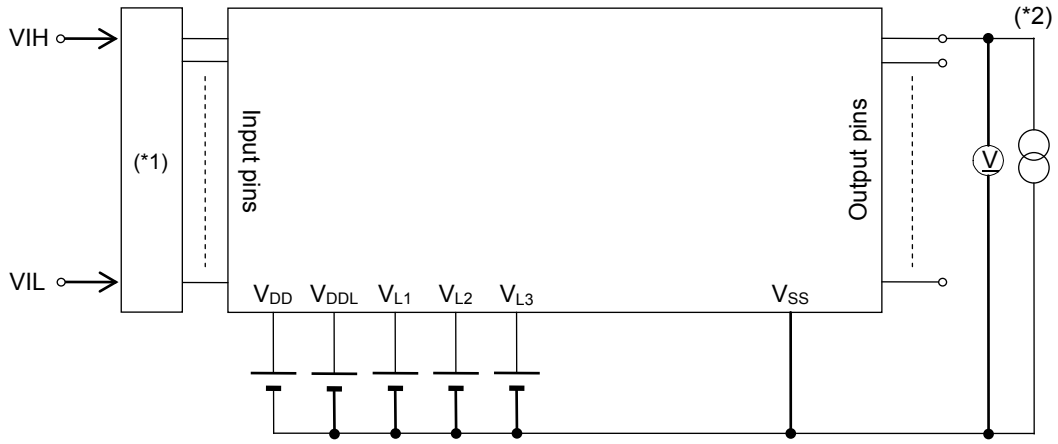
● MEASURING CIRCUITS

MEASURING CIRCUIT1



C_V : 1μF
C_L : 2.2μF
C_a,C_b,C_c : 1μF
C_{12} : 1μF
C_{GL} : 12pF
C_{DL} :12pF
32.768kHz crystal oscilation:
(DT-26 from Daishinku)

MEASURING CIRCUIT 2



(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

● AC characteristics (USB)

(V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Applied pin
			Min.	Typ.	Max.		
Rise time (*1)	T_R	CL = 50 pF	4	–	20	ns	DP, DM
Fall time (*1)	T_F	CL = 50 pF	4	–	20	ns	
Output signal crossover voltage	V_{CRS}	CL = 50 pF	0.8	–	2.5	V	
Data rate	T_{DRATE}	Average bit rate (12Mbps ±0.25%)	11.97	–	12.03	Mbps	

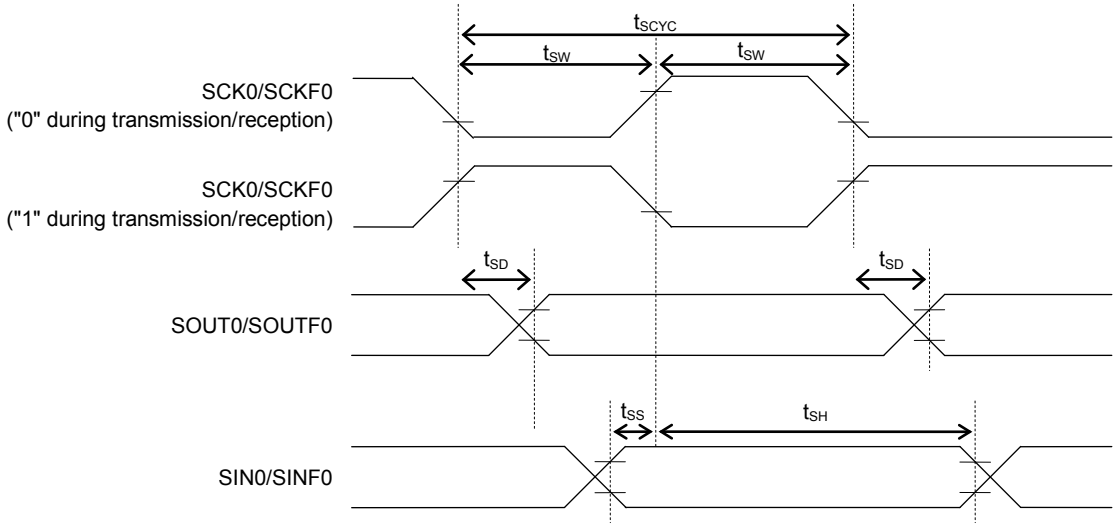
* 1: T_R and T_F: Rise time and fall time between 10% and 90% of the pulse amplitude, respectively

● AC charctoristics (synchronous serial port)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Conditon	Rating			Unit
			Min.	Typ.	Max.	
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation is not active	10	–	–	μs
		High-speed oscillation is active	500	–	–	ns
SCK output cycle (master mode)	t_{SCYC}	–	–	SCK*1	–	s
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation is not active	4	–	–	μs
		High-speed oscillation is active	200	–	–	ns
SCK output pulse width (master mode)	t_{SW}	–	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	–	–	–	180	ns
SOUT output delay time (master mode)	t_{SD}	–	–	–	80	ns
SIN input Setup time (slave mode)	t_{SS}	–	50	–	–	ns
SIN input Setup time (master mode)	t_{SS}	–	130	–	–	ns
SINinput Hold time	t_{SH}	–	50	–	–	ns

*1 : The clock period which is selected by the below registers(min:250ns@ regularly, min:500ns@P02,P22 is used)
In case of SSIO : S0CK2-0 of serial port 0 mode register(SIO0MOD).
In case of SSIOF : SF0BR9-0 of SIOF0 port register(SF0BRR)



● AC characteristics（I^2C Bus interface : Standard mode 100kHz）

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

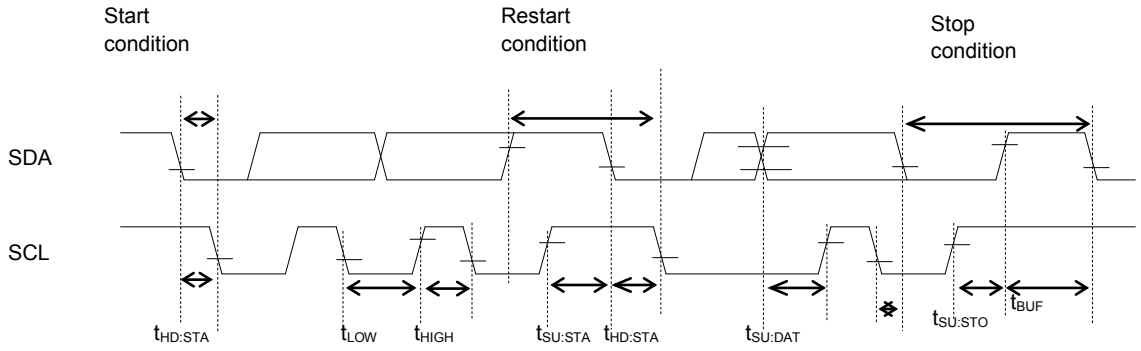
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	–	0	–	100	kHz
SCL hold time (Start/restart condition)	$t_{HD:STA}$	–	4.0	–	–	μs
SCL"L" level time	t_{LOW}	–	4.7	–	–	μs
SCL"H" level time	t_{HIGH}	–	4.0	–	–	μs
SCL setup time (restart condition)	$t_{SU:STA}$	–	4.7	–	–	μs
SDA setup time	$t_{SU:DAT}$	–	0.25	–	–	μs
SDA setup time (stop condition)	$t_{SU:STO}$	–	4.0	–	–	μs
Bus-free time	t_{BUF}	–	4.7	–	–	μs

● AC characteristics（I^2C bus interface : fast mode 400kHz）

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

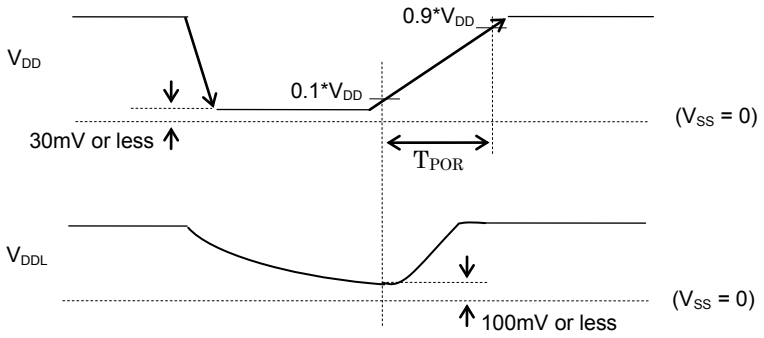
Parameter	Symbol	Condition	Rateing			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	–	0	–	400	kHz
SCLhold time (start/restart condition)	$t_{HD:STA}$	–	0.6	–	–	μs
SCL"L" level time	t_{LOW}	–	1.3	–	–	μs
SCL"H" level time	t_{HIGH}	–	0.6	–	–	μs
SCL setup time (restart condition)	$t_{SU:STA}$	–	0.6	–	–	μs
SDA setup time	$t_{SU:DAT}$	–	0.1	–	–	μs
SDA setup time (stop condition)	$t_{SU:STO}$	–	0.6	–	–	μs
Bus-free time	t_{BUF}	–	1.3	–	–	μs

*1: Only at the time of SYSCLK=16MHz or 24MHz



- Power-on and shutdown Procedures

  In case of power-on or shutdown of V_{DD}, the procedures and constraints are shown as following.



Power down/on and power on reset sequence

Note:

If V_{DDL} level is 100mV or more over, reset the IC by RESET_N pin after power-on.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL630Q464-01	Oct. 26. 2016	-	-	Final Edition

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