Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv10z128vlh7

Ordering Information [1]

Part Number	Memory		FlexCAN	Maximum number of I\O's
	Flash (KB)	SRAM (KB)		
MKV11Z128VLH7	128	16	Yes	54
MKV11Z128VLF7	128	16	Yes	40
MKV11Z128VLC7 [2]	128	16	Yes	28
MKV11Z128VFM7	128	16	Yes	28
MKV11Z64VLH7	64	16	Yes	54
MKV11Z64VLF7	64	16	Yes	40
MKV11Z64VLC7 [2]	64	16	Yes	28
MKV11Z64VFM7	64	16	Yes	28
MKV10Z64VLH7	64	16	No	54
MKV10Z64VLF7	64	16	No	40
MKV10Z64VLC7 [2]	64	16	No	28
MKV10Z64VFM7	128	16	No	28
MKV10Z128VLH7	128	16	No	54
MKV10Z128VLF7	128	16	No	40
MKV10Z128VLC7 [2]	128	16	No	28
MKV10Z128VFM7	128	16	No	28

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.
2. The 32-pin LQFP package supporting this part number is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit http://www.freescale.com/KPYW for more details.

Related Resources

Type	Description
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in package drawings.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	Digital pin input voltage (except open drain pins)	–0.3	VDD + 0.3[1]	V
	Open drain pins (PTC6 and PTC7)	–0.3	5.5	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum value of V_{IO} (except open drain pins) must be 3.8 V.

2 General

Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on freescale.com for guidelines on optimizing EMC performance.

- *AN2321: Designing for Board Level Electromagnetic Compatibility*
- *AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers*
- *AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers*
- *AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications*
- *AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

2.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad All port pins, except PTC6 and PTC7 • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –1.5 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
V_{OH}	Output high voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –6 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad All port pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	 — —	 0.5 0.5	 V V	
V_{OL}	Output low voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA	 — —	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	1
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	1
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	2

1. Measured at V_{DD} = 3.6 V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 75 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	
	• VLLS0 → RUN	—	123	132	µs	
	• VLLS1 → RUN	—	123	132	µs	
	• VLLS3 → RUN	—	67	72	µs	
	• VLPS → RUN	—	4	5	µs	
	• STOP → RUN	—	4	5	µs	

2.2.5 KV11x Power consumption operating behaviors

Table 5. KV11x power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	5	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					Target IDD
	• at 1.8 V 50 MHz (25 MHz Bus)	—	5.3	6.2	mA	
	• at 3.0 V 50 MHz (25 MHz Bus)	—	5.4	6.3	mA	
	• at 1.8 V 75 MHz (25 MHz Bus)	—	7.2	8.3	mA	
	• at 3.0 V 75 MHz (25 MHz Bus)	—	7.3	8.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					Target IDD

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{FTM}	FTM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.							µA
	MCGIRCLK (4 MHz internal reference clock)	150	150	150	150	150	150	
	OSCERCLK (4 MHz external crystal)	300	300	300	320	340	350	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA
I_{WDOG}	WDOG peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode (except for 75 MHz which is in FEE mode), and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

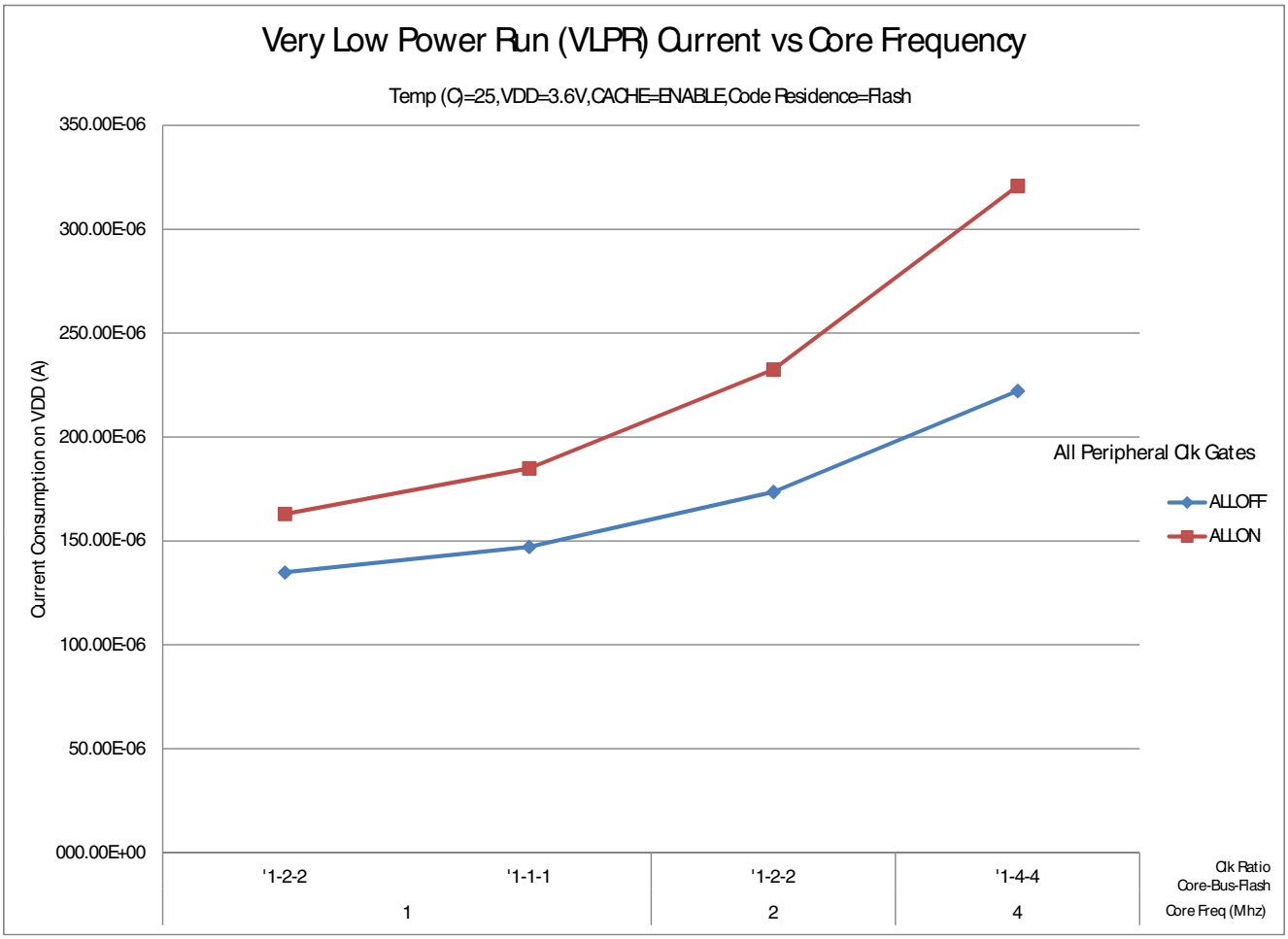

Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	15	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	17	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	12	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	4	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code.

2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 13. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	 0	 25	 MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	 20	 —	 ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

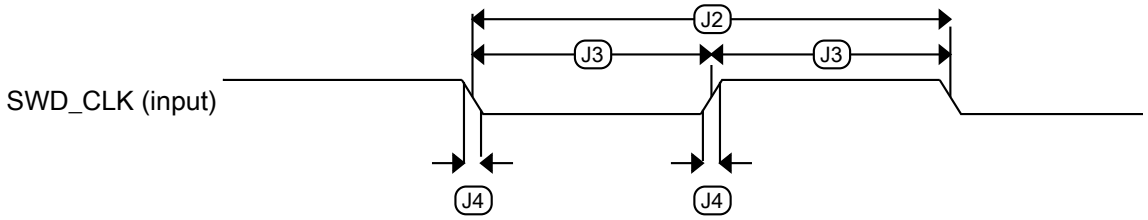

Figure 5. Serial wire clock input timing

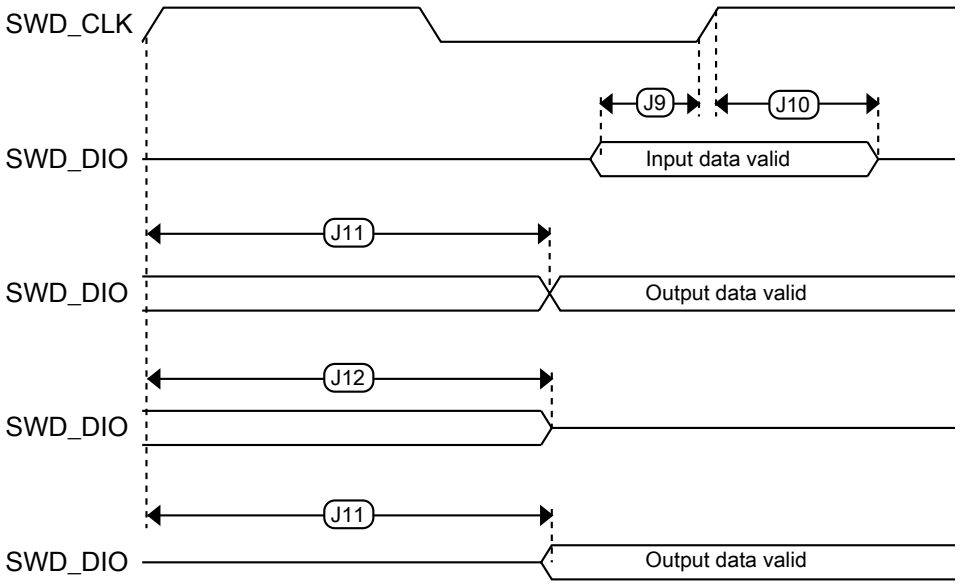

Figure 6. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1

Table continues on the next page...

Table 16. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	500	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 17. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 18. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	100	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	140	1150	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 19. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	12.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	8.0	mA

3.4.1.4 Reliability specifications

Table 20. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

Table 22. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
		• Avg = 32 16-bit single-ended mode • Avg = 32	78	92	—	dB	
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

Table 23. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	35	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	100	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to V_{DD} – 0.7 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

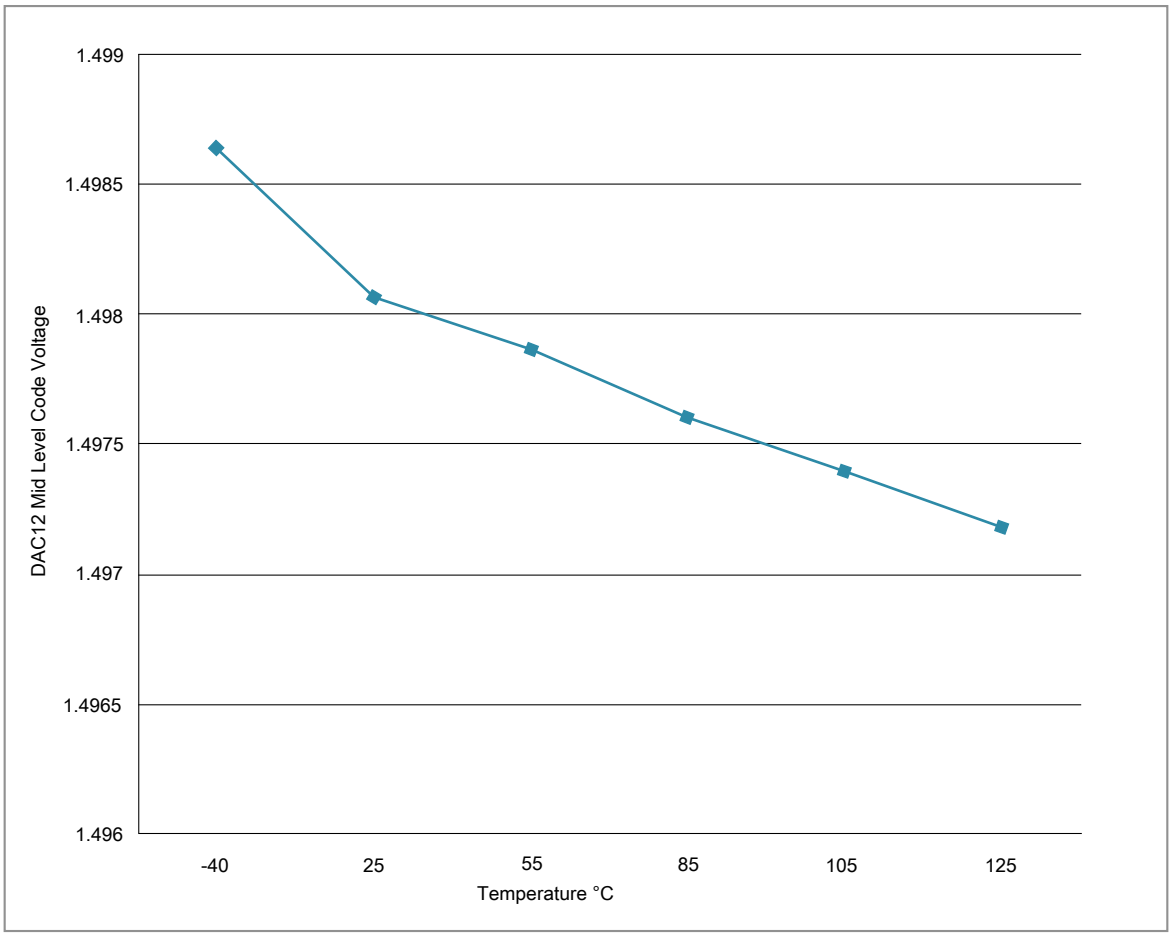

Figure 13. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

Table 27. Slave mode DSPI timing (limited voltage range) (continued)

Symbol	Description	Min.	Max.	Unit	Notes
DS11	DSPI_SCK to DSPI_SOUT valid	–	27	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	–	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.2	–	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	–	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	–	15	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	–	21	ns	
	Frequency of operation	–	**18.75**	**MHz**	4
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	2
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	–	17	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	–	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.2	–	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	–	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	–	15	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	–	11	ns	

1. Normal pads
2. The SPI module is clocked by the system clock
3. Open Drain pads: SIN: PTC7, SOUT:PTC6
4. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

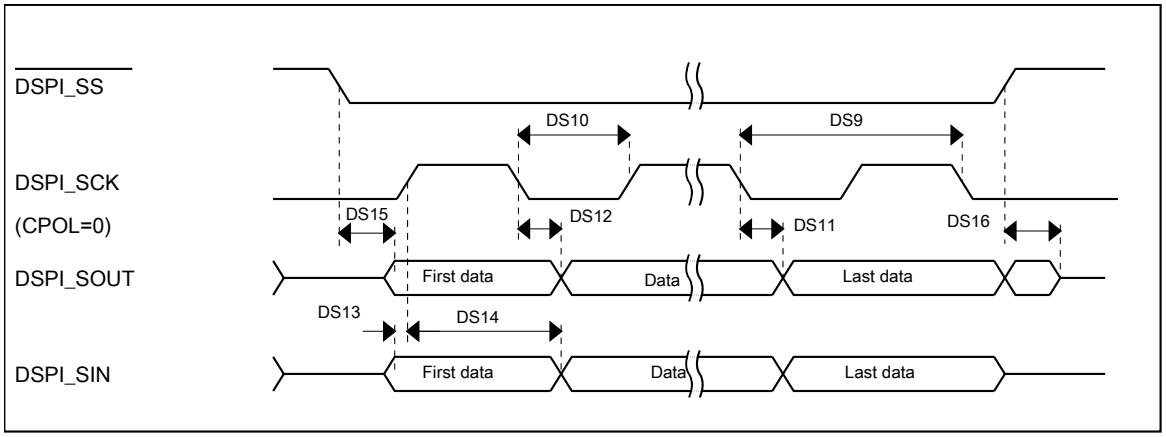

Figure 15. DSPI classic SPI timing — slave mode

3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 28. Master mode DSPI timing (full voltage range)

Symbol	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.7	3.6	V	1
	Frequency of operation	–	**18.75**	**MHz**	2
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	10		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	
	Frequency of operation	–	**18.75**	**MHz**	6
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	26		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	

Table continues on the next page...

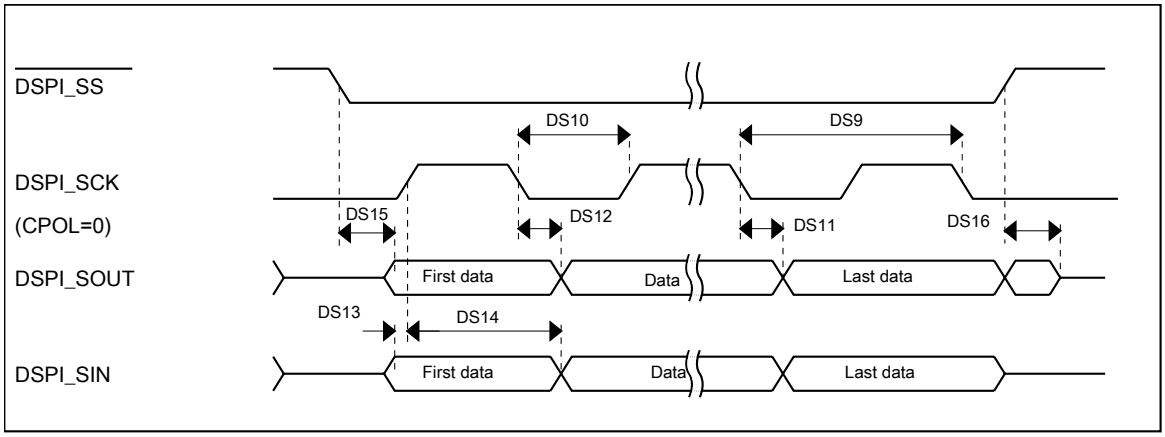

Figure 17. DSPI classic SPI timing — slave mode

3.8.3 I²C

See General switching specifications.

3.8.4 UART

See General switching specifications.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00473D
32-pin LQFP [1]	98ASH70029A
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W

1. The 32-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit http://www.freescale.com/KPYW for more details.

64 LQFP	48 QFP	32 QFN	32 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
14	10	—	—	VREFH	VREFH	VREFH							
15	11	—	—	VREFL	VREFL	VREFL							
16	12	—	—	VSSA	VSSA	VSSA							
17	13	—	—	PTE29	CMP1_IN5/ CMP0_IN5	CMP1_IN5/ CMP0_IN5	PTE29		FTM0_CH2		FTM_ CLKIN0		
18	14	9	9	PTE30	ADC1_SE4/ CMP1_IN4/ DAC0_OUT	ADC1_SE4/ CMP1_IN4/ DAC0_OUT	PTE30		FTM0_CH3		FTM_ CLKIN1		
19	—	—	—	PTE31	ADC0_SE14/ CMP0_IN4	ADC0_SE14/ CMP0_IN4	PTE31						
20	15	10	10	PTE24	DISABLED		PTE24	CAN0_TX	FTM0_CH0		I2C0_SCL	EWM_OUT_ b	
21	16	11	11	PTE25/ LLWU_P21	DISABLED		PTE25/ LLWU_P21	CAN0_RX	FTM0_CH1		I2C0_SDA	EWM_IN	
22	17	12	12	PTA0	SWD_CLK	SWD_CLK	PTA0	UART0_ CTS_b	FTM0_CH5		EWM_IN		SWD_CLK
23	18	13	13	PTA1	DISABLED		PTA1	UART0_RX	FTM2_CH0	CMP0_OUT	FTM2_QD_ PHA	FTM1_CH1	FTM4_CH0
24	19	14	14	PTA2	DISABLED		PTA2	UART0_TX	FTM2_CH1	CMP1_OUT	FTM2_QD_ PHB	FTM1_CH0	FTM4_CH1
25	20	15	15	PTA3	SWD_DIO	SWD_DIO	PTA3	UART0_ RTS_b	FTM0_CH0	FTM2_FLT0	EWM_OUT_ b		SWD_DIO
26	21	16	16	PTA4/ LLWU_P3	NMI_b	NMI_b	PTA4/ LLWU_P3		FTM0_CH1	FTM4_FLT0	FTM0_FLT3		NMI_b
27	—	—	—	PTA5	DISABLED		PTA5		FTM0_CH2	FTM5_FLT0			
28	—	—	—	PTA12	DISABLED		PTA12	CAN0_TX	FTM1_CH0				FTM1_QD_ PHA
29	—	—	—	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1				FTM1_QD_ PHB
30	22	—	—	VDD	VDD	VDD							
31	23	—	—	VSS	VSS	VSS							
32	24	17	17	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_ CLKIN0		FTM3_CH2	
33	25	18	18	PTA19	XTAL0	XTAL0	PTA19	FTM0_FLT0	FTM1_FLT0	FTM_ CLKIN1		LPTMR0_ ALT1	
34	26	19	19	PTA20	RESET_b		PTA20						RESET_b
35	27	20	20	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8	ADC0_SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	UART0_RX
36	28	21	21	PTB1	ADC0_SE9/ ADC1_SE9	ADC0_SE9/ ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_ PHB	UART0_TX
37	29	—	—	PTB2	ADC0_SE10/ ADC1_SE10/ ADC1_DM2	ADC0_SE10/ ADC1_SE10/ ADC1_DM2	PTB2	I2C0_SCL	UART0_ RTS_b	FTM0_FLT1		FTM0_FLT3	
38	30	—	—	PTB3	ADC1_SE2/ ADC1_DP2	ADC1_SE2/ ADC1_DP2	PTB3	I2C0_SDA	UART0_ CTS_b			FTM0_FLT0	

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Document Number KV11P64M75
Revision 3, 06/2015