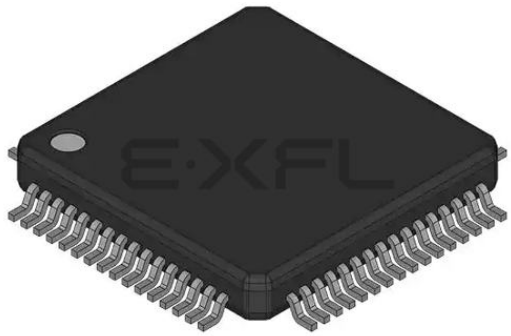


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv10z64vlh7

Ordering Information [1]

Part Number	Memory		FlexCAN	Maximum number of I\O's
	Flash (KB)	SRAM (KB)		
MKV11Z128VLH7	128	16	Yes	54
MKV11Z128VLF7	128	16	Yes	40
MKV11Z128VLC7 [2]	128	16	Yes	28
MKV11Z128VFM7	128	16	Yes	28
MKV11Z64VLH7	64	16	Yes	54
MKV11Z64VLF7	64	16	Yes	40
MKV11Z64VLC7 [2]	64	16	Yes	28
MKV11Z64VFM7	64	16	Yes	28
MKV10Z64VLH7	64	16	No	54
MKV10Z64VLF7	64	16	No	40
MKV10Z64VLC7 [2]	64	16	No	28
MKV10Z64VFM7	128	16	No	28
MKV10Z128VLH7	128	16	No	54
MKV10Z128VLF7	128	16	No	40
MKV10Z128VLC7 [2]	128	16	No	28
MKV10Z128VFM7	128	16	No	28

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.
2. The 32-pin LQFP package supporting this part number is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit http://www.freescale.com/KPYW for more details.

Related Resources

Type	Description
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in package drawings.

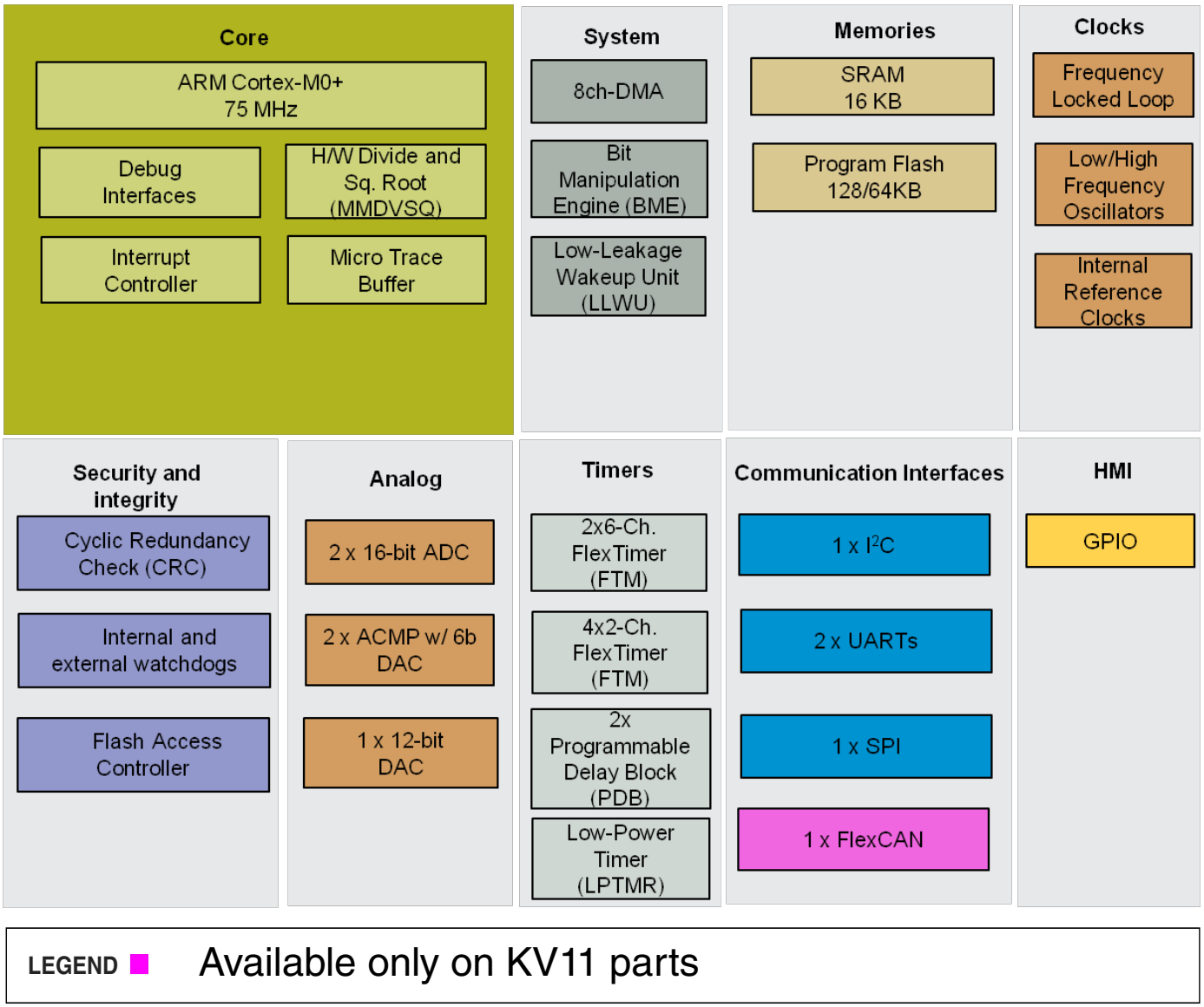


Figure 1. KV11 block diagram

Table of Contents

2.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad All port pins, except PTC6 and PTC7 • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –1.5 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
V_{OH}	Output high voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –6 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad All port pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	 — —	 0.5 0.5	 V V	
V_{OL}	Output low voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA	 — —	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	1
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	1
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	2

1. Measured at V_{DD} = 3.6 V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 75 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	
	• VLLS0 → RUN	—	123	132	µs	
	• VLLS1 → RUN	—	123	132	µs	
	• VLLS3 → RUN	—	67	72	µs	
	• VLPS → RUN	—	4	5	µs	
	• STOP → RUN	—	4	5	µs	

2.2.5 KV11x Power consumption operating behaviors

Table 5. KV11x power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	5	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					Target IDD
	• at 1.8 V 50 MHz (25 MHz Bus)	—	5.3	6.2	mA	
	• at 3.0 V 50 MHz (25 MHz Bus)	—	5.4	6.3	mA	
	• at 1.8 V 75 MHz (25 MHz Bus)	—	7.2	8.3	mA	
	• at 3.0 V 75 MHz (25 MHz Bus)	—	7.3	8.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					Target IDD

Table continues on the next page...

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FTM}	FTM clock	—	75	MHz	
VLPR mode					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz	

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time Fast slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 8 7	 ns ns	3
	Port rise and fall time Slow slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 15 25	 ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (low drive) is 25pF.

4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or there is a change from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 4 MHz	—	500	—	µA	
	• 8 MHz	—	600	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

3.4.1.2 Flash timing specifications — commands

Table 18. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	100	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	140	1150	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 19. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	12.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	8.0	mA

3.4.1.4 Reliability specifications

Table 20. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

Table 21. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

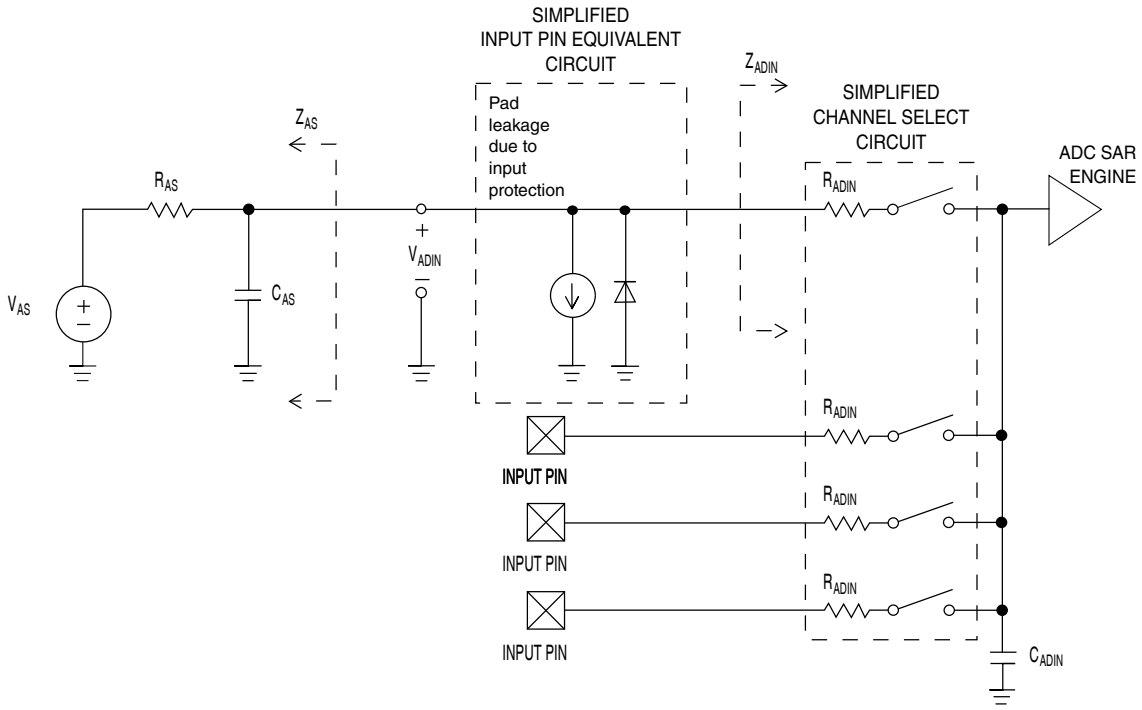


Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 22. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

Table 22. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.7 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 –97 –91	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode	82	100	—	dB	7

Table continues on the next page...

3.6.3.1 12-bit DAC operating requirements

Table 24. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.3.2 12-bit DAC operating behaviors

Table 25. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08)—high-speed mode	—	1	—	µs	1
	—low-power mode	—	—	5	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	

Table continues on the next page...

Table 26. Master mode DSPI timing (limited voltage range) (continued)

Symbol	Description	Min.	Max.	Unit	Notes
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	13	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	

1. Normal pads
2. The SPI module is clocked by the system clock
3. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
4. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].
5. Open Drain pads: SIN: PTC7, SOUT:PTC6
6. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

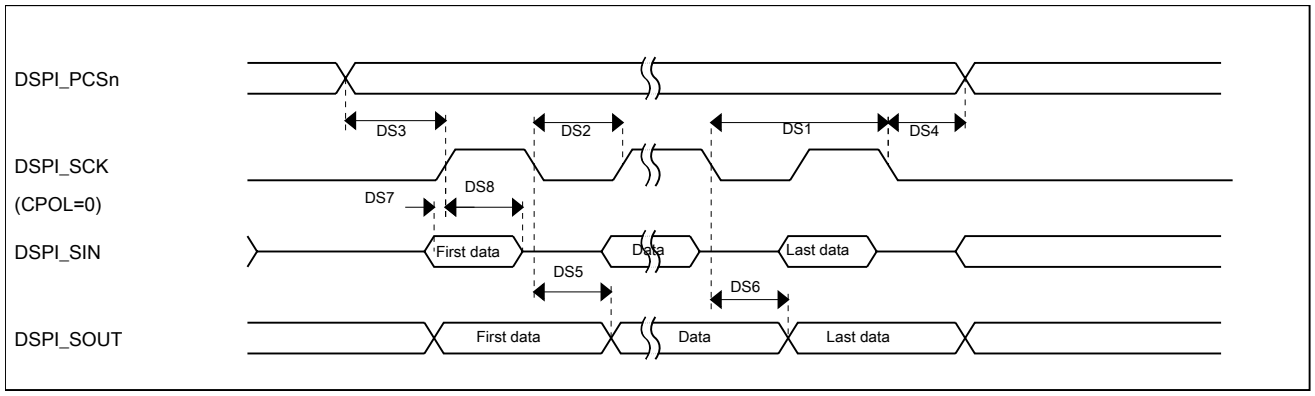


Figure 14. DSPI classic SPI timing — master mode

Table 27. Slave mode DSPI timing (limited voltage range)

Symbol	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	–	**12.5**	**MHz**	1
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	–	ns	2
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	–	21	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	–	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.2	–	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	–	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	–	15	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	–	15	ns	
	Frequency of operation	–	**12.5**	**MHz**	3
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	2
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	

Table continues on the next page...

3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 28. Master mode DSPI timing (full voltage range)

Symbol	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.7	3.6	V	1
	Frequency of operation	–	**18.75**	**MHz**	2
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	10		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	
	Frequency of operation	–	**18.75**	**MHz**	6
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	26		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	

Table continues on the next page...

Table 28. Master mode DSPI timing (full voltage range) (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Frequency of operation	–	**25**	**MHz**	7
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	10		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. Normal pads
3. The SPI module is clocked by the system clock
4. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
5. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC]
6. Open Drain pads: SIN: PTC7, SOUT:PTC6
7. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

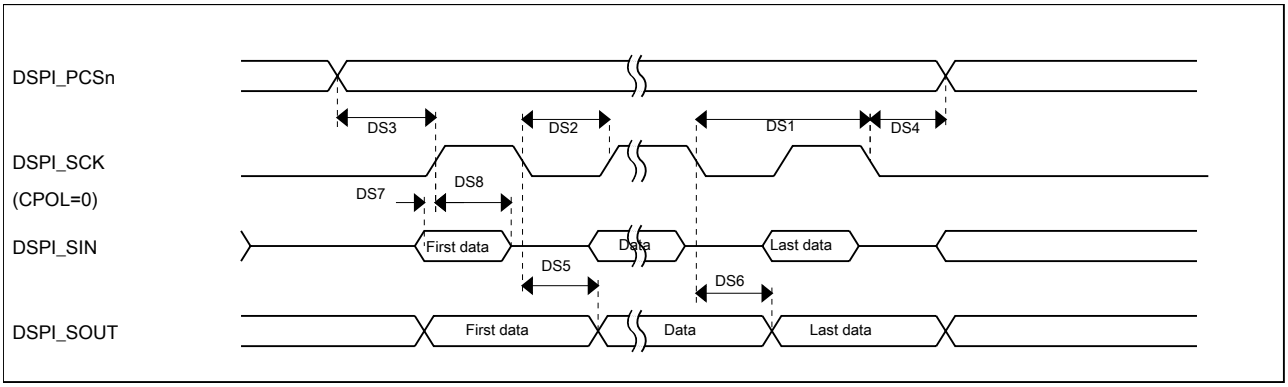


Figure 16. DSPI classic SPI timing — master mode

Table 29. Slave mode DSPI timing (full voltage range)

Symbol	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.7	3.6	V	
	Frequency of operation	–	**9.375**	**MHz**	1

Table continues on the next page...

64 LQFP	48 QFP	32 QFN	32 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
14	10	—	—	VREFH	VREFH	VREFH							
15	11	—	—	VREFL	VREFL	VREFL							
16	12	—	—	VSSA	VSSA	VSSA							
17	13	—	—	PTE29	CMP1_IN5/ CMP0_IN5	CMP1_IN5/ CMP0_IN5	PTE29		FTM0_CH2		FTM_ CLKIN0		
18	14	9	9	PTE30	ADC1_SE4/ CMP1_IN4/ DAC0_OUT	ADC1_SE4/ CMP1_IN4/ DAC0_OUT	PTE30		FTM0_CH3		FTM_ CLKIN1		
19	—	—	—	PTE31	ADC0_SE14/ CMP0_IN4	ADC0_SE14/ CMP0_IN4	PTE31						
20	15	10	10	PTE24	DISABLED		PTE24	CAN0_TX	FTM0_CH0		I2C0_SCL	EWM_OUT_ b	
21	16	11	11	PTE25/ LLWU_P21	DISABLED		PTE25/ LLWU_P21	CAN0_RX	FTM0_CH1		I2C0_SDA	EWM_IN	
22	17	12	12	PTA0	SWD_CLK	SWD_CLK	PTA0	UART0_ CTS_b	FTM0_CH5		EWM_IN		SWD_CLK
23	18	13	13	PTA1	DISABLED		PTA1	UART0_RX	FTM2_CH0	CMP0_OUT	FTM2_QD_ PHA	FTM1_CH1	FTM4_CH0
24	19	14	14	PTA2	DISABLED		PTA2	UART0_TX	FTM2_CH1	CMP1_OUT	FTM2_QD_ PHB	FTM1_CH0	FTM4_CH1
25	20	15	15	PTA3	SWD_DIO	SWD_DIO	PTA3	UART0_ RTS_b	FTM0_CH0	FTM2_FLT0	EWM_OUT_ b		SWD_DIO
26	21	16	16	PTA4/ LLWU_P3	NMI_b	NMI_b	PTA4/ LLWU_P3		FTM0_CH1	FTM4_FLT0	FTM0_FLT3		NMI_b
27	—	—	—	PTA5	DISABLED		PTA5		FTM0_CH2	FTM5_FLT0			
28	—	—	—	PTA12	DISABLED		PTA12	CAN0_TX	FTM1_CH0				FTM1_QD_ PHA
29	—	—	—	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1				FTM1_QD_ PHB
30	22	—	—	VDD	VDD	VDD							
31	23	—	—	VSS	VSS	VSS							
32	24	17	17	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_ CLKIN0		FTM3_CH2	
33	25	18	18	PTA19	XTAL0	XTAL0	PTA19	FTM0_FLT0	FTM1_FLT0	FTM_ CLKIN1		LPTMR0_ ALT1	
34	26	19	19	PTA20	RESET_b		PTA20						RESET_b
35	27	20	20	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8	ADC0_SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	UART0_RX
36	28	21	21	PTB1	ADC0_SE9/ ADC1_SE9	ADC0_SE9/ ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_ PHB	UART0_TX
37	29	—	—	PTB2	ADC0_SE10/ ADC1_SE10/ ADC1_DM2	ADC0_SE10/ ADC1_SE10/ ADC1_DM2	PTB2	I2C0_SCL	UART0_ RTS_b	FTM0_FLT1		FTM0_FLT3	
38	30	—	—	PTB3	ADC1_SE2/ ADC1_DP2	ADC1_SE2/ ADC1_DP2	PTB3	I2C0_SDA	UART0_ CTS_b			FTM0_FLT0	

64 LQFP	48 QFP	32 QFN	32 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
39	31	—	—	PTB16	DISABLED		PTB16		UART0_RX	FTM_ CLKIN2	CAN0_TX	EWM_IN	
40	32	—	—	PTB17	DISABLED		PTB17		UART0_TX	FTM_ CLKIN1	CAN0_RX	EWM_OUT_ b	
41	—	—	—	PTB18	DISABLED		PTB18	CAN0_TX		FTM3_CH2			
42	—	—	—	PTB19	DISABLED		PTB19	CAN0_RX		FTM3_CH3			
43	33	—	—	PTC0	ADC1_SE11	ADC1_SE11	PTC0	SPI0_PCS4	PDB_ EXTRG0		CMP0_OUT	FTM0_FLT0	SPI0_PCS0
44	34	22	22	PTC1/ LLWU_P6	ADC1_SE3	ADC1_SE3	PTC1/ LLWU_P6	SPI0_PCS3	UART1_ RTS_b	FTM0_CH0	FTM2_CH0		
45	35	23	23	PTC2	ADC0_SE11/ CMP1_IN0	ADC0_SE11/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_ CTS_b	FTM0_CH1	FTM2_CH1		
46	36	24	24	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0	
47	—	—	—	VSS	VSS	VSS							
48	—	—	—	VDD	VDD	VDD							
49	37	25	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	
50	38	26	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	FTM0_CH2
51	39	27	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB_ EXTRG1		UART0_RX		I2C0_SCL
52	40	28	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN			UART0_TX		I2C0_SDA
53	—	—	—	PTC8	ADC1_SE14/ CMP0_IN2	ADC1_SE14/ CMP0_IN2	PTC8		FTM3_CH4				
54	—	—	—	PTC9	ADC1_SE15/ CMP0_IN3	ADC1_SE15/ CMP0_IN3	PTC9		FTM3_CH5				
55	—	—	—	PTC10	ADC1_SE16	ADC1_SE16	PTC10		FTM5_CH0	FTM5_QD_ PHA			
56	—	—	—	PTC11/ LLWU_P11	ADC1_SE17	ADC1_SE17	PTC11/ LLWU_P11		FTM5_CH1	FTM5_QD_ PHB			
57	41	—	—	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART0_ CTS_b	FTM0_CH0	UART1_RX	FTM3_CH0	
58	42	—	—	PTD1	ADC0_SE2	ADC0_SE2	PTD1	SPI0_SCK	UART0_ RTS_b	FTM0_CH1	UART1_TX	FTM3_CH1	
59	43	—	—	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART0_RX	FTM0_CH2		FTM3_CH2	I2C0_SCL
60	44	—	—	PTD3	DISABLED		PTD3	SPI0_SIN	UART0_TX	FTM0_CH3		FTM3_CH3	I2C0_SDA
61	45	29	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_ RTS_b	FTM0_CH4	FTM2_CH0	EWM_IN	SPI0_PCS0
62	46	30	30	PTD5	ADC0_SE3	ADC0_SE3	PTD5	SPI0_PCS2	UART0_ CTS_b	FTM0_CH5	FTM2_CH1	EWM_OUT_ b	SPI0_SCK
63	47	31	31	PTD6/ LLWU_P15	ADC1_SE6	ADC1_SE6	PTD6/ LLWU_P15	FTM4_CH0	UART0_RX	FTM0_CH0	FTM1_CH0	FTM0_FLT0	SPI0_SOUT
64	48	32	32	PTD7	DISABLED		PTD7	FTM4_CH1	UART0_TX	FTM0_CH1	FTM1_CH1	FTM0_FLT1	SPI0_SIN

5.2 KV11 Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

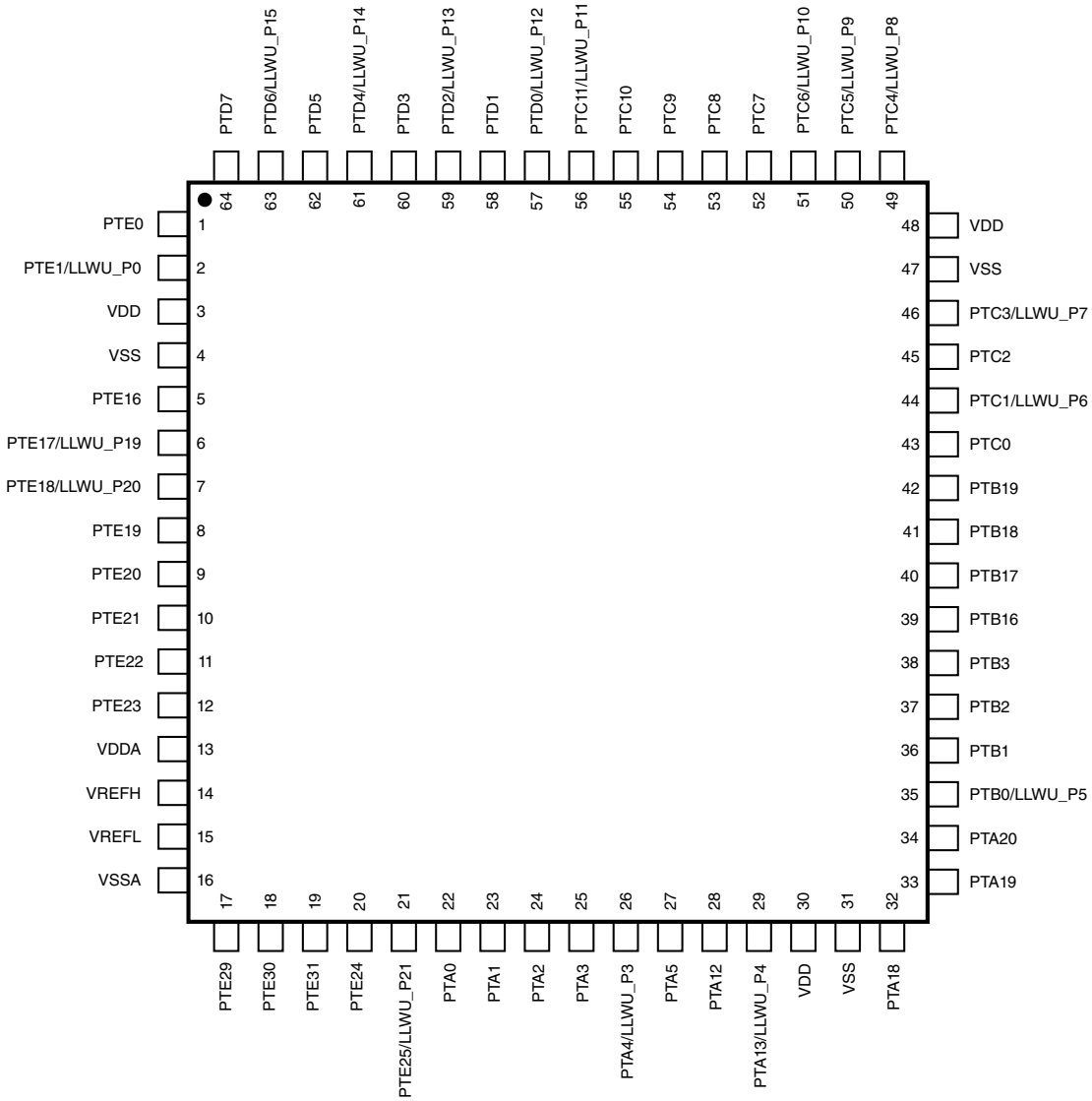


Figure 18. 64 LQFP Pinout Diagram

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

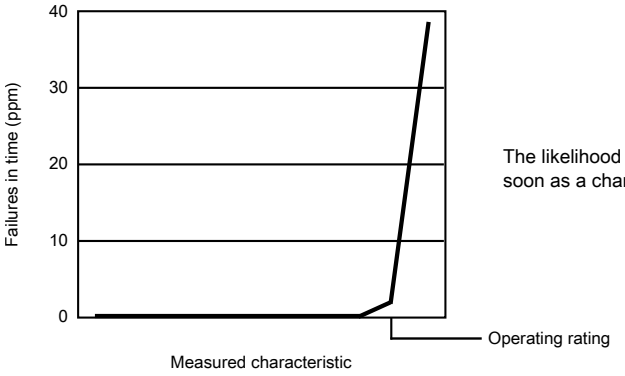
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

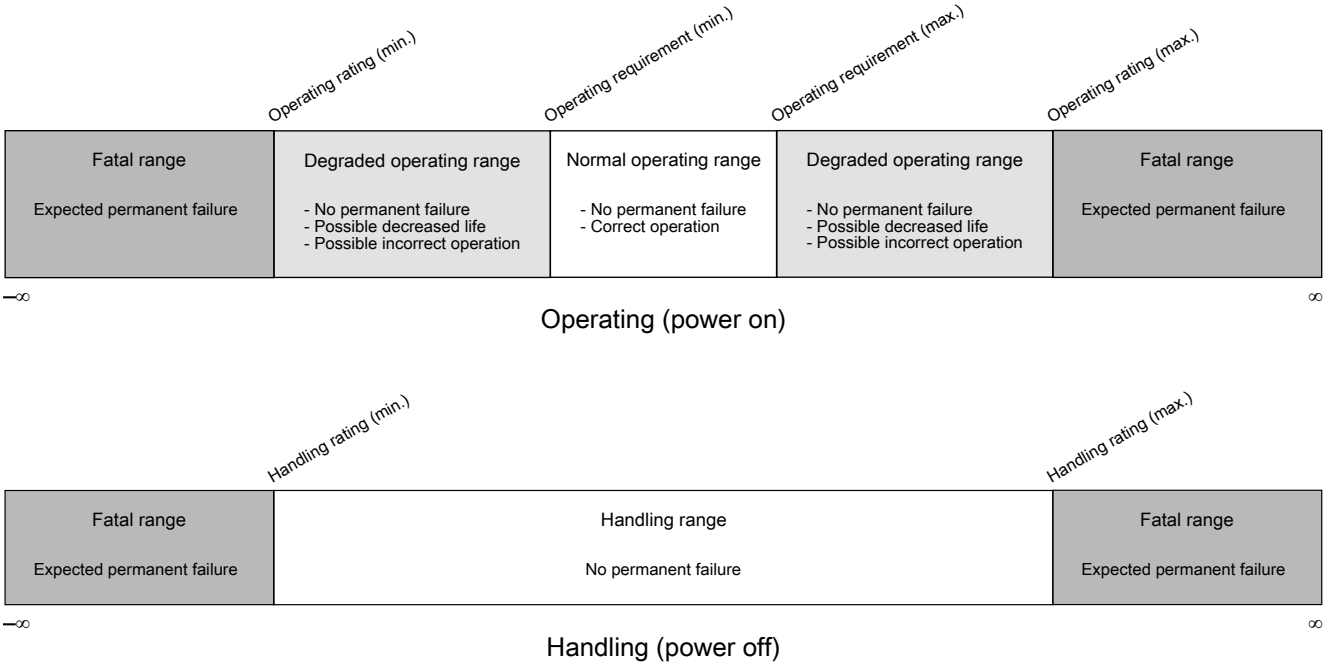
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

8.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Document Number KV11P64M75
Revision 3, 06/2015