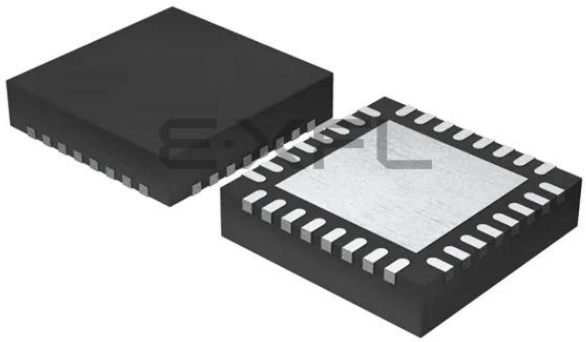

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	28
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv11z128vfm7

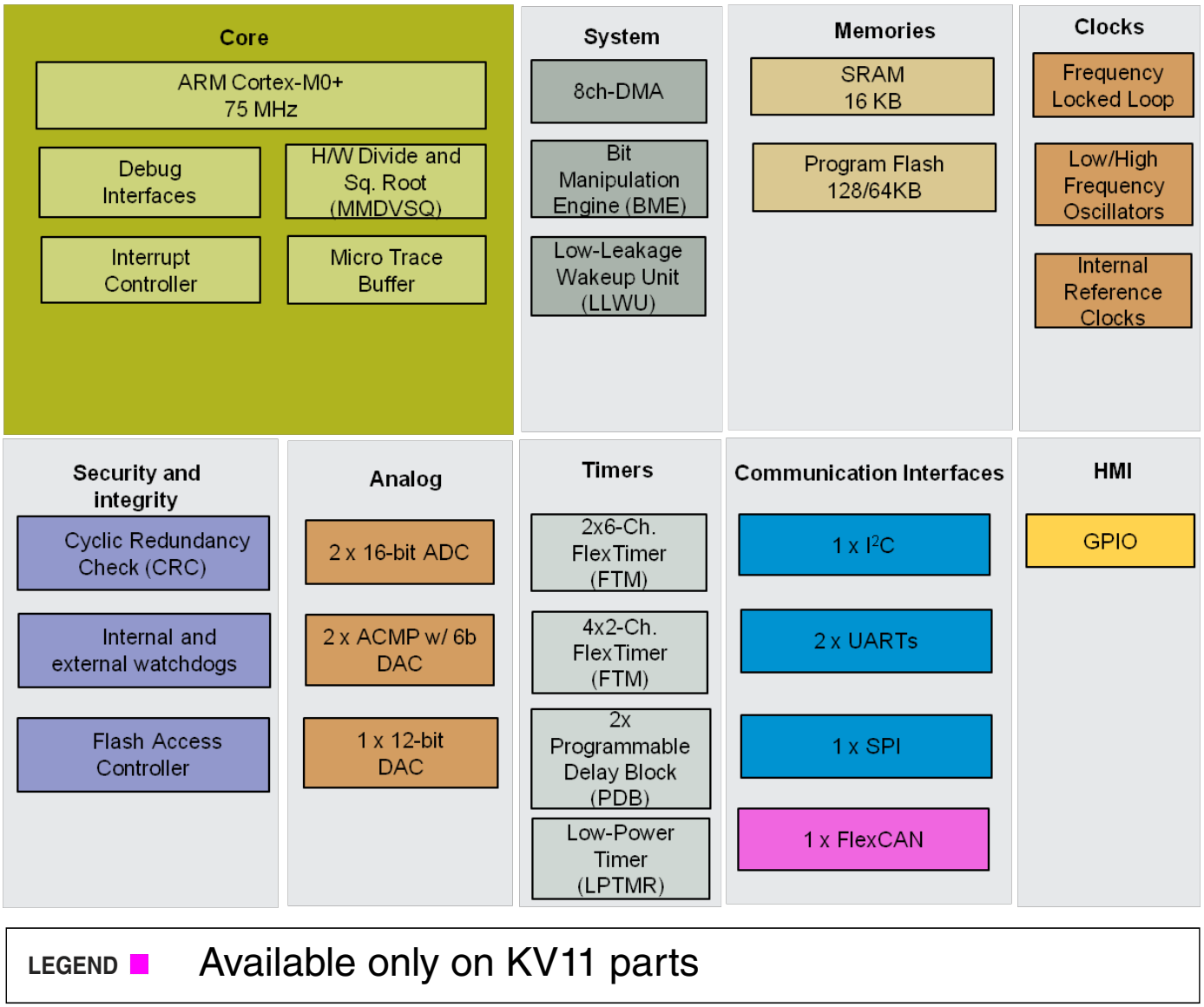

Figure 1. KV11 block diagram

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human-body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

1.4 Voltage and current operating ratings

Table 5. KV11x power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 1.8 V 50 MHz	—	8.5	9.7	mA	
	• at 3.0 V 50 MHz	—	8.5	9.8	mA	
	• at 1.8 V 75 MHz	—	11.6	13.0	mA	
	• at 3.0 V 75 MHz	—	11.7	13.2	mA	
I_{DD_WAIT}	Wait mode high frequency 75 MHz current at 3.0 V — all peripheral clocks disabled	—	4	—	mA	—
I_{DD_WAIT}	Wait mode reduced frequency 50 MHz current at 3.0 V — all peripheral clocks disabled	—	3.4	—	mA	—
I_{DD_VLPR}	Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks disabled	—	268	—	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPR}	Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks enabled	—	437	—	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPW}	Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks enabled	—	348.9	—	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPW}	Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks disabled	—	173.4	—	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_STOP}	Stop mode current at 3.0 V					—
	• -40 °C to 25 °C	—	248	286	µA	
	• at 50 °C	—	269	—		
	• at 70 °C	—	290	—		
	• at 85 °C	—	319	—		
	• at 105 °C	—	386	—		
I_{DD_VLPS}	Very-Low-Power Stop mode current at 3.0 V					—
	• -40 °C to 25 °C	—	1.9	—	µA	
	• at 50 °C	—	6	—		
	• at 70 °C	—	12.7	—		
	• at 85 °C	—	23.5	—		
	• at 105 °C	—	47.6	—		
I_{DD_VLLS3}	Very-Low-Leakage Stop mode 3 current at 3.0 V				µA	—
	• -40 °C to 25 °C	—	1.24	—		
	• at 50 °C	—	1.9	—		
	• at 70 °C	—	3.4	—		
		—	5.7	—		

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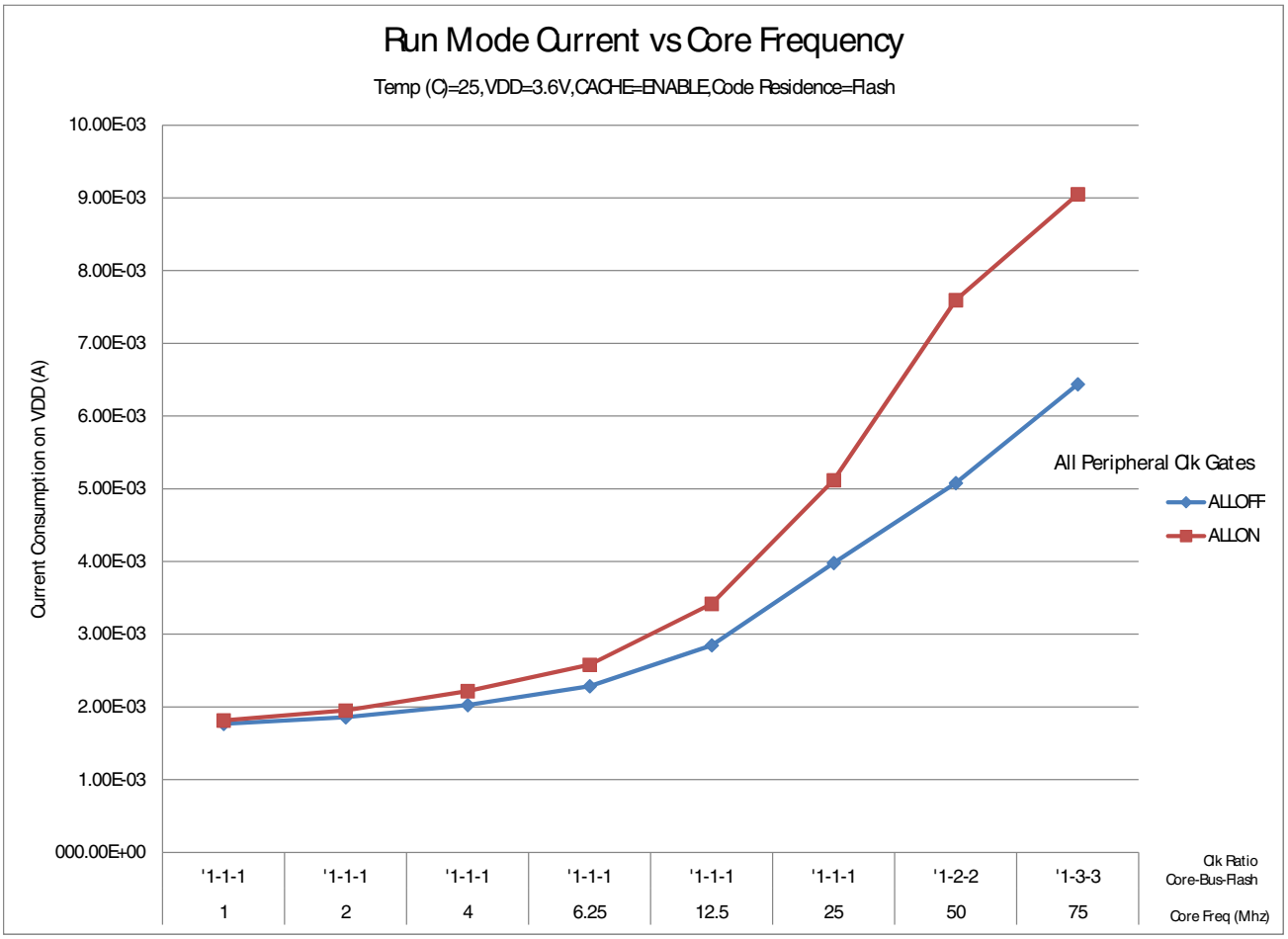


Figure 3. Run mode supply current vs. core frequency

Table 14. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	±2	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C		—	± 0.4	± 1.5	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	$\%f_{intf\_ft}$	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00, DMX32 = 0) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01, DMX32 = 0) 1280 × f_{fll_ref}	40	41.94	48	MHz	
		Mid range (DRS = 10, DMX32 = 0) 1920 x f_{fll_ref}	60	62.915	75	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00, DMX32 = 1) 732 × f_{fll_ref}	—	23.99	—	MHz	5 6
		Mid range (DRS = 01, DMX32 = 1) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid range (DRS = 10, DMX32 = 1) 2197 × f_{fll_ref}	–	71.991	–	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 75 MHz		—	180	—	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft}.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.

4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or there is a change from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 4 MHz	—	500	—	µA	
	• 8 MHz	—	600	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50 48	MHz	1, 2

Table continues on the next page...

Table 16. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	500	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 17. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

3.6.1.1 16-bit ADC operating conditions

Table 21. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 * VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	1200	Ksps	5

Table continues on the next page...

Table 22. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.7 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 –97 –91	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode	82	100	—	dB	7

Table continues on the next page...

Table 23. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	35	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	100	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to V_{DD} – 0.7 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

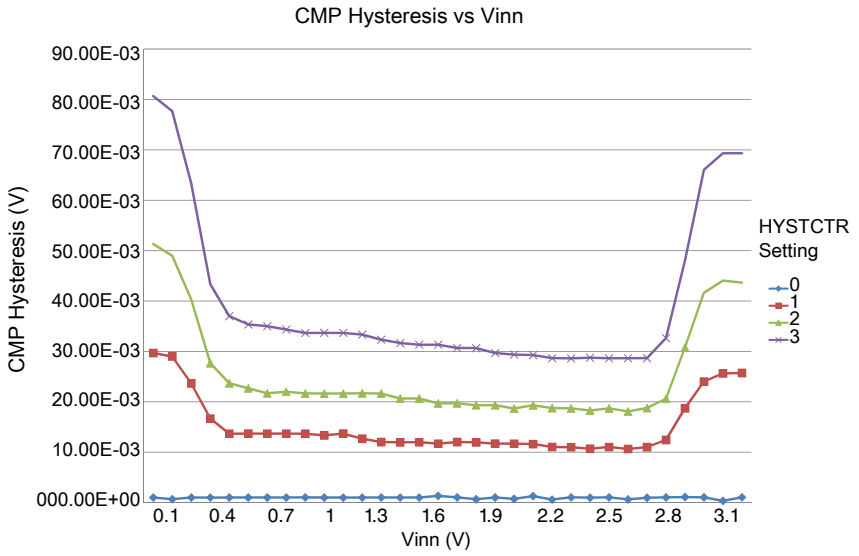


Figure 10. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

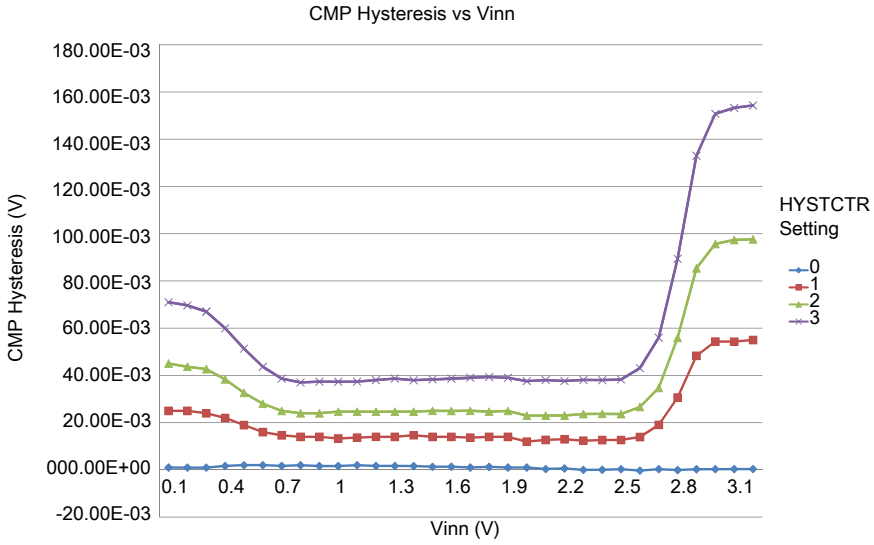


Figure 11. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

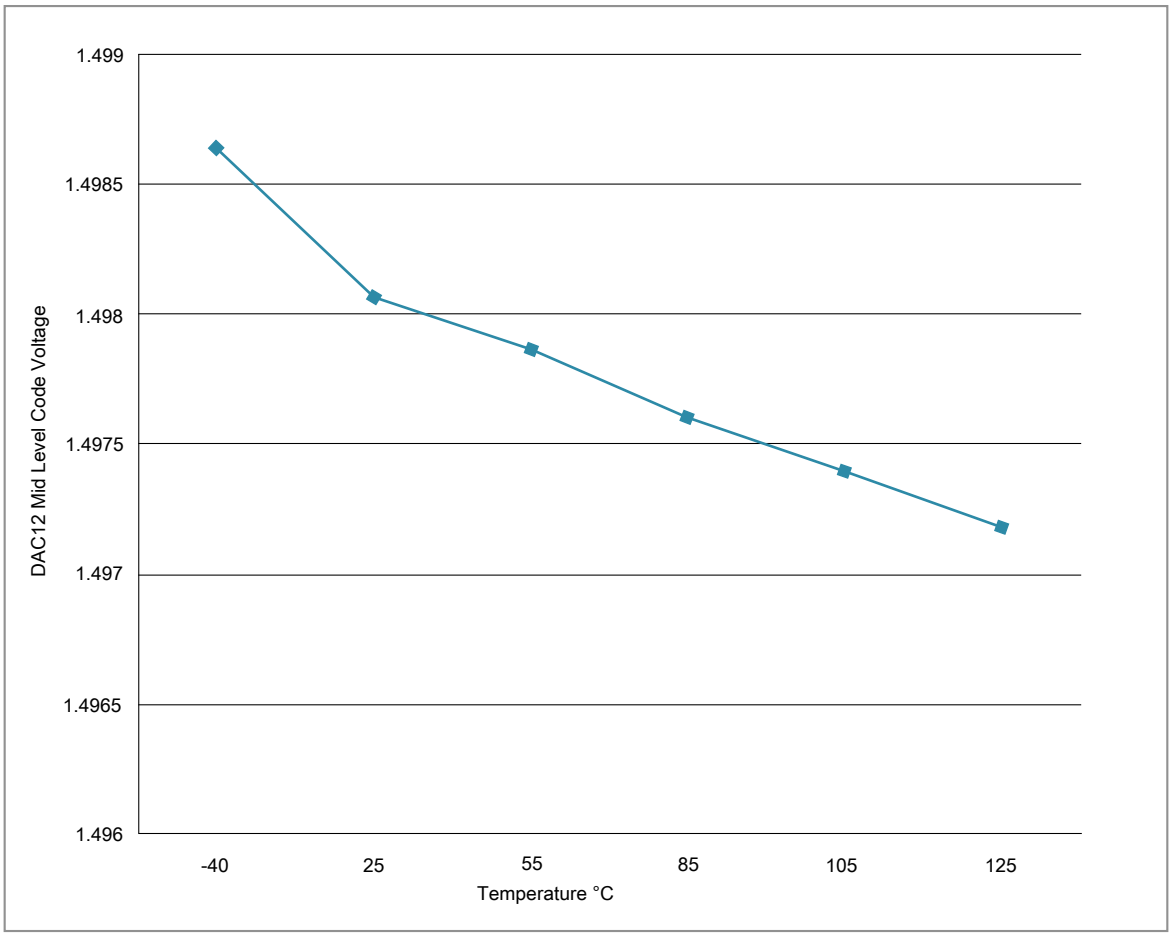


Figure 13. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

Table 26. Master mode DSPI timing (limited voltage range) (continued)

Symbol	Description	Min.	Max.	Unit	Notes
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	13	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	

1. Normal pads
2. The SPI module is clocked by the system clock
3. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
4. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].
5. Open Drain pads: SIN: PTC7, SOUT:PTC6
6. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

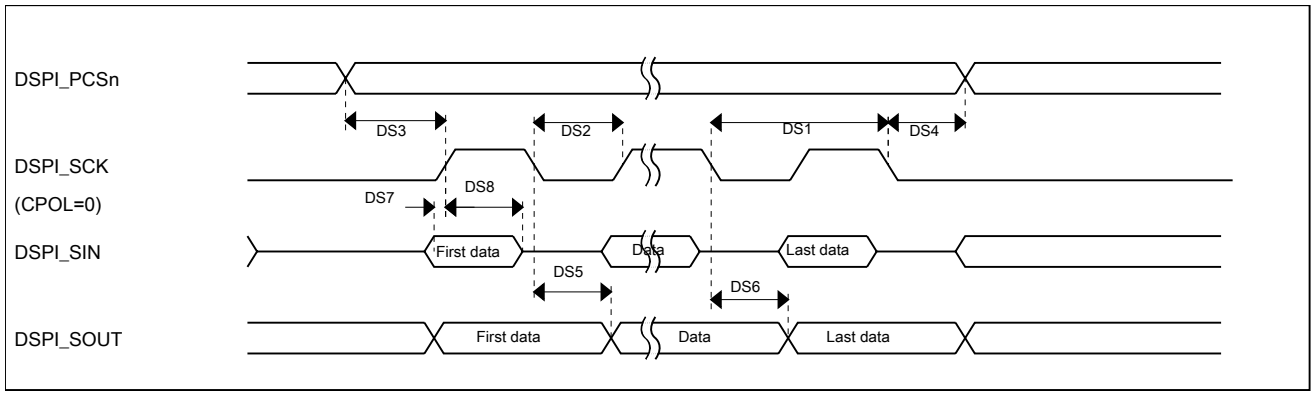


Figure 14. DSPI classic SPI timing — master mode

Table 27. Slave mode DSPI timing (limited voltage range)

Symbol	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	–	**12.5**	**MHz**	1
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	–	ns	2
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	–	21	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	–	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.2	–	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	–	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	–	15	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	–	15	ns	
	Frequency of operation	–	**12.5**	**MHz**	3
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	2
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	

Table continues on the next page...

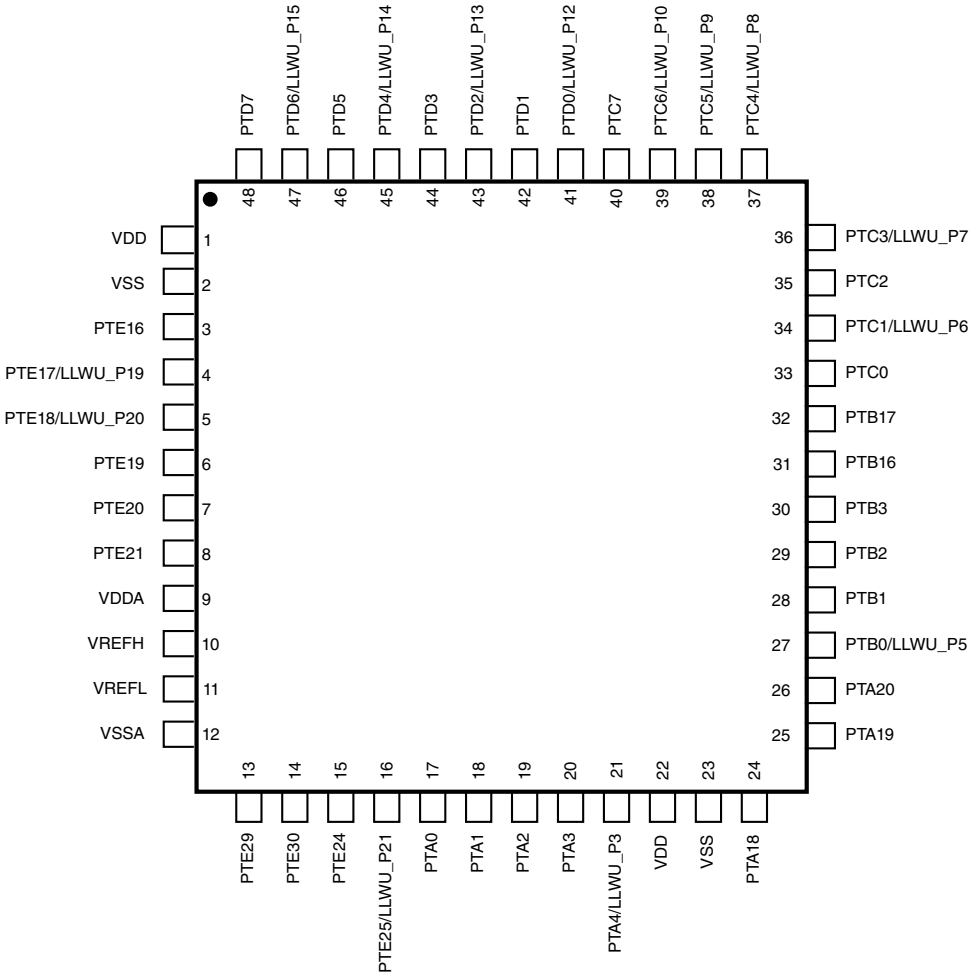


Figure 19. 48 QFP Pinout Diagram

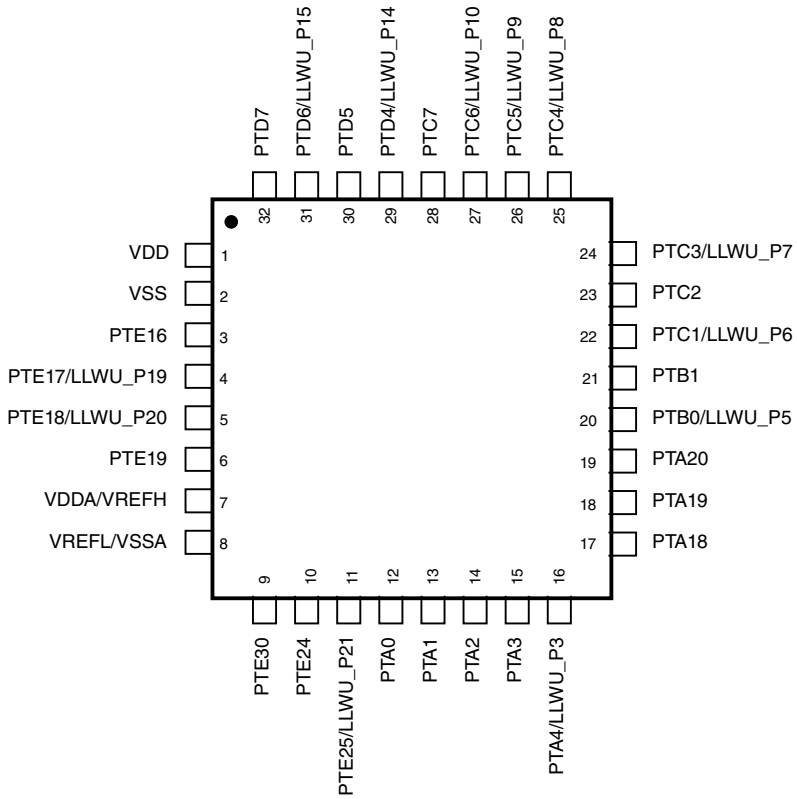


Figure 20. 32 LQFP Pinout Diagram

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

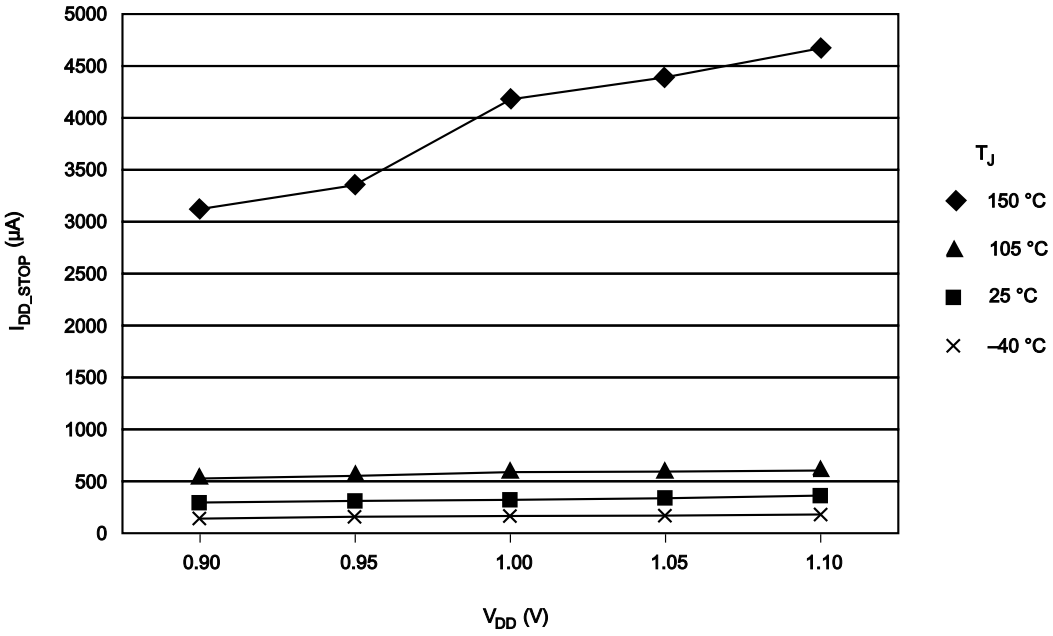
8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA



8.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 30. Revision history

Rev. No.	Date	Substantial Changes
0	11/2014	Initial Prelim release.
1	02/2015	Updated the following sections: • DSPI switching specifications (limited voltage range) • DSPI switching specifications (full voltage range) • KV11 Signal Multiplexing and Pin Assignments

Table continues on the next page...

Table 30. Revision history (continued)

Rev. No.	Date	Substantial Changes
2	04/2015	Updated the following sections: • Power mode transition operating behaviors • Power consumption operating behaviors • 16-bit ADC operating conditions • Fields • Updated the table "16-bit ADC electrical characteristics" with a footnote • Added the figure "Run mode supply current vs. core frequency" to the section "Diagram: Typical IDD_RUN operating behavior"
3	06/2015	• Added a footnote to the ambient temperature entry in the table "Thermal operating requirements"