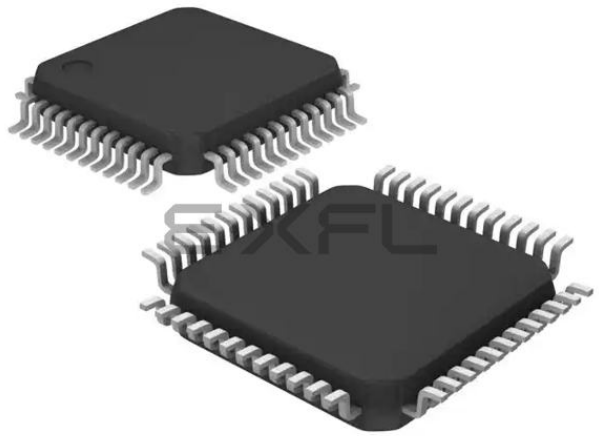

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
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Peripherals	DMA, LVD, POR, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv11z64vlf7

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human-body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

1.4 Voltage and current operating ratings

Table 5. KV11x power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 1.8 V 50 MHz	—	8.5	9.7	mA	
	• at 3.0 V 50 MHz	—	8.5	9.8	mA	
	• at 1.8 V 75 MHz	—	11.6	13.0	mA	
	• at 3.0 V 75 MHz	—	11.7	13.2	mA	
I_{DD_WAIT}	Wait mode high frequency 75 MHz current at 3.0 V — all peripheral clocks disabled	—	4	—	mA	—
I_{DD_WAIT}	Wait mode reduced frequency 50 MHz current at 3.0 V — all peripheral clocks disabled	—	3.4	—	mA	—
I_{DD_VLPR}	Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks disabled	—	268	—	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPR}	Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks enabled	—	437	—	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPW}	Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks enabled	—	348.9	—	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_VLPW}	Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks disabled	—	173.4	—	µA	4 MHz CPU speed, 1 MHz bus speed.
I_{DD_STOP}	Stop mode current at 3.0 V					—
	• -40 °C to 25 °C	—	248	286	µA	
	• at 50 °C	—	269	—		
	• at 70 °C	—	290	—		
	• at 85 °C	—	319	—		
	• at 105 °C	—	386	—		
I_{DD_VLPS}	Very-Low-Power Stop mode current at 3.0 V					—
	• -40 °C to 25 °C	—	1.9	—	µA	
	• at 50 °C	—	6	—		
	• at 70 °C	—	12.7	—		
	• at 85 °C	—	23.5	—		
	• at 105 °C	—	47.6	—		
I_{DD_VLLS3}	Very-Low-Leakage Stop mode 3 current at 3.0 V				µA	—
	• -40 °C to 25 °C	—	1.24	—		
	• at 50 °C	—	1.9	—		
	• at 70 °C	—	3.4	—		
		—	5.7	—		

Table continues on the next page...

Table 5. KV11x power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 85 °C • at 105 °C	—	11.3	—		
I_{DD_VLLS1}	Very-Low-Leakage Stop mode 1 current at 3.0 V • -40°C to 25°C • at 50°C • at 70°C • at 85°C • at 105°C	 — — — — —	 0.746 0.8 1.5 2.7 5.9	 — — — — —	µA	—
I_{DD_VLLS0}	Very-Low-Leakage Stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V • -40 °C to 25 °C • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 0.273 0.515 1.2 2.39 5.59	 — — — — —	µA	—
I_{DD_VLLS0}	Very-Low-Leakage Stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V • -40 °C to 25 °C • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 0.14 0.34 1.02 2.21 5.41	 — — — — —	µA	2

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. No brownout

Table 6. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{FTM}	FTM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.							µA
	MCGIRCLK (4 MHz internal reference clock)	150	150	150	150	150	150	
	OSCERCLK (4 MHz external crystal)	300	300	300	320	340	350	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA
I_{WDOG}	WDOG peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode (except for 75 MHz which is in FEE mode), and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 75 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	48	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FLASH}	Flash clock	—	24	MHz	
f_{LPTMR}	LPTMR clock	—	24	MHz	
High Speed run mode					
f_{SYS}	System and core clock	—	75	MHz	
f_{BUS}	Bus clock	—	25	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	

Table continues on the next page...

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FTM}	FTM clock	—	75	MHz	
VLPR mode					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz	

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time Fast slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 8 7	 ns ns	3
	Port rise and fall time Slow slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 15 25	 ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (low drive) is 25pF.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature [1]	–40	105	°C

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 12. Thermal attributes

Board type	Symbol	Description	64 LQFP	48 LQFP	32 LQFP	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	64	81	85	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	57	57	34	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	68	72	82	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	51	50	28	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	28	35	33	14	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	25	25	2.5	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	7	7	8	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.

Table 14. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	±2	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C		—	± 0.4	± 1.5	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	$\%f_{intf\_ft}$	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00, DMX32 = 0) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01, DMX32 = 0) 1280 × f_{fll_ref}	40	41.94	48	MHz	
		Mid range (DRS = 10, DMX32 = 0) 1920 x f_{fll_ref}	60	62.915	75	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00, DMX32 = 1) 732 × f_{fll_ref}	—	23.99	—	MHz	5 6
		Mid range (DRS = 01, DMX32 = 1) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid range (DRS = 10, DMX32 = 1) 2197 × f_{fll_ref}	–	71.991	–	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 75 MHz		—	180	—	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft}.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50 48	MHz	1, 2

Table continues on the next page...

3.4.1.2 Flash timing specifications — commands

Table 18. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	100	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	140	1150	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 19. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	12.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	8.0	mA

3.4.1.4 Reliability specifications

Table 20. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

3.6.1.1 16-bit ADC operating conditions

Table 21. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 * VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	1200	Ksps	5

Table continues on the next page...

Table 22. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.7 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 –97 –91	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode	82	100	—	dB	7

Table continues on the next page...

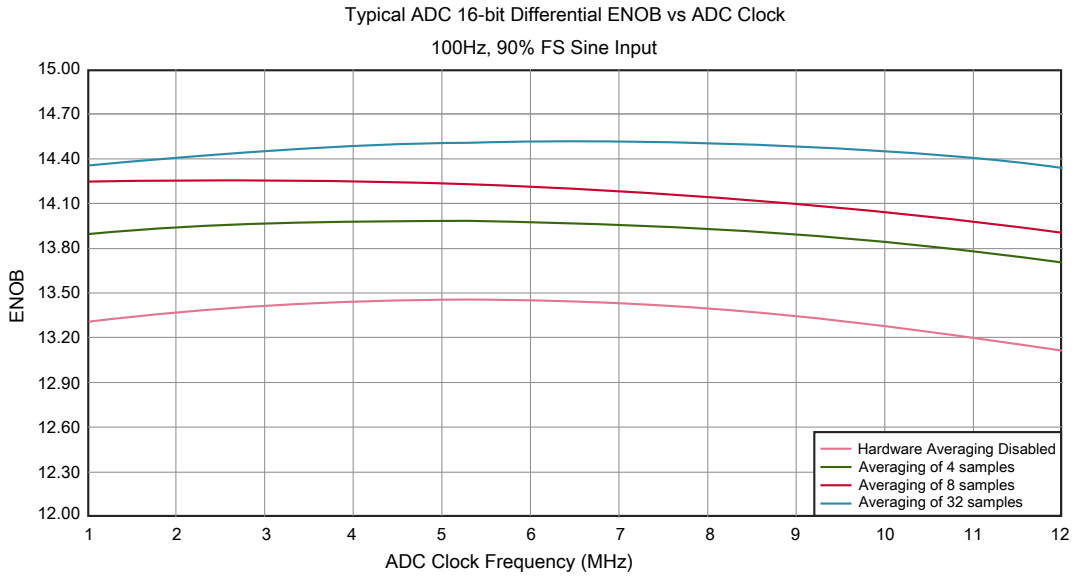

Figure 8. Typical ENOB vs. ADC_CLK for 16-bit differential mode

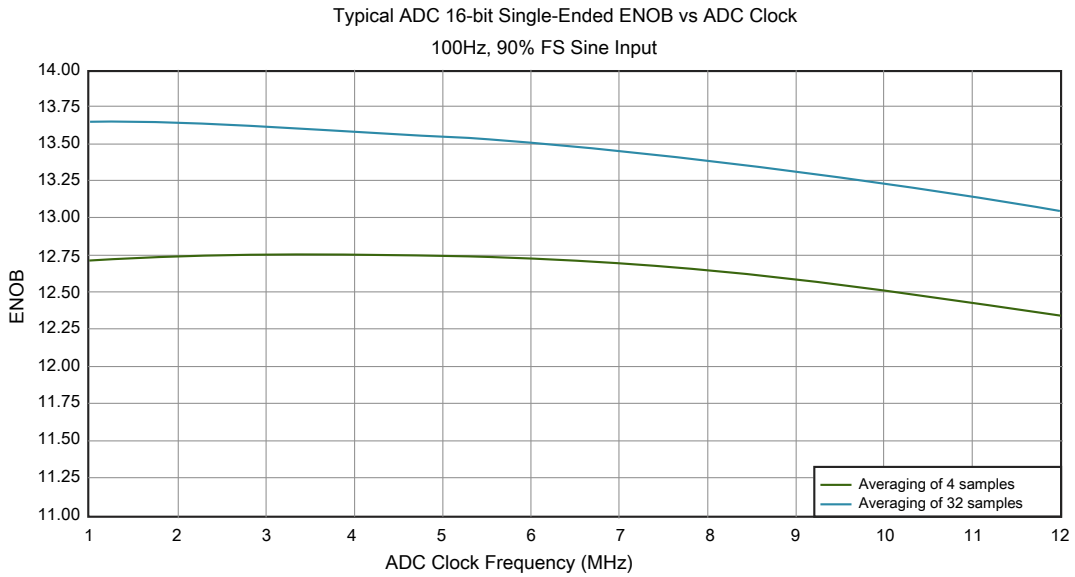

Figure 9. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 23. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V

Table continues on the next page...

3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 28. Master mode DSPI timing (full voltage range)

Symbol	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.7	3.6	V	1
	Frequency of operation	–	**18.75**	**MHz**	2
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	10		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	
	Frequency of operation	–	**18.75**	**MHz**	6
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	26		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	

Table continues on the next page...

Table 29. Slave mode DSPI timing (full voltage range) (continued)

Symbol	Description	Min.	Max.	Unit	Notes
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	2
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	–	27.8	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	–	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.7	–	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	–	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	–	22	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	–	22	ns	
	Frequency of operation	–	**9.375**	**MHz**	3
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	2
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	–	43.8	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	–	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.7	–	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	–	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	–	22	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	–	38	ns	
	Frequency of operation		**12.5**	**MHz**	4
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	2
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	–	20.8	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	–	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.7	–	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	–	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	–	22	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	–	15	ns	

1. Normal pads
2. The SPI module is clocked by the system clock
3. Open Drain pads: SIN: PTC7, SOUT:PTC6
4. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

64 LQFP	48 QFP	32 QFN	32 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
39	31	—	—	PTB16	DISABLED		PTB16		UART0_RX	FTM_ CLKIN2	CAN0_TX	EWM_IN	
40	32	—	—	PTB17	DISABLED		PTB17		UART0_TX	FTM_ CLKIN1	CAN0_RX	EWM_OUT_ b	
41	—	—	—	PTB18	DISABLED		PTB18	CAN0_TX		FTM3_CH2			
42	—	—	—	PTB19	DISABLED		PTB19	CAN0_RX		FTM3_CH3			
43	33	—	—	PTC0	ADC1_SE11	ADC1_SE11	PTC0	SPI0_PCS4	PDB_ EXTRG0		CMP0_OUT	FTM0_FLT0	SPI0_PCS0
44	34	22	22	PTC1/ LLWU_P6	ADC1_SE3	ADC1_SE3	PTC1/ LLWU_P6	SPI0_PCS3	UART1_ RTS_b	FTM0_CH0	FTM2_CH0		
45	35	23	23	PTC2	ADC0_SE11/ CMP1_IN0	ADC0_SE11/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_ CTS_b	FTM0_CH1	FTM2_CH1		
46	36	24	24	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0	
47	—	—	—	VSS	VSS	VSS							
48	—	—	—	VDD	VDD	VDD							
49	37	25	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	
50	38	26	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	FTM0_CH2
51	39	27	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB_ EXTRG1		UART0_RX		I2C0_SCL
52	40	28	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN			UART0_TX		I2C0_SDA
53	—	—	—	PTC8	ADC1_SE14/ CMP0_IN2	ADC1_SE14/ CMP0_IN2	PTC8		FTM3_CH4				
54	—	—	—	PTC9	ADC1_SE15/ CMP0_IN3	ADC1_SE15/ CMP0_IN3	PTC9		FTM3_CH5				
55	—	—	—	PTC10	ADC1_SE16	ADC1_SE16	PTC10		FTM5_CH0	FTM5_QD_ PHA			
56	—	—	—	PTC11/ LLWU_P11	ADC1_SE17	ADC1_SE17	PTC11/ LLWU_P11		FTM5_CH1	FTM5_QD_ PHB			
57	41	—	—	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART0_ CTS_b	FTM0_CH0	UART1_RX	FTM3_CH0	
58	42	—	—	PTD1	ADC0_SE2	ADC0_SE2	PTD1	SPI0_SCK	UART0_ RTS_b	FTM0_CH1	UART1_TX	FTM3_CH1	
59	43	—	—	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART0_RX	FTM0_CH2		FTM3_CH2	I2C0_SCL
60	44	—	—	PTD3	DISABLED		PTD3	SPI0_SIN	UART0_TX	FTM0_CH3		FTM3_CH3	I2C0_SDA
61	45	29	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_ RTS_b	FTM0_CH4	FTM2_CH0	EWM_IN	SPI0_PCS0
62	46	30	30	PTD5	ADC0_SE3	ADC0_SE3	PTD5	SPI0_PCS2	UART0_ CTS_b	FTM0_CH5	FTM2_CH1	EWM_OUT_ b	SPI0_SCK
63	47	31	31	PTD6/ LLWU_P15	ADC1_SE6	ADC1_SE6	PTD6/ LLWU_P15	FTM4_CH0	UART0_RX	FTM0_CH0	FTM1_CH0	FTM0_FLT0	SPI0_SOUT
64	48	32	32	PTD7	DISABLED		PTD7	FTM4_CH1	UART0_TX	FTM0_CH1	FTM1_CH1	FTM0_FLT1	SPI0_SIN

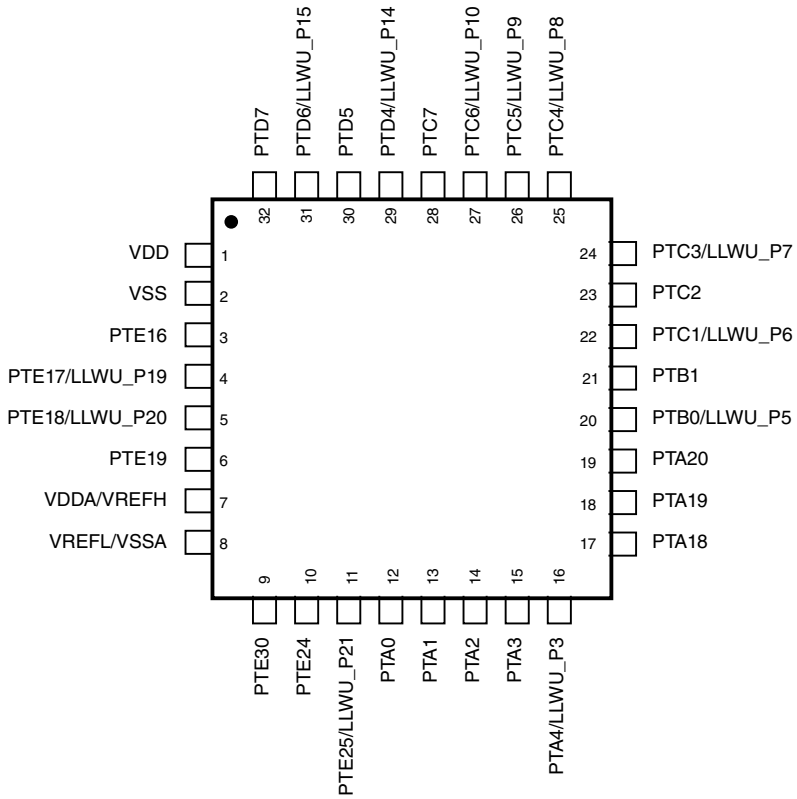

Figure 20. 32 LQFP Pinout Diagram

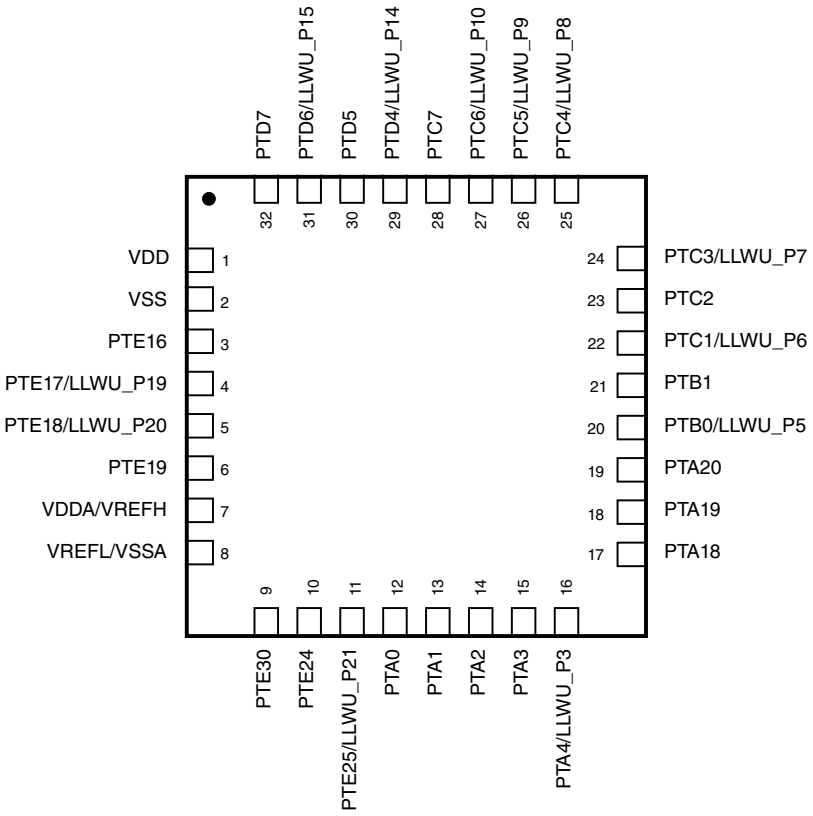

Figure 21. 32 QFN Pinout Diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the MKV11 device numbers.

7 Part identification

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

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