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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv11z64vlh7

Ordering Information [1]

Part Number	Memory		FlexCAN	Maximum number of I\O's
	Flash (KB)	SRAM (KB)		
MKV11Z128VLH7	128	16	Yes	54
MKV11Z128VLF7	128	16	Yes	40
MKV11Z128VLC7 [2]	128	16	Yes	28
MKV11Z128VFM7	128	16	Yes	28
MKV11Z64VLH7	64	16	Yes	54
MKV11Z64VLF7	64	16	Yes	40
MKV11Z64VLC7 [2]	64	16	Yes	28
MKV11Z64VFM7	64	16	Yes	28
MKV10Z64VLH7	64	16	No	54
MKV10Z64VLF7	64	16	No	40
MKV10Z64VLC7 [2]	64	16	No	28
MKV10Z64VFM7	128	16	No	28
MKV10Z128VLH7	128	16	No	54
MKV10Z128VLF7	128	16	No	40
MKV10Z128VLC7 [2]	128	16	No	28
MKV10Z128VFM7	128	16	No	28

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.
2. The 32-pin LQFP package supporting this part number is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit http://www.freescale.com/KPYW for more details.

Related Resources

Type	Description
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in package drawings.

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Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{ICcont}	Contiguous pin DC injection current—regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection	–25	—	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/I_{ICIO}.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad All port pins, except PTC6 and PTC7 • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –1.5 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
V_{OH}	Output high voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –6 mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	 V V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad All port pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	 — —	 0.5 0.5	 V V	
V_{OL}	Output low voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA	 — —	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	1
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	1
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	2

1. Measured at V_{DD} = 3.6 V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 75 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 4. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	
	• VLLS0 → RUN	—	123	132	µs	
	• VLLS1 → RUN	—	123	132	µs	
	• VLLS3 → RUN	—	67	72	µs	
	• VLPS → RUN	—	4	5	µs	
	• STOP → RUN	—	4	5	µs	

2.2.5 KV11x Power consumption operating behaviors

Table 5. KV11x power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	5	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					Target IDD
	• at 1.8 V 50 MHz (25 MHz Bus)	—	5.3	6.2	mA	
	• at 3.0 V 50 MHz (25 MHz Bus)	—	5.4	6.3	mA	
	• at 1.8 V 75 MHz (25 MHz Bus)	—	7.2	8.3	mA	
	• at 3.0 V 75 MHz (25 MHz Bus)	—	7.3	8.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					Target IDD

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{FTM}	FTM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.							µA
	MCGIRCLK (4 MHz internal reference clock)	150	150	150	150	150	150	
	OSCERCLK (4 MHz external crystal)	300	300	300	320	340	350	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA
I_{WDOG}	WDOG peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode (except for 75 MHz which is in FEE mode), and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

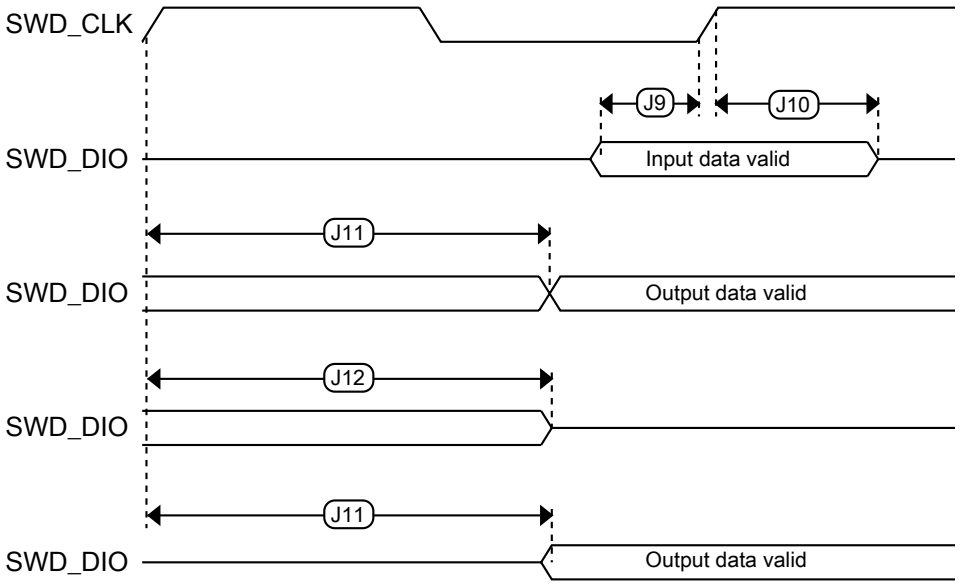


Figure 6. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	±2	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C		—	± 0.4	± 1.5	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C		—	+1/-2	± 3	$\%f_{intf\_ft}$	2
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS = 00, DMX32 = 0) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01, DMX32 = 0) 1280 × f_{fll_ref}	40	41.94	48	MHz	
		Mid range (DRS = 10, DMX32 = 0) 1920 x f_{fll_ref}	60	62.915	75	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00, DMX32 = 1) 732 × f_{fll_ref}	—	23.99	—	MHz	5 6
		Mid range (DRS = 01, DMX32 = 1) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid range (DRS = 10, DMX32 = 1) 2197 × f_{fll_ref}	–	71.991	–	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 75 MHz		—	180	—	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft}.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.

4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or there is a change from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 4 MHz	—	500	—	µA	
	• 8 MHz	—	600	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

Table 16. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	500	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 17. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

Table 22. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.7 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 –97 –91	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode	82	100	—	dB	7

Table continues on the next page...

3.6.3.1 12-bit DAC operating requirements

Table 24. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.3.2 12-bit DAC operating behaviors

Table 25. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08)—high-speed mode	—	1	—	µs	1
	—low-power mode	—	—	5	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	

Table continues on the next page...

3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 28. Master mode DSPI timing (full voltage range)

Symbol	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.7	3.6	V	1
	Frequency of operation	–	**18.75**	**MHz**	2
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	10		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	
	Frequency of operation	–	**18.75**	**MHz**	6
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	26		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	

Table continues on the next page...

Table 28. Master mode DSPI timing (full voltage range) (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Frequency of operation	–	**25**	**MHz**	7
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	–	ns	3
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 4	(t_{SCK}/2) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{SCK}/2) – 4	–	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{SCK}/2) – 4	–	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	–	10		
DS6	DSPI_SCK to DSPI_SOUT invalid	–7.8	–	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	–	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	–	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. Normal pads
3. The SPI module is clocked by the system clock
4. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
5. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC]
6. Open Drain pads: SIN: PTC7, SOUT:PTC6
7. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

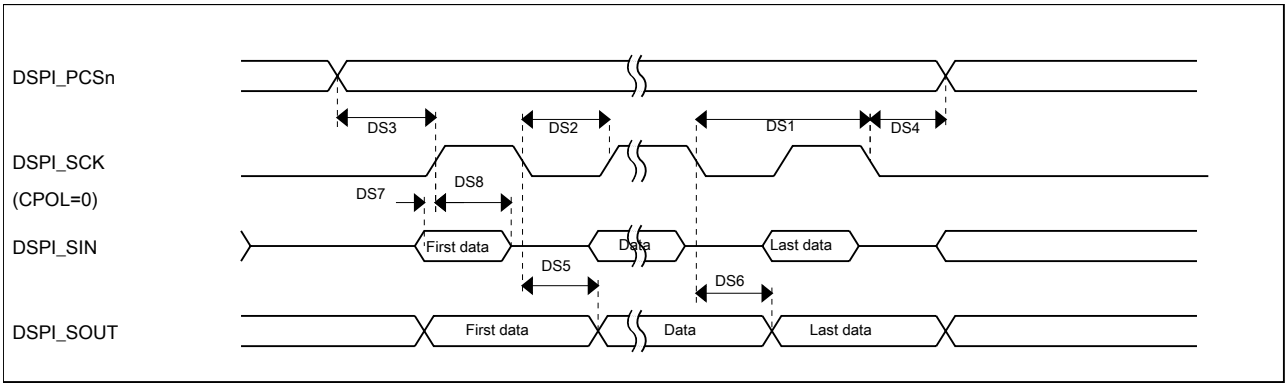


Figure 16. DSPI classic SPI timing — master mode

Table 29. Slave mode DSPI timing (full voltage range)

Symbol	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.7	3.6	V	
	Frequency of operation	–	**9.375**	**MHz**	1

Table continues on the next page...

5 Pinout

5.1 KV11 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 are high current pins.
- PTC6 and PTC7 have open drain outputs

64 LQFP	48 QFP	32 QFN	32 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	—	7	7	VDDA/ VREFH	VDDA/ VREFH	VDDA/ VREFH							
—	—	8	8	VREFL/ VSSA	VREFL/ VSSA	VREFL/ VSSA							
1	—	—	—	PTE0	ADC1_SE12	ADC1_SE12	PTE0		UART1_TX				
2	—	—	—	PTE1/ LLWU_P0	ADC1_SE13	ADC1_SE13	PTE1/ LLWU_P0		UART1_RX				
3	1	1	1	VDD	VDD	VDD							
4	2	2	2	VSS	VSS	VSS							
5	3	3	3	PTE16	ADC0_SE1/ ADC0_DP1/ ADC1_SE0	ADC0_SE1/ ADC0_DP1/ ADC1_SE0	PTE16	SPI0_PCS0	UART1_TX	FTM_ CLKIN0		FTM0_FLT3	
6	4	4	4	PTE17/ LLWU_P19	ADC0_DM1/ ADC0_SE5/ ADC1_SE5	ADC0_DM1/ ADC0_SE5/ ADC1_SE5	PTE17/ LLWU_P19	SPI0_SCK	UART1_RX	FTM_ CLKIN1		LPTMR0_ ALT3	
7	5	5	5	PTE18/ LLWU_P20	ADC0_SE6/ ADC1_SE1/ ADC1_DP1	ADC0_SE6/ ADC1_SE1/ ADC1_DP1	PTE18/ LLWU_P20	SPI0_SOUT	UART1_ CTS_b	I2C0_SDA		SPI0_SIN	
8	6	6	6	PTE19	ADC0_SE7/ ADC1_SE7/ ADC1_DM1	ADC0_SE7/ ADC1_SE7/ ADC1_DM1	PTE19	SPI0_SIN	UART1_ RTS_b	I2C0_SCL		SPI0_SOUT	
9	7	—	—	PTE20	ADC0_SE0/ ADC0_DP0	ADC0_SE0/ ADC0_DP0	PTE20		FTM1_CH0	UART0_TX			
10	8	—	—	PTE21	ADC0_SE4/ ADC0_DM0	ADC0_SE4/ ADC0_DM0	PTE21		FTM1_CH1	UART0_RX			
11	—	—	—	PTE22	ADC0_SE12	ADC0_SE12	PTE22						
12	—	—	—	PTE23	ADC0_SE13	ADC0_SE13	PTE23						
13	9	—	—	VDDA	VDDA	VDDA							

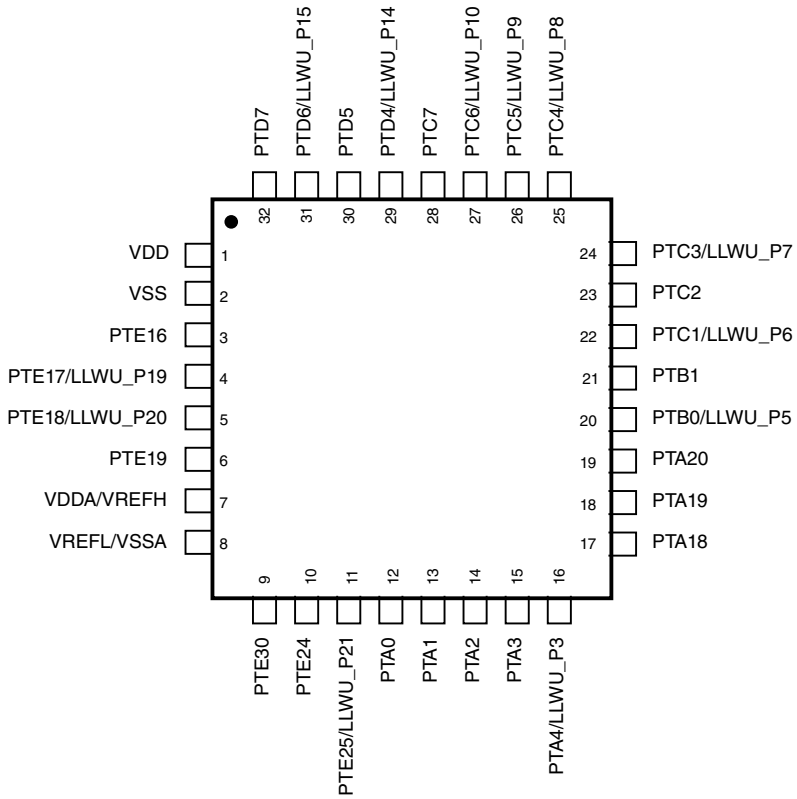


Figure 20. 32 LQFP Pinout Diagram

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KV## M FFF R T PP CC N

7.3 Fields

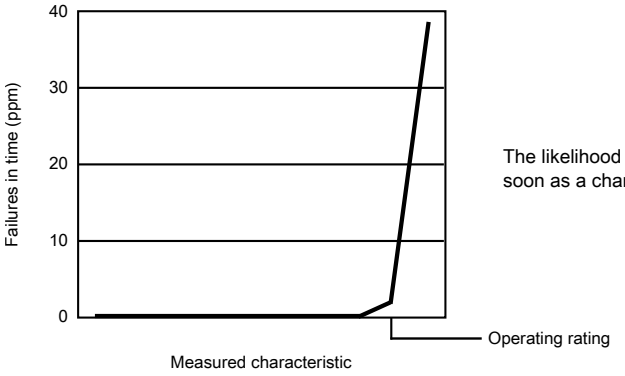
This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KV##	Kinetis family	• KV10 and KV11
M	Key attribute	• Z = M0+ core
FFF	Program flash memory size	• 128 = 128 KB
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• FK = 24 QFN (4 mm x 4 mm) • LC = 32 LQFP (7 mm x 7 mm) • FM = 32 QFN (5 mm x 5 mm) • LF = 48 LQFP (7 mm x 7 mm) • FT = 48 QFN (10 mm x 10 mm) • LH = 64 LQFP (10 mm x 10 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm)
CCC	Maximum CPU frequency (MHz)	• 7 = 75 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

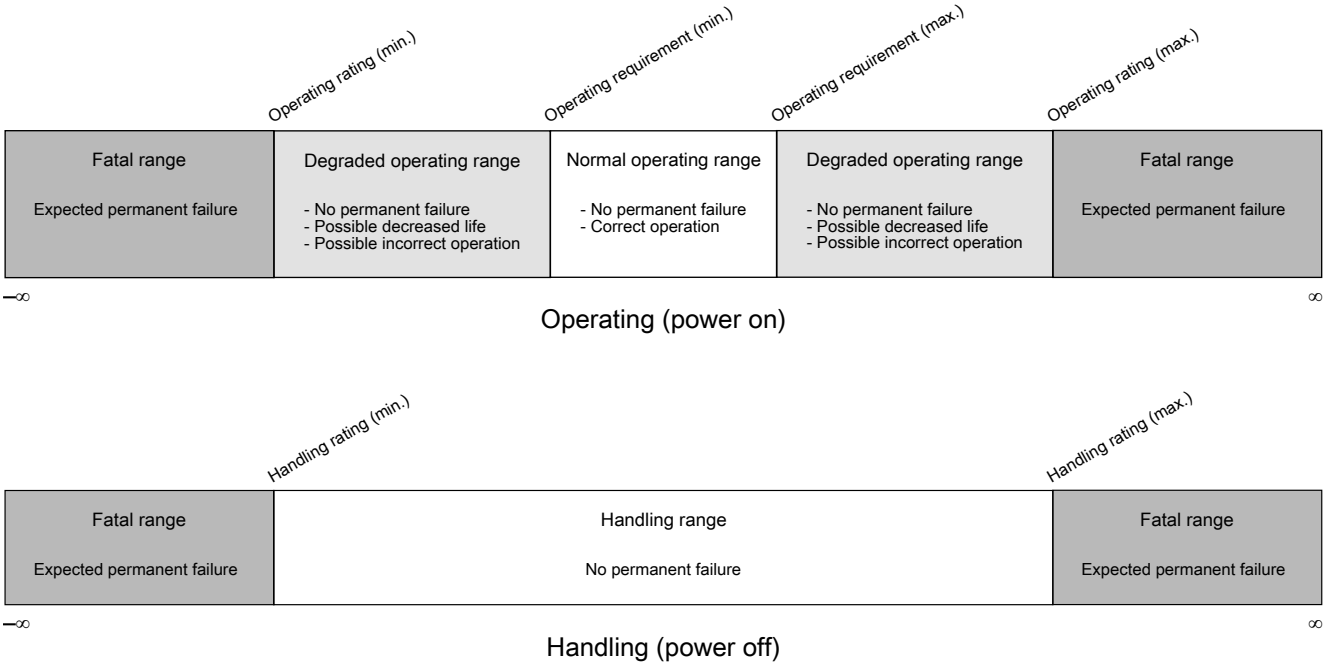
This is an example part number:

8.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

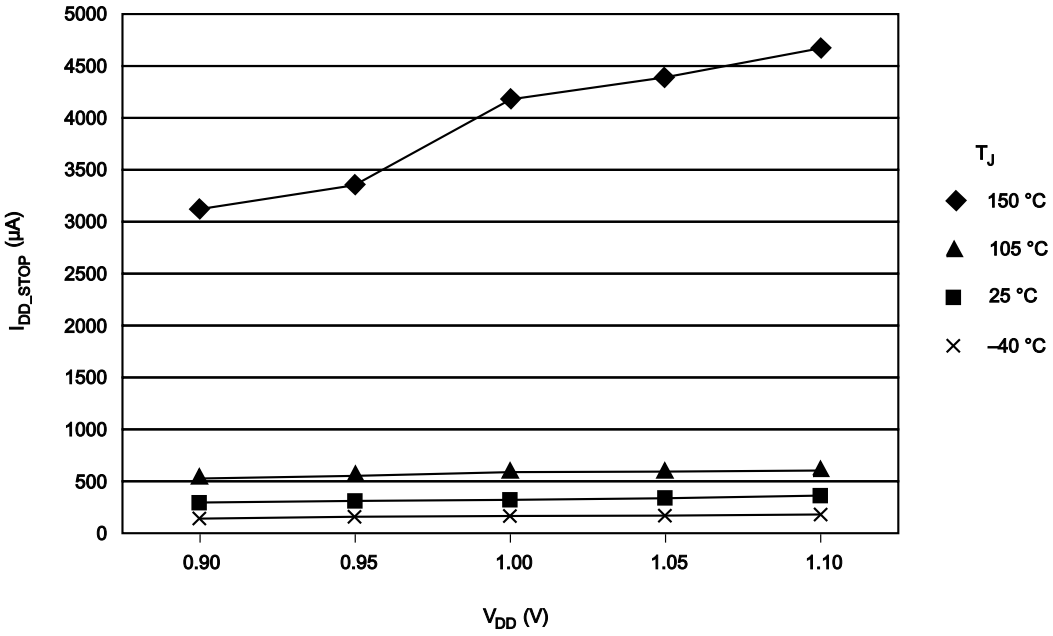
8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.



8.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 30. Revision history

Rev. No.	Date	Substantial Changes
0	11/2014	Initial Prelim release.
1	02/2015	Updated the following sections: • DSPI switching specifications (limited voltage range) • DSPI switching specifications (full voltage range) • KV11 Signal Multiplexing and Pin Assignments

Table continues on the next page...

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