Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2cc8h0agv2000a

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
27	-	-	-	P59 SOT11_1 (SDA11_1) IC02_1 TIOB3_1 MADATA25_0	E	I
28	-	-	-	P5A SCK11_1 (SCL11_1) IC03_1 TIOB4_1 MADATA26_0	E	I
29	-	-	-	P5B FRCK0_1 TIOB5_1 MADATA27_0	E	I
30	21	18	G3	P08 SIN14_0 TIOB12_0 INT17_0 MDQM0_0	E	K
31	22	19	G4	P09 SOT14_0 (SDA14_0) TIOB13_0 INT18_0 MDQM1_0	E	K
32	23	20	G5	P0A ADTG_1 SCK14_0 (SCL14_0) AIN2_1 MCLKOUT_0	L	I
33	-	-	-	P5C TIOA11_2 MADATA28_0 RTCCO_1 SUBOUT_1	E	I
34	24	-	G6	P30 RX0_1 TIOA13_2 INT03_2 MDQM2_0 I2SDI0_0	E	K
35	25	-	H4	P31 TX0_1 TIOB13_2 MDQM3_0 I2SCK0_0	E	I
36	26	21	H2	P32 BIN2_1 INT19_0 S_DATA1_0	L	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
37	27	22	J1	P33 FRCK0_0 ZIN2_1 S_DATA0_0	L	I
38	28	23	H3	P34 IC03_0 INT00_1 S_CLK_0	L	K
39	29	24	H1	VCC	-	-
40	30	25	H5	VSS	-	-
41	31	26	H6	P35 IC02_0 INT01_1 S_CMD_0	L	K
42	32	27	J5	P36 IC01_0 INT02_1 S_DATA3_0	L	K
43	33	28	J4	P37 IC00_0 INT03_1 S_DATA2_0	L	K
44	34	29	J3	P38 ADTG_2 DTTI0X_0 S_WP_0	E	I
45	35	30	J2	P39 SIN2_1 RTO00_0 (PPG00_0) TIOA0_1 AIN3_1 INT16_1 S_CD_0 MAD24_0	G	K
46	36	31	K1	P3A SOT2_1 (SDA2_1) RTO01_0 (PPG00_0) TIOA1_1 BIN3_1 INT17_1 MAD23_0	G	K
47	37	32	K2	P3B SCK2_1 (SCL2_1) RTO02_0 (PPG02_0) TIOA2_1 ZIN3_1 INT18_1 MAD22_0 MNALE_0	G	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
48	38	33	K3	P3C SIN13_0 RTO03_0 (PPG02_0) TIOA3_1 INT19_1 MAD21_0 MNCLE_0	G	K
49	39	34	K4	P3D SOT13_0 (SDA13_0) RTO04_0 (PPG04_0) TIOA4_1 MAD20_0 MNWEX_0	G	I
50	40	35	L1	P3E SCK13_0 (SCL13_0) RTO05_0 (PPG04_0) TIOA5_1 MAD19_0 MNREX_0	G	I
51	41	-	L2	P5D SIN10_1 TIOB11_2 INT01_2 MADATA29_0 I2SMCLK0_0	E	K
52	42	-	L3	P5E SOT10_1 (SDA10_1) TIOA12_2 MADATA30_0 I2SDO0_0	E	I
53	43	-	M2	P5F SCK10_1 (SCL10_1) TIOB12_2 MADATA31_0 I2SWS0_0	E	I
54	44	36	M1	VSS	-	-
55	45	37	N1	VCC	-	-
56	46	38	N2	P40 SIN3_1 RTO10_0 (PPG10_0) TIOA0_0 AIN0_0 INT23_0 MCSX7_0	G	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
190	158	128	A7	PCB INT28_0 E_COUT	L	W
191	159	129	C7	PCC E_TCK	K	V
192	160	130	A6	PCD SOT4_1 (SDA4_1) INT14_0 E_TXER	L	W
193	161	131	D7	PCE SIN4_1 INT15_0 E_TX03	L	W
194	162	132	E7	PCF RTS4_1 INT12_0 E_TX02	L	W
195	163	133	F7	PD0 INT30_1 E_TX01	L	W
196	164	134	B6	PD1 INT31_1 E_TX00	L	W
197	165	135	C6	PD2 CTS4_1 FRCK2_1 E_TXEN	L	V
198	166	136	D6	P6E ADTG_5 SCK4_1 (SCL4_1) IC23_1 INT29_0 E_PPS	E	W
199	-	-	-	P6D SCK14_1 (SCL14_1) IC22_1 TIOB6_2	E	I
200	-	-	-	P6C SOT14_1 (SDA14_1) IC21_1 TIOA6_2	E	I
201	-	-	-	P6B SIN14_1 IC20_1 TIOB7_2 INT14_2	E	K
202	-	-	-	P6A DTTI2X_1 TIOA7_2	E	I
203	-	-	-	P69 RTO20_1 (PPG20_1) TIOB14_2	E	I

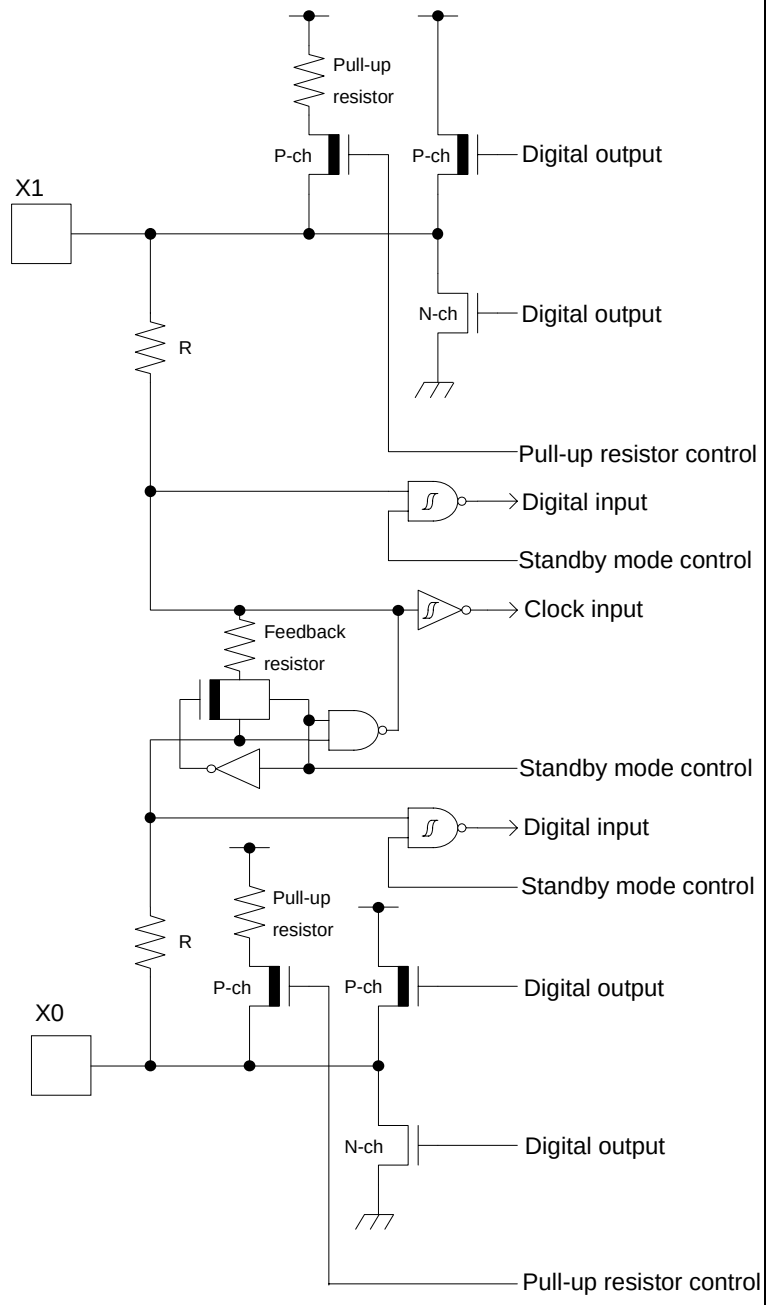
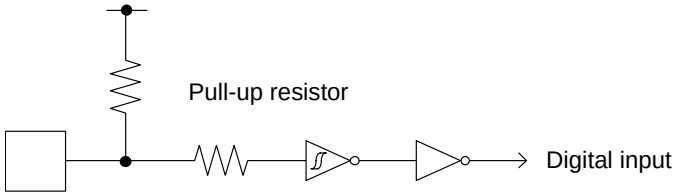
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
216	176	144	B1	VSS	-	-
-	-	-	E1		-	-
-	-	-	G1		-	-
-	-	-	P7		-	-
-	-	-	P11		-	-
-	-	-	L14		-	-
-	-	-	A11		-	-
-	-	-	A5		-	-
-	-	-	N7		-	-
-	-	-	M7		-	-
-	-	-	L7		-	-
-	-	-	K7		-	-
-	-	-	J7		-	-
--	-	-	G7		-	-
-	-	-	H7		-	-
-	-	-	H8		-	-
-	-	-	G8		-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Clock	X0	Main clock (oscillation) input pin	106	86	70	P12
	X1	Main clock (oscillation) I/O pin	107	87	71	P13
	X0A	Sub clock (oscillation) input pin	73	58	50	P5
	X1A	Sub clock (oscillation) I/O pin	74	59	51	P6
	CROUT_0	Built-in High-speed CR-oscillation clock output port	157	127	103	D13
	CROUT_1		184	152	122	E8
Analog power	AVCC	A/D converter and D/A converter analog power-supply pin	110	90	74	M13
	AVRL	A/D converter analog reference voltage input pin	112	92	76	L13
	AVRH	A/D converter analog reference voltage input pin	113	93	77	L12
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	75	60	52	P8
Analog GND	AVSS	A/D converter and D/A converter GND pin	111	91	75	M12
C pin	C	Power supply stabilization capacity pin	62	52	44	P2

Note:

- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 1 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA
B		・ CMOS level hysteresis input ・ Pull-up resistor: approximately 50 kΩ

6. Handling Precautions

Every semiconductor device has a characteristic, inherent rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins that connect semiconductor devices to power supply and I/O functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device; therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power-supply pin or ground pin.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	200 MHz	128	236	mA	*3 When all peripheral clocks are on
					192 MHz	123	230	mA	
					180 MHz	116	221	mA	
				*6	160 MHz	102	205	mA	
					144 MHz	93	193	mA	
					120 MHz	79	175	mA	
					100 MHz	67	161	mA	
					80 MHz	54	145	mA	
					60 MHz	42	130	mA	
					40 MHz	30	115	mA	
					20 MHz	17	99	mA	
					8 MHz	9.2	90.0	mA	
					4 MHz	6.7	86.9	mA	
				*5	200 MHz	74	170	mA	*3 When all peripheral clocks are off
					192 MHz	71	167	mA	
					180 MHz	67	162	mA	
				*6	160 MHz	59	152	mA	
					144 MHz	53	145	mA	
					120 MHz	45	135	mA	
					100 MHz	39	127	mA	
					80 MHz	32	118	mA	
					60 MHz	25	110	mA	
					40 MHz	18	101	mA	
					20 MHz	11	92	mA	
					8 MHz	6.5	86.8	mA	
					4 MHz	5.1	85.0	mA	

*1: T_A = +25 °C, V_{CC} = 3.3 V

*2: T_J = +125 °C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

*7: With data access to a MainFlash memory.

*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, TIMER Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.56	3.01	mA	*3, *4 T_A = +25°C
					-	27.03	mA	*3, *4 T_A = +85°C
					-	39.92	mA	*3, *4 T_A = +105°C
	I_{CCT}		Timer mode*5 (main oscillation)	4 MHz	1.40	3.85	mA	*3, *4 T_A = +25°C
					-	27.87	mA	*3, *4 T_A = +85°C
					-	40.76	mA	*3, *4 T_A = +105°C
			Timer mode (built-in High-speed CR)	4 MHz	0.95	3.40	mA	*3, *4 T_A = +25°C
					-	27.42	mA	*3, *4 T_A = +85°C
					-	40.31	mA	*3, *4 T_A = +105°C
			Timer mode*6 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T_A = +25°C
					-	27.04	mA	*3, *4 T_A = +85°C
					-	39.93	mA	*3, *4 T_A = +105°C
			Timer mode (built-in low-speed CR)	100 kHz	0.58	3.03	mA	*3, *4 T_A = +25°C
					-	27.05	mA	*3, *4 T_A = +85°C
					-	39.94	mA	*3, *4 T_A = +105°C
	I_{CCR}		RTC mode*5 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T_A = +25°C
					-	27.04	mA	*3, *4 T_A = +85°C
					-	39.93	mA	*3, *4 T_A = +105°C

*1: V_{CC} = 3.3 V

*2: V_{CC} = 5.5 V

*3: When all ports are fixed

*4: When LVD is off

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

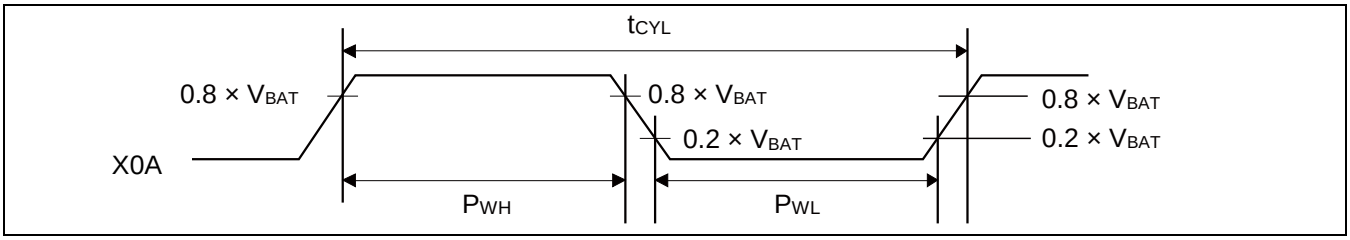
*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 1.65V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 7. Handling Devices.



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = - 20°C to + 105°C	3.92	4	4.08	MHz	When trimming *1
		T_J = - 40°C to + 125°C	3.88	4	4.12		
		T_J = - 40°C to + 125°C	3	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

*2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

Built-In Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Minimum pulse width	t_{OEW}	MOEX	-	MCLK×n-3	-	ns	
MCSX ↓ →Address output delay time	t_{CSL-AV}	MCSX[7: 0], MAD[24: 0]	-	-9	+9	ns	
MOEX ↑ →Address hold time	t_{OEH-AX}	MOEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7: 0]	-	MCLK×m-9	MCLK×m+9	ns	
MOEX ↑ → MCSX ↑ time	$t_{OEH-CSH}$		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[3: 0]	-	MCLK×m-9	MCLK×m+9	ns	
Data set up→MOEX ↑ time	t_{DS-OE}	MOEX, MADATA[31: 0]	-	20	-	ns	
MOEX ↑ → Data hold time	t_{DH-OE}	MOEX, MADATA[31: 0]	-	0	-	ns	
MWEX Minimum pulse width	t_{WEW}	MWEX	-	MCLK×n-3	-	ns	
MWEX ↑ →Address output delay time	t_{WEH-AX}	MWEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH-CSH}$		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[3: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MCSX ↓ → Data output time	t_{CSL-DX}	MCSX, MADATA[31: 0]	-	MCLK-9	MCLK+9	ns	
MWEX ↑ → Data hold time	t_{WEH-DX}	MWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*

NAND Flash Mode

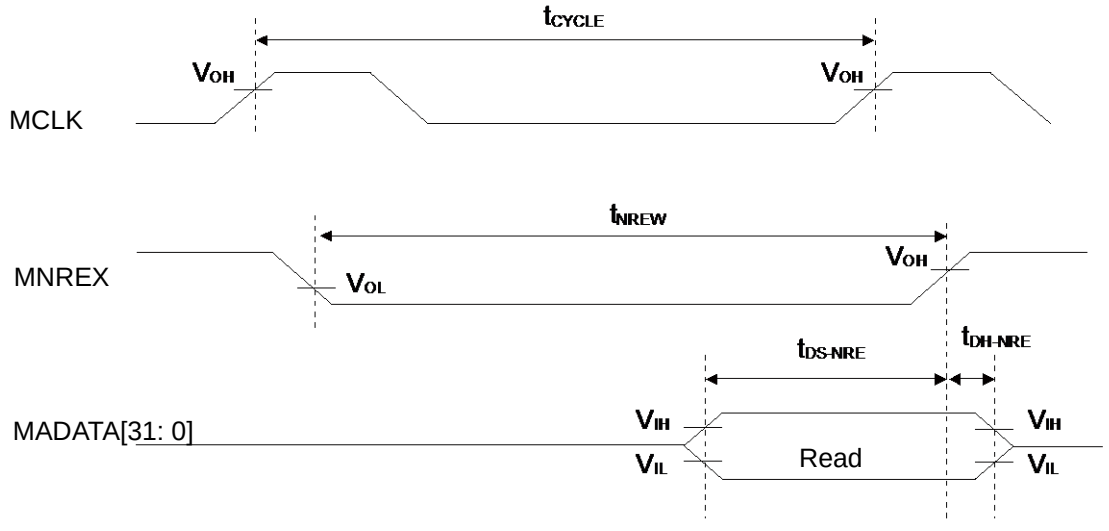
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

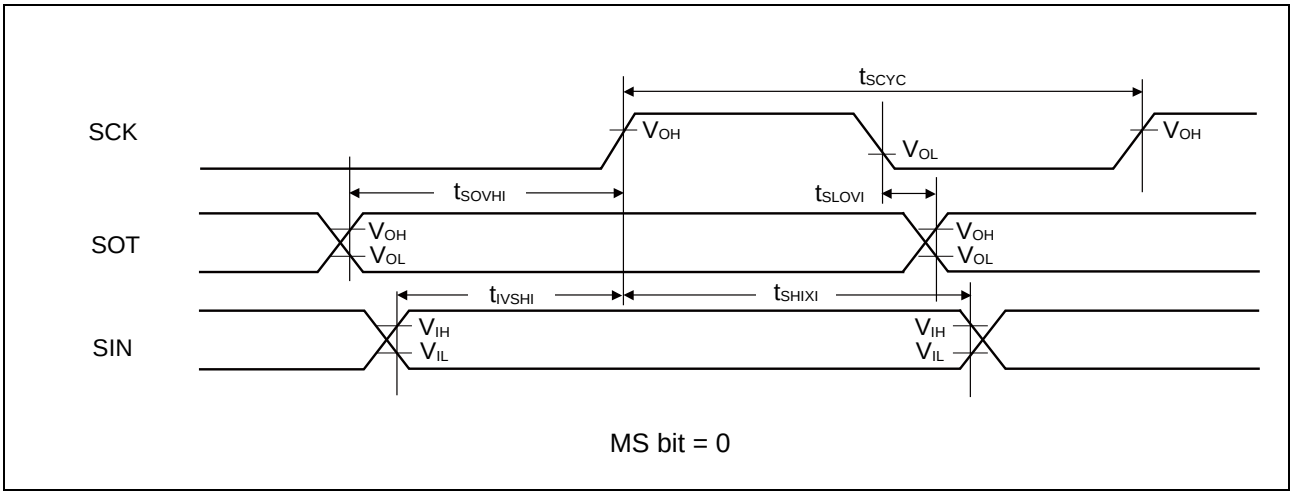
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t_{NREW}	MNREX	-	MCLK×n-3	-	ns	
Data set up →MNREX ↑ time	t_{DS-NRE}	MNREX, MADATA[31: 0]	-	20	-	ns	
MNREX ↑ → Data hold time	t_{DH-NRE}	MNREX, MADATA[31: 0]	-	0	-	ns	
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNWEX ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	-	0	MCLK×m+9	ns	
MNWEX Min pulse width	t_{NWEW}	MNWEX	-	MCLK×n-3	-	ns	
MNWEX ↓ → Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[31: 0]	-	-9	9	ns	
MNWEX ↑ → Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

Note:

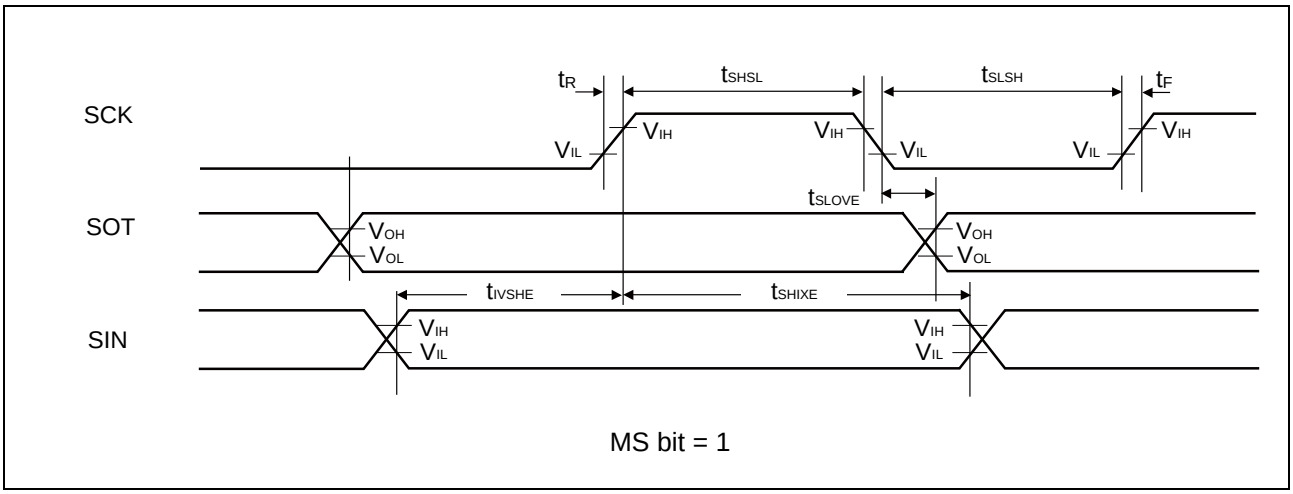
- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*

NAND Flash Read

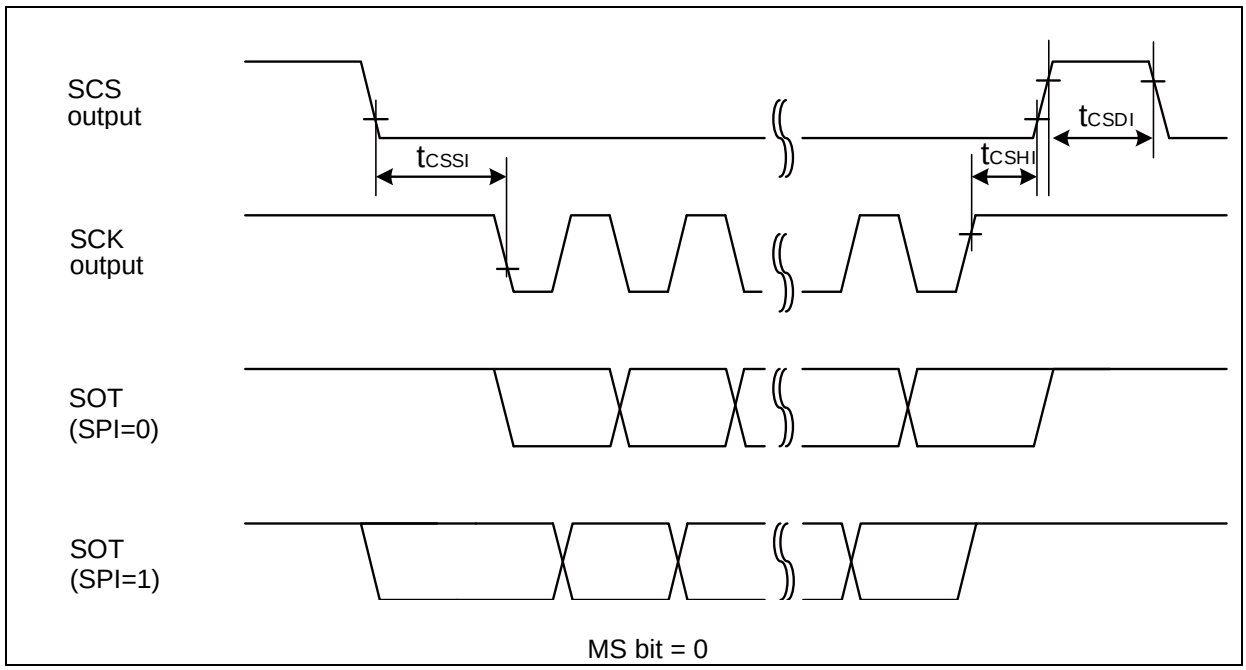


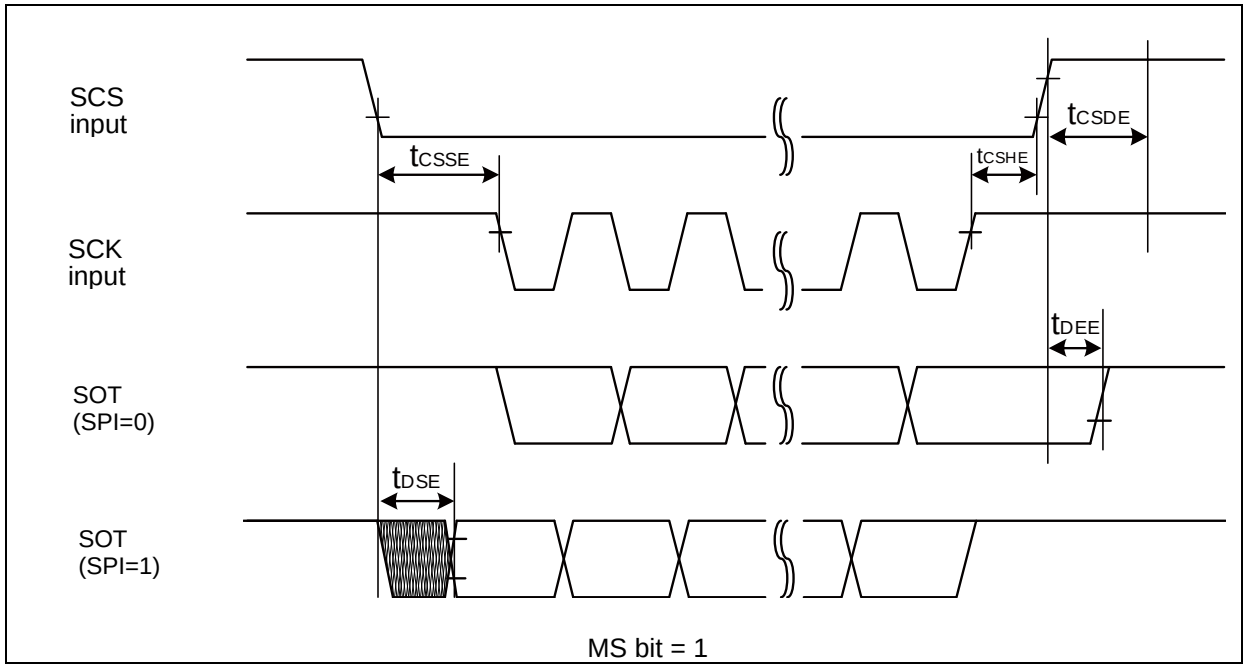


MS bit = 0



MS bit = 1


SCS
output
tCSSI
tCSDI
tCSHI
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
MS bit = 0


SCS
input
tCSSE
tCSDE
tCSHE
SCK
input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)
MS bit = 1

Fast mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
SCL clock frequency	t_{SUSTA}		0.26	-	µs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between "Stop condition" and "START condition"	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

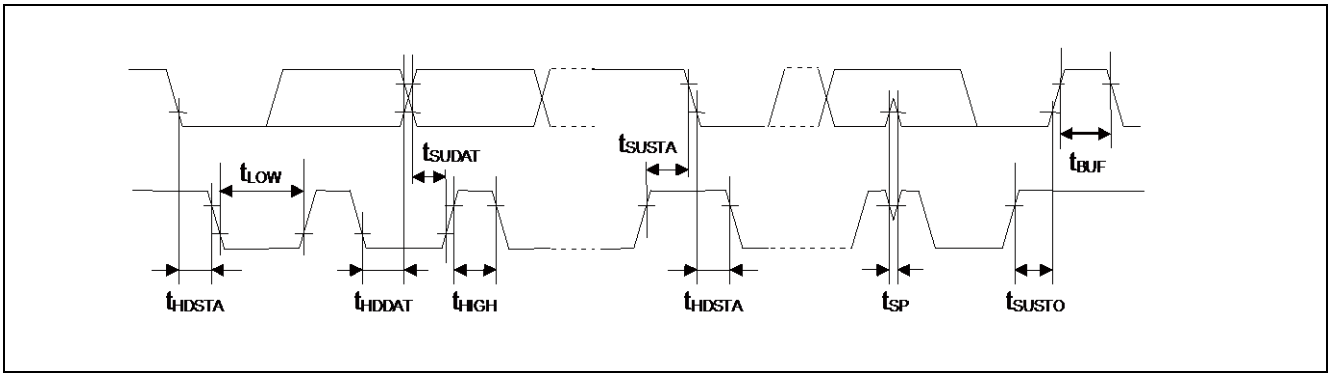
*2: The maximum t_{HDDT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

*3: The Fast mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns."

*4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I^2C is connected, see 8.Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

*6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register. See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.



Slave Mode Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{SCYC}	I2SCK	-	-	12.288	MHz	
Input clock pulse width	t_{SHW}	I2SCK	-	45	55	%	
	t_{SLW}			45	55	%	
I2SWS→I2SCK Setup time	t_{SFI}	I2SCK, I2SWS	-	8	-	ns	
I2SWS→I2SCK Hold time	t_{HFI}	I2SCK, I2SWS	-	0	-	ns	
I2SCK ↑ →I2SDO Delay time*1	t_{DDO}	I2SCK, I2SDO	-	0	32	ns	
I2SCK ↑ →I2SDO Delay Time*2	t_{DFB1}		-	0	32	ns	
I2SDI→I2SCK ↓ Setup time	t_{SDI}	I2SCK, I2SDI	-	8	-	ns	
I2SDI→I2SCK ↓ Hold time	t_{HDI}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SCK, I2SWS, I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

*1: Except for the first bit of transmission frame

*2: When FSPH bit = 1.

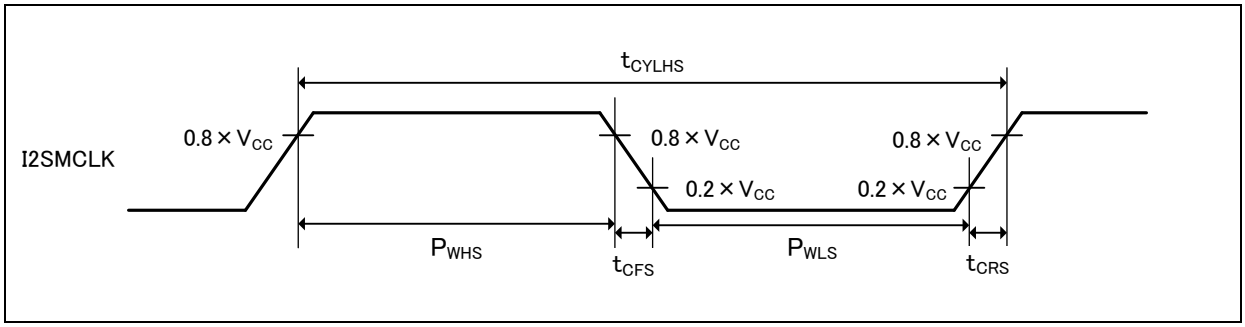
Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 ×I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz. See Chapter 7-2: I^2S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.

I2SMCLK Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	I2SMCK	-	-	25	MHz	
Input clock cycle	t_{CYLHS}	-	-	40	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock



I2SMCLK Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	I2SMCK	-	-	12.288	MHz	

12.11.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR Timer mode		315	567	µs	
Sub Timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep Standby RTC mode with RAM retention		336	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		336	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)