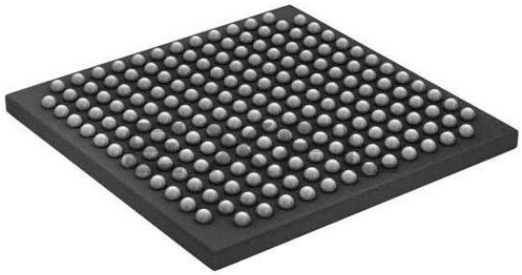

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	192-LFBGA
Supplier Device Package	192-FBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2cc8j0agb1000a

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
190	158	128	A7	PCB INT28_0 E_COUT	L	W
191	159	129	C7	PCC E_TCK	K	V
192	160	130	A6	PCD SOT4_1 (SDA4_1) INT14_0 E_TXER	L	W
193	161	131	D7	PCE SIN4_1 INT15_0 E_TX03	L	W
194	162	132	E7	PCF RTS4_1 INT12_0 E_TX02	L	W
195	163	133	F7	PD0 INT30_1 E_TX01	L	W
196	164	134	B6	PD1 INT31_1 E_TX00	L	W
197	165	135	C6	PD2 CTS4_1 FRCK2_1 E_TXEN	L	V
198	166	136	D6	P6E ADTG_5 SCK4_1 (SCL4_1) IC23_1 INT29_0 E_PPS	E	W
199	-	-	-	P6D SCK14_1 (SCL14_1) IC22_1 TIOB6_2	E	I
200	-	-	-	P6C SOT14_1 (SDA14_1) IC21_1 TIOA6_2	E	I
201	-	-	-	P6B SIN14_1 IC20_1 TIOB7_2 INT14_2	E	K
202	-	-	-	P6A DTTI2X_1 TIOA7_2	E	I
203	-	-	-	P69 RTO20_1 (PPG20_1) TIOB14_2	E	I

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_2FFF		Multi-Function Timer unit 1
0x4002_3000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_CFFF		Reserved
0x4003_D000	0x4003_DFFF		I^2S prescaler
0x4003_E000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch 0
0x4006_3000	0x4006_3FFF		CAN ch 1
0x4006_4000	0x4006_5FFF		Ethernet-MAC ch 0
0x4006_6000	0x4006_6FFF		Ethernet-MAC setting register
0x4006_7000	0x4006_BFFF		Reserved
0x4006_C000	0x4006_CFFF		I^2S
0x4006_D000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x4007_FFFF		CAN-FD (CAN ch 2)
0x4008_0000	0x4008_0FFF		Programmable-CRC
0x4008_1000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		Workflash I/F register
0xD000_0000	0xDFFF_FFFF		High-speed quad SPI control register

11. Pin Status In Each CPU State

The terms used for pin status have the following meanings:

- INITX = 0

  This is the period when the INITX pin is at the L level.

- INITX = 1

  This is the period when the INITX pin is at the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected							GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/ input enabled

*4: $ETHV_{CC}$ must not drop below V_{SS} - 0.5 V.

*5: V_{BAT} must not drop below V_{SS} - 0.5 V.

*6: Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.

*7: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*8: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

*9: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

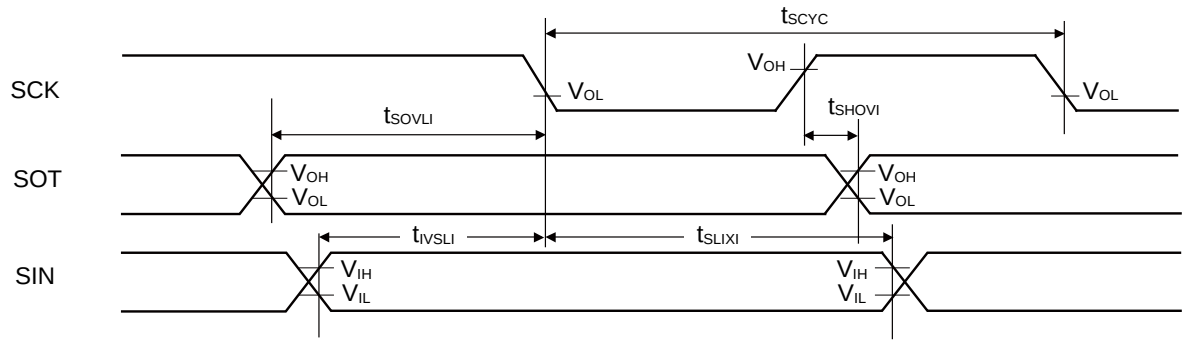
WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

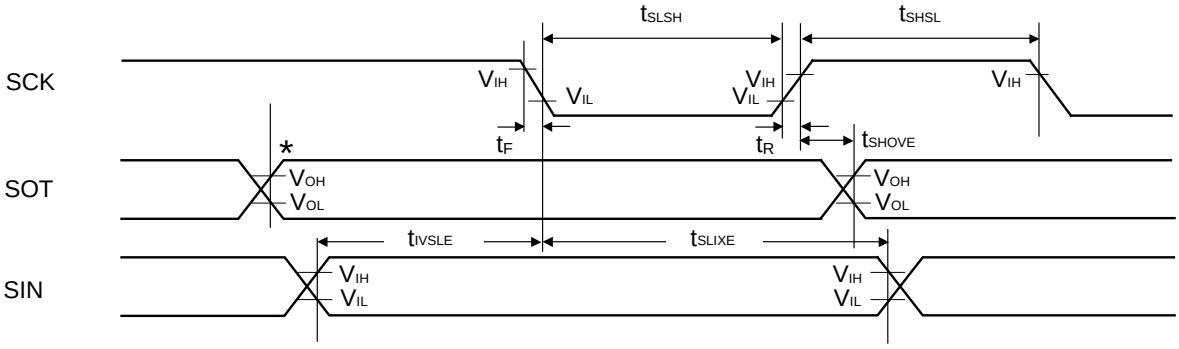
12.3.2 Pin Characteristics

(V_{CC} = $USBV_{CC}0$ = $USBV_{CC}1$ = $ETHV_{CC}$ = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
				$ETHV_{CC}$×0.8	-	$ETHV_{CC}$ + 0.3	V	
		MADATAxx	V_{CC} > 3.0 V, V_{CC} ≤ 3.6 V,	2.4	-	V_{CC} + 0.3	V	At External Bus
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	$ETHV_{CC}$+0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
				V_{SS} - 0.3	-	$ETHV_{CC}$×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
		TTL Schmitt input pin	-	V_{SS} - 0.3	-	0.8	V	
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
			$ETHV_{CC}$ ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	$ETHV_{CC}$	V	
			$ETHV_{CC}$ < 4.5 V, I_{OH} = - 2 mA					
		8 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 4 mA					
			$ETHV_{CC}$ ≥ 4.5 V, I_{OH} = - 8 mA	$ETHV_{CC}$ - 0.5	-	$ETHV_{CC}$	V	
			$ETHV_{CC}$ < 4.5 V, I_{OH} = - 4 mA					
		10 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 10 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5 V, I_{OH} = - 20.5 mA	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	*1
			$USBV_{CC}$ < 4.5 V, I_{OH} = - 13.0 mA					
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
			V_{CC} < 4.5V, I_{OH} = - 3 mA					



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Units
			Min	Max	Min	Max	
SCS ↑ →SCK ↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK ↓ →SCS ↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS ↑ →SCK ↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK ↓ →SCS ↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↑ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↓ →SOT delay time	t_{DEE}		0	-	0	-	ns

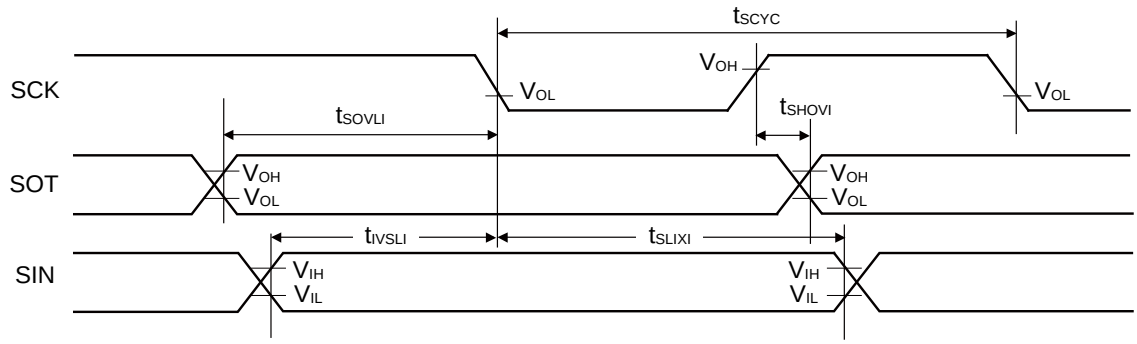
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

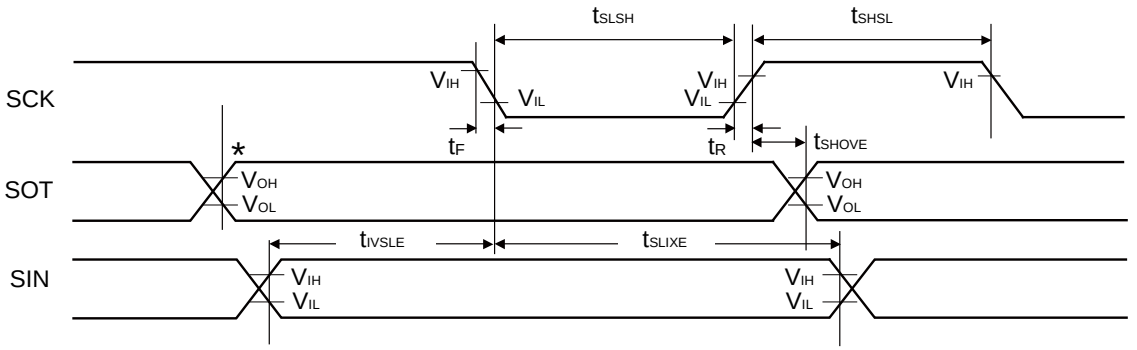
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

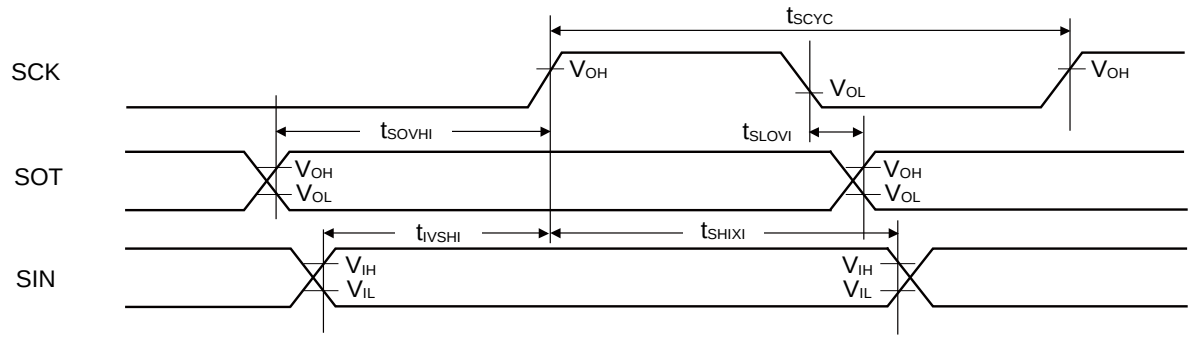


MS bit = 0

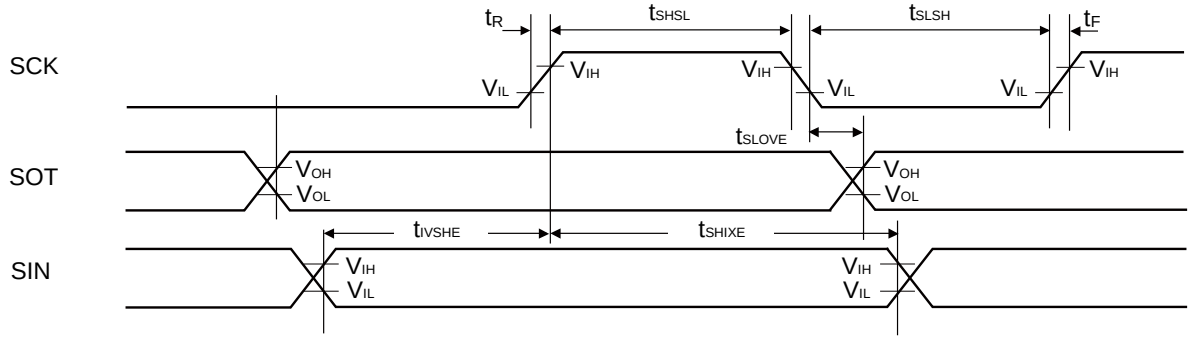


MS bit = 1

*: Changes when writing to TDR register



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Min	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

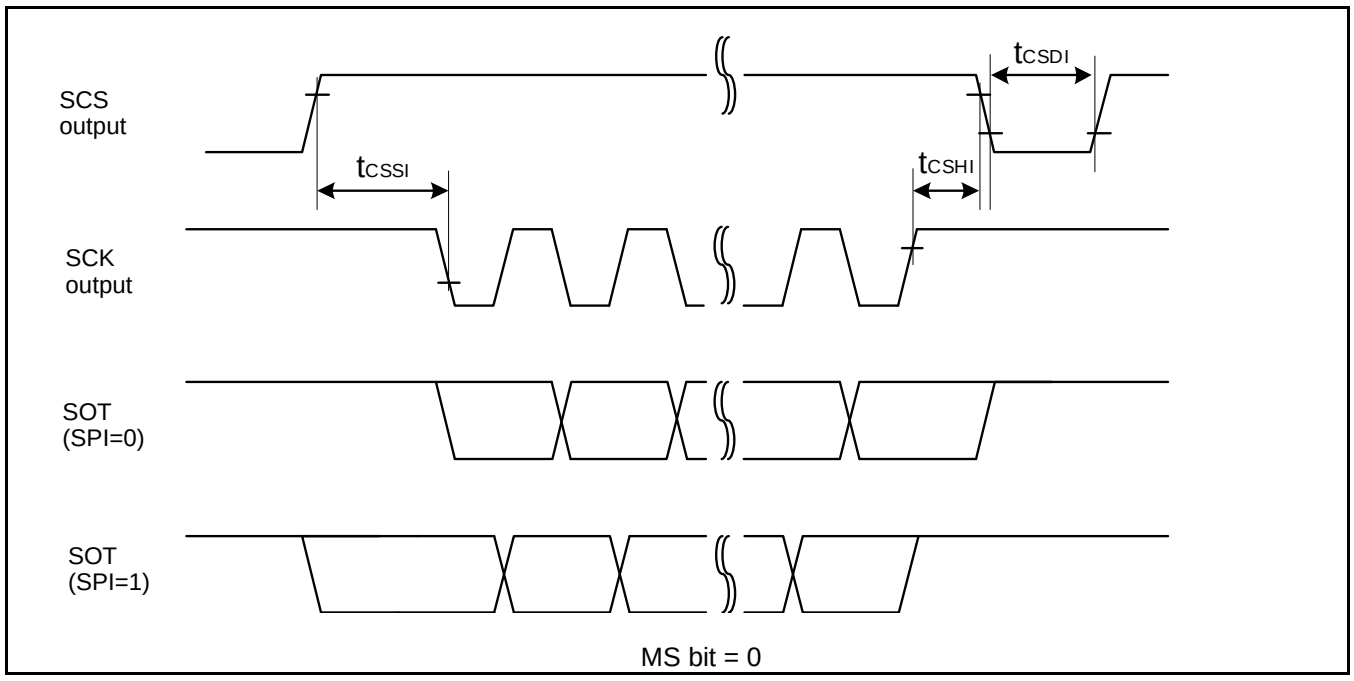
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

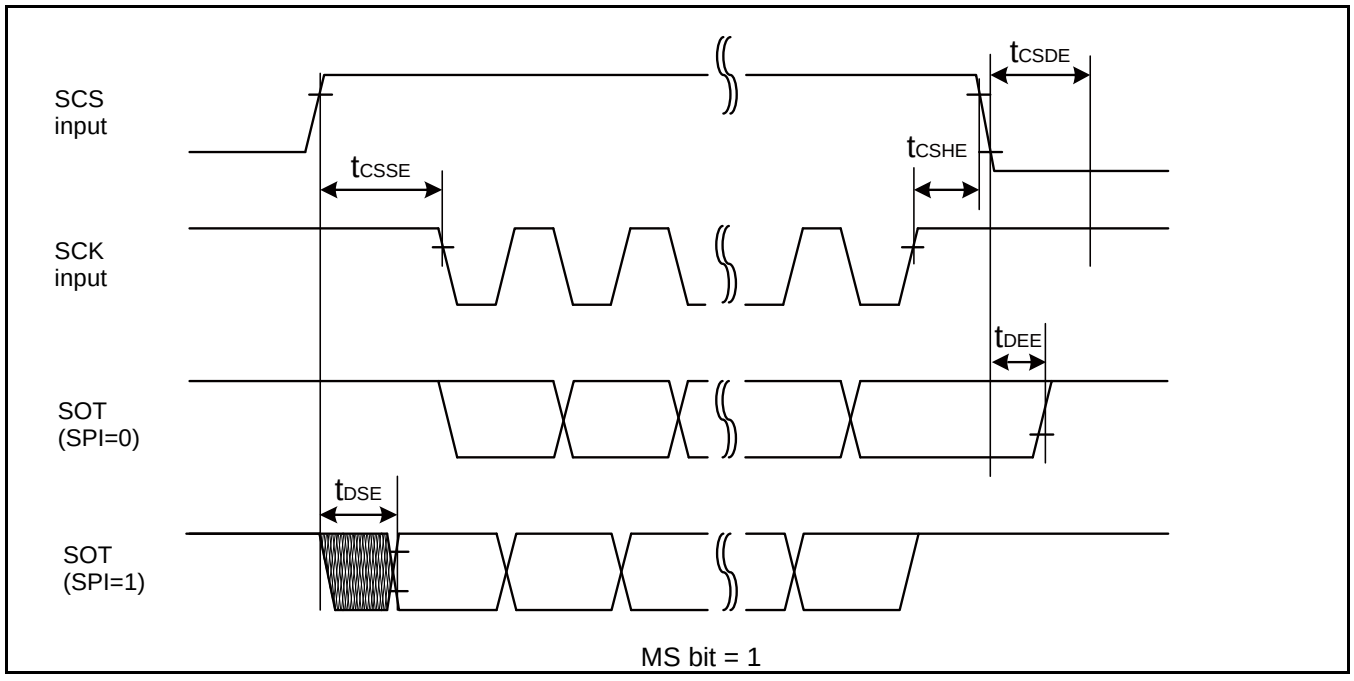
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

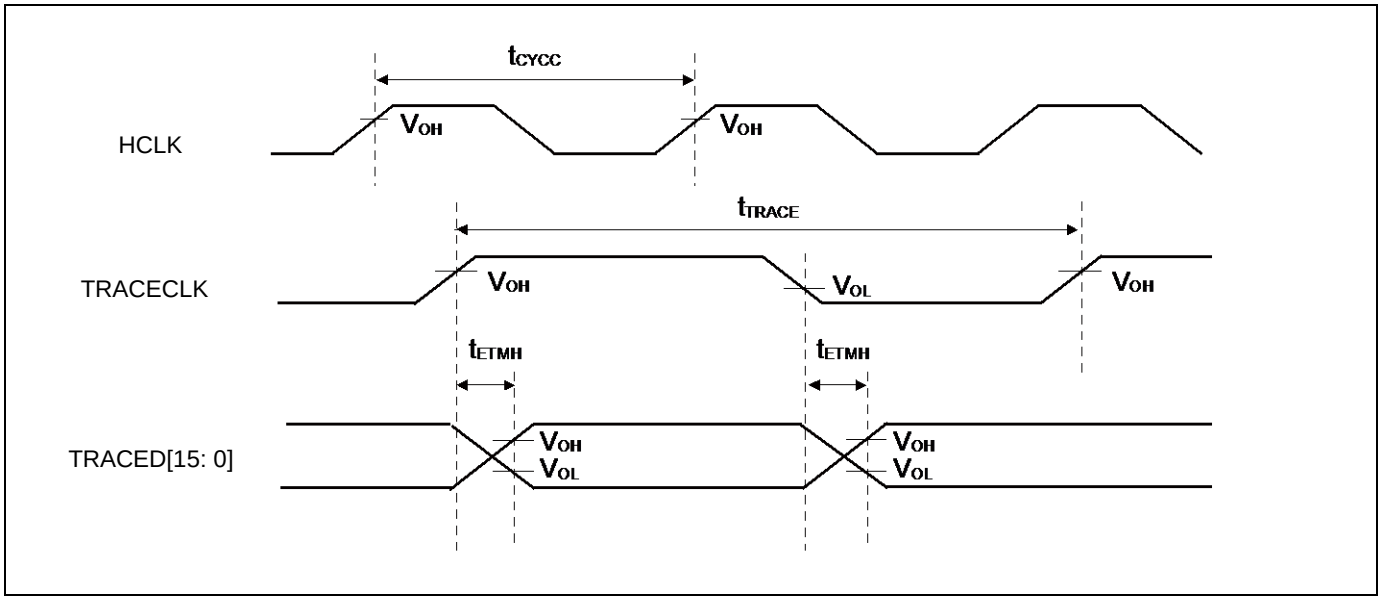
12.4.17 ETM/ HTM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	$V_{CC} \geq 4.5V$	2	9	ns	
			$V_{CC} < 4.5V$	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5V$		50	MHz	
			$V_{CC} < 4.5V$		32	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 4.5V$	20	-	ns	
			$V_{CC} < 4.5V$	31.25	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*



12.4.20 I²S Timing

Master Mode Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDJ}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

*: Except for the first bit of transmission frame

Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter 7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH – 15	-	AVRH + 15	mV	
			AV_{CC} - 15	-	AV_{CC} + 15	mV	
Conversion time	-	-	0.5*1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is when the value of Ts = 150 ns and Tc = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).

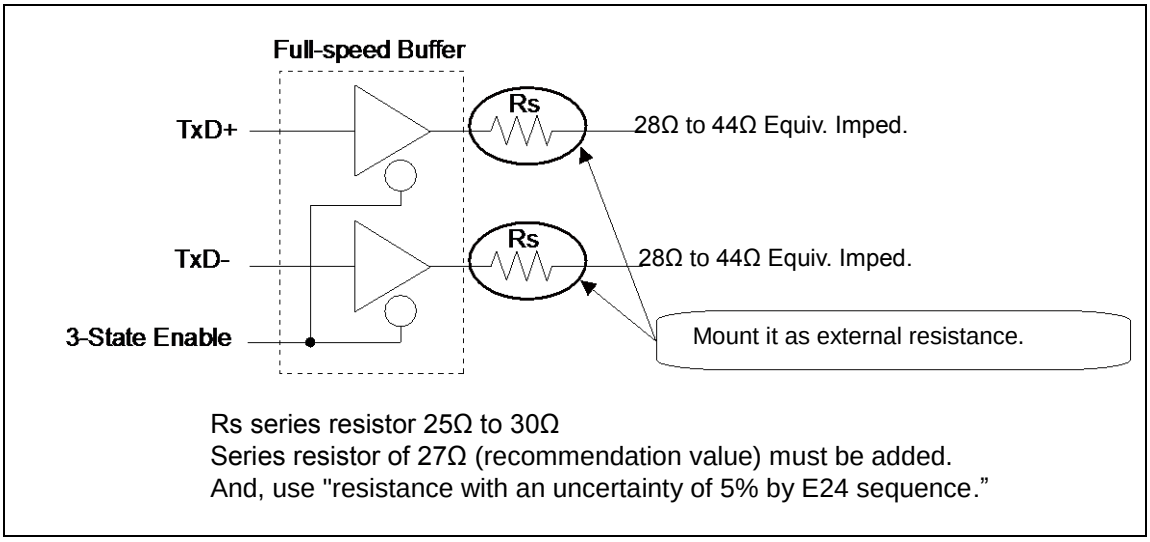
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 8. Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

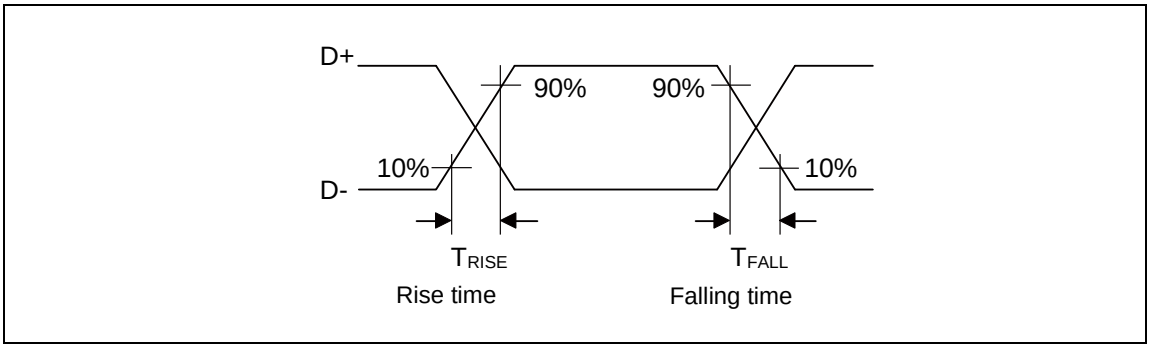
*2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).

*6: USB Full-speed connection is performed via twisted-pair cable shield with 90Ω ± 15% characteristic impedance (differential mode).
USB standard defines that the output impedance of the USB driver must be in the range from 28 Ω to 44 Ω. So, a discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommended value 27 Ω) series resistor Rs.



*7: They indicate rise time (t_{RISE}) and fall time (t_{FALL}) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.

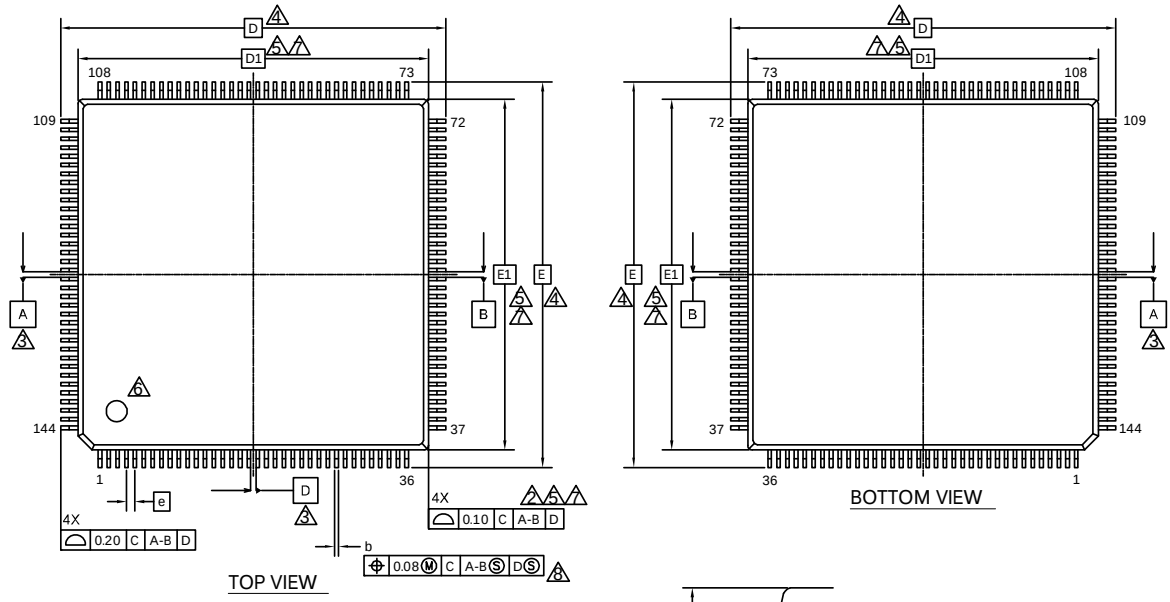


Note:

- *See Low-Speed Load (Compliance Load) for conditions of external load.*

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS 144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 **

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 Rev**

15. Major Changes

Spansion Publication Number: DS709-00009

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 0.2		
1, 3	Title	Added the following products. S6E2CC8HHA/S6E2CC9HHA/S6E2CCAHHA/ S6E2CC8JHA/S6E2CC9JHA/S6E2CCAJHA/ S6E2CC8LHA/S6E2CC9LHA/S6E2CCALHA
14	2.Feature	Added “Crypto Assist Function”
16, 17	3.Product Lineup	Added “Crypto Assist Function”
18	4.Packages	Added the following products. S6E2CC8HHA/S6E2CC9HHA/S6E2CCAHHA/ S6E2CC8JHA/S6E2CC9JHA/S6E2CCAJHA/ S6E2CC8LHA/S6E2CC9LHA/S6E2CCALHA
212	15.ORDERING INFORMATION	Added the following part numbers. S6E2CC8HHAGV20000/S6E2CC9HHAGV20000/S6E2CCAHHAGV20000/ S6E2CC8JHAGV20000/S6E2CC9JHAGV20000/S6E2CCAJHAGV20000/ S6E2CC8JHAGB10000/S6E2CC9JHAGB10000/S6E2CCAJHAGB10000/ S6E2CC8LHAGL20000/S6E2CC9LHAGL20000/S6E2CCALHAGL20000
Revision 0.3		
1, 3	Title	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
14	2.Features	Added Voice Function
15, 16	3.Product Lineup	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
17	4.Packages	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
211	15.Ordering Information	Added the following products. S6E2CCAJGAGV20000/ S6E2CC8JGAGB10000/ S6E2CC8JFAGB10000 S6E2CCAJGAGB10000/ S6E2CCAJFAGB10000
Revision 1.0		
7 15	2. Features 3. Product Lineup	Added that CAN-FD Interface supported non-CAN FD.
12 15 90 91	2. Features 3. Product Lineup 10. Block Diagram 12. Memory Map	Deleted HDM-CEC/Remote Control Receiver.
18-20	5. Pin Assignments	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Modified the pin name of I2S. (MI2S*_0→MI2S*0_0) Deleted the pin of IGTRG0_0.
22-24	6. Pin Descriptions	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Modified the pin name of I2S. (MI2S*_0→MI2S*0_0) Modified the pin number of PF7 in LQFP216.(91→90) Modified the pin number of X1. (73, 58, 50, P5→107, 87, 71, P13) Modified the pin number of X0A. (107, 87, 71, P13→73, 58, 50, P5)
75-82	7. I/O Circuit Type	Modified IOH/IOL of Type S.(IOH=-12mA→-10mA, IOL=12mA→10mA) Added the case of using I2C in Type E, F, G, L, N, S.
97-105	13. Pin Status In Each CPU State	Deleted X and Y in Pin Status Type.
106-107	14.1. Absolute Maximum Ratings	Added 10mA type.
108-112	14.2. Recommended Operating Conditions	Added AVRL in Analog reference voltage. Modified the mistake in Ethernet-MAC Pins. Modified the leakage current in Maximum leakage current at operating
113-122	14.3.1. Current Rating	Modified the maximum current of each category.

Page	Section	Change Results
123-124	14.3.2. Pin Characteristics	Added the characteristic of external bus in H level input voltage (hysteresis input). Added the characteristic of 10mA type.
127	14.4.5. Operating Conditions of USB/Ethernet PLL・I2S PLL (in the case of using main clock for input clock of PLL)	Modified the maximum of I2S PLL macro oscillation clock frequency. (307.2MHz→384MHz)
196	14.5.12-bit A/D Converter	Modified the minimum of Sampling time. Modified the characteristic of State transition time to operation permission Added AVRL in Analog reference voltage.
204	14.8.2. Interrupt of Low-Voltage Detection	Modified the SVHI values in Conditions

NOTE: Please see “Document History” about later revised information.