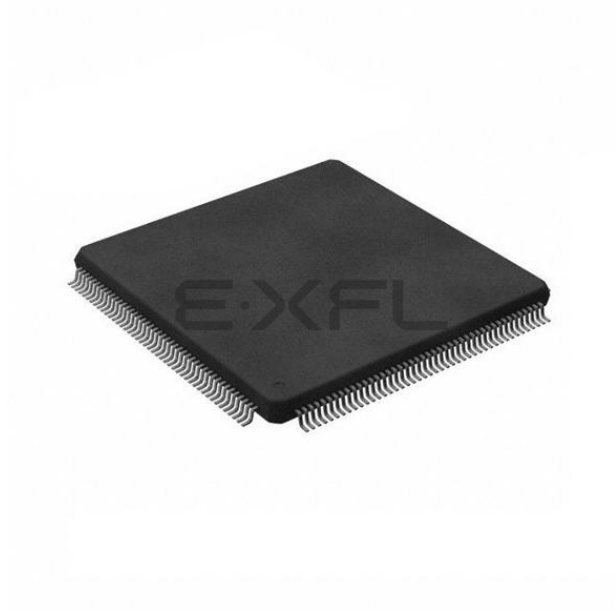

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2cc8j0agv2000a

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
106	86	70	P12	PE2 X0	A	A
107	87	71	P13	PE3 X1	A	B
108	88	72	N14	VSS	-	-
109	89	73	M14	VCC	-	-
110	90	74	M13	AVCC	-	-
111	91	75	M12	AVSS	-	-
112	92	76	L13	AVRL	-	-
113	93	77	L12	AVRH	-	-
114	94	78	L11	P10 AN00 SIN10_0 TIOA0_2 AIN0_2 INT08_0	F	M
115	95	79	K13	P11 AN01 SOT10_0 (SDA10_0) TIOB0_2 BIN0_2	F	L
116	96	80	K12	P12 AN02 SCK10_0 (SCL10_0) TIOA1_2 ZIN0_2	F	L
117	97	81	K14	P13 AN03 SIN6_1 RX1_1 INT25_1	F	M
118	98	82	K11	P14 AN04 SOT6_1 (SDA6_1) TX1_1	F	L
119	-	-	-	PB8 ADTG_6 SCS63_1 INT08_2 TRACED8	E	O
120	-	-	-	PB9 SIN9_1 AIN2_2 INT09_2 TRACED9	E	O
121	-	-	-	PBA SOT9_1 (SDA9_1) BIN2_2 TRACED10	E	N

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
190	158	128	A7	PCB INT28_0 E_COUT	L	W
191	159	129	C7	PCC E_TCK	K	V
192	160	130	A6	PCD SOT4_1 (SDA4_1) INT14_0 E_TXER	L	W
193	161	131	D7	PCE SIN4_1 INT15_0 E_TX03	L	W
194	162	132	E7	PCF RTS4_1 INT12_0 E_TX02	L	W
195	163	133	F7	PD0 INT30_1 E_TX01	L	W
196	164	134	B6	PD1 INT31_1 E_TX00	L	W
197	165	135	C6	PD2 CTS4_1 FRCK2_1 E_TXEN	L	V
198	166	136	D6	P6E ADTG_5 SCK4_1 (SCL4_1) IC23_1 INT29_0 E_PPS	E	W
199	-	-	-	P6D SCK14_1 (SCL14_1) IC22_1 TIOB6_2	E	I
200	-	-	-	P6C SOT14_1 (SDA14_1) IC21_1 TIOA6_2	E	I
201	-	-	-	P6B SIN14_1 IC20_1 TIOB7_2 INT14_2	E	K
202	-	-	-	P6A DTTI2X_1 TIOA7_2	E	I
203	-	-	-	P69 RTO20_1 (PPG20_1) TIOB14_2	E	I

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Ethernet	E_COL	Collision detection	186	154	124	F8
	E_COUT	Clock output for Ethernet PHY	190	158	128	A7
	E_CRS	Carrier detection	187	155	125	B7
	E_MDC	Management clock	184	152	122	E8
	E_MDIO	Management data I/O	183	151	121	D8
	E_PPS	PTP counter monitor	198	166	136	D6
	E_RX00	Received data0	181	149	119	F9
	E_RX01	Received data1	180	148	118	E9
	E_RX02	Received data2	179	147	117	D9
	E_RX03	Received data3	178	146	116	B8
	E_RXCK_REFCK	Received clock input/ Reference clock	185	153	123	A10
	E_RXDV	Received data enable	182	150	120	C8
	E_RXER	Received data error detection	177	145	115	C9
	E_TCK	Transition clock input	191	159	129	C7
	E_TX00	Transition data0	196	164	134	B6
	E_TX01	Transition data1	195	163	133	F7
	E_TX02	Transition data2	194	162	132	E7
	E_TX03	Transition data3	193	161	131	D7
	E_TXEN	Transition data enable	197	165	135	C6
	E_TXER	Transition data error detection	192	160	130	A6
I^2S	I2SMCLK0_0	I^2S external clock pin	51	41	-	L2
	I2SDO0_0	I^2S serial transition data output pin	52	42	-	L3
	I2SWS0_0	I^2S frame synchronization signal pin	53	43	-	M2
	I2SDI0_0	I^2S serial received data input pin	34	24	-	G6
	I2SCK0_0	I^2S bit clock pin	35	25	-	H4
High-speed quad SPI	Q_SCK_0	SPI clock output pin	173	143	-	D10
	Q_IO0_0	SPI data input/output pin	172	142	-	C10
	Q_IO1_0		171	141	-	B10
	Q_IO2_0		170	140	-	D11
	Q_IO3_0		169	139	-	C11
	Q_CS0_0	SPI chip select output pin	174	144	-	B9
	Q_CS1_0		175	-	-	-
	Q_CS2_0		176	-	-	-

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, flame

   CAUTION: Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected							GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/ input enabled

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7 *9	5.5	V	
Power supply voltage (for USB ch 0)		$USBV_{CC}0$	-	3.0	3.6 ($\leqV_{CC}$)	V	*1
				2.7	5.5 ($\leqV_{CC}$)		*2
Power supply voltage (for USB ch 1)		$USBV_{CC}1$	-	3.0	3.6 ($\leqV_{CC}$)	V	*3
				2.7	5.5 ($\leqV_{CC}$)		*4
Power supply voltage (for Ethernet-MAC)		$ETHV_{CC}$	-	3.0	3.6 ($\leqV_{CC}$)	V	*5
				4.5	5.5 ($\leqV_{CC}$)		*5
				2.7	5.5 ($\leqV_{CC}$)		*6
Power supply voltage (VBAT)		V_{BAT}	-	1.65	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	$AV_{CC} = V_{CC}$
Analog reference voltage		AVRH	-	*8	AV_{CC}	V	
		AVRL	-	AV_{SS}	AV_{SS}	V	
Operating temperature	Junction temperature	T_J	-	- 40	+ 125	°C	
	Ambient temperature	T_A	-	-40	*7	°C	

*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0)

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80)

*3: When P83/UDP1 and P82/UDM1 pins are used as USB (UDP1, UDM1)

*4: When P83/UDP1 and P82/UDM1 pins are used as GPIO (P83, P82)

*5: When the pins in Ethernet-MAC Pins, except P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pin

*6: When the pins in Ethernet-MAC Pins, except P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pin

*7: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).
The calculation formula of the ambient temperature (T_A) is:

$T_A (Max) = T_J(Max) - Pd(Max) \times \theta_{JA}$

Pd: Power dissipation (W)
θ_{JA}: Package thermal resistance (°C/W)

$Pd (Max) = V_{CC} \times I_{CC} (Max) + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (- I_{OH}))$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

*8: The minimum value of analog reference voltage depends on the value of compare clock cycle (Tcck). See 12.5. 12-bit A/D Converter for the details.

*9: For the voltage range between V_{CC}(min) and the low voltage detection reset (VDH), the MCU must be clocked from either the High-speed CR or the low-speed CR.

Current Explanation Diagram

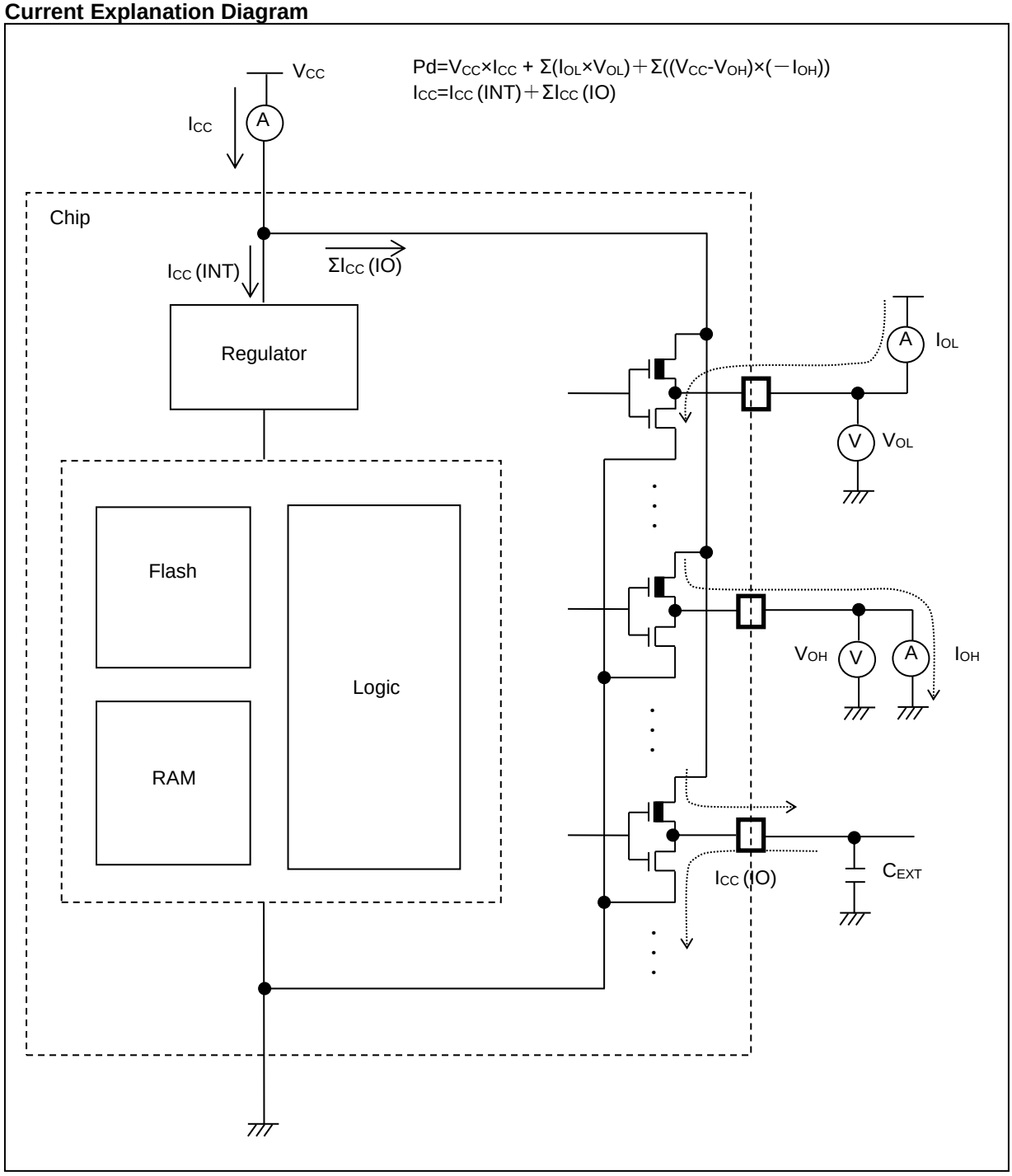


Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	200 MHz	128	236	mA	*3 When all peripheral clocks are on
					192 MHz	123	230	mA	
					180 MHz	116	221	mA	
				*6	160 MHz	102	205	mA	
					144 MHz	93	193	mA	
					120 MHz	79	175	mA	
					100 MHz	67	161	mA	
					80 MHz	54	145	mA	
					60 MHz	42	130	mA	
					40 MHz	30	115	mA	
					20 MHz	17	99	mA	
					8 MHz	9.2	90.0	mA	
					4 MHz	6.7	86.9	mA	
				*5	200 MHz	74	170	mA	*3 When all peripheral clocks are off
					192 MHz	71	167	mA	
					180 MHz	67	162	mA	
				*6	160 MHz	59	152	mA	
					144 MHz	53	145	mA	
					120 MHz	45	135	mA	
					100 MHz	39	127	mA	
					80 MHz	32	118	mA	
					60 MHz	25	110	mA	
					40 MHz	18	101	mA	
					20 MHz	11	92	mA	
					8 MHz	6.5	86.8	mA	
					4 MHz	5.1	85.0	mA	

*1: T_A = +25 °C, V_{CC} = 3.3 V

*2: T_J = +125 °C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

*7: With data access to a MainFlash memory.

*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
			$ETHV_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5$ V, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 4 mA					
			$ETHV_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$RTHV_{CC} < 4.5$ V, I_{OL} = 4 mA					
		10 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 10 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5$ V, I_{OL} = 18.5 mA	V_{SS}	-	0.4	V	*1
			$USBV_{CC} < 4.5$ V, I_{OL} = 10.5 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OL} = 3 mA					
			$V_{CC} \leq 4.5$ V, I_{OL} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, USBVCC0, USBVCC1, ETHVCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

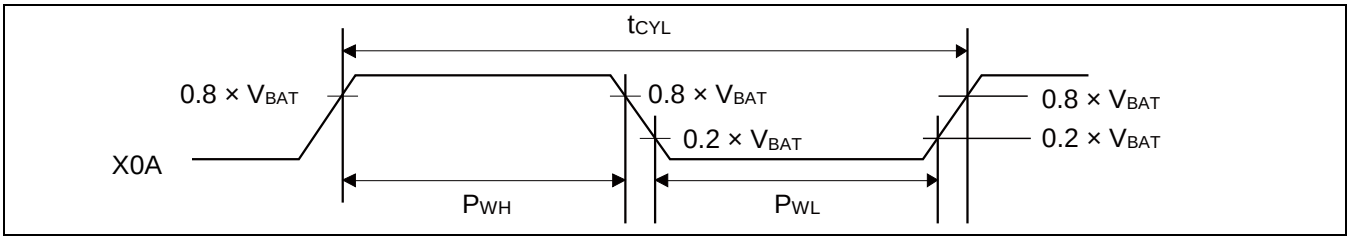
*1: $USBV_{CC}0$ and $USBV_{CC}1$ are described as $USBV_{CC}$.

12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 1.65V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 7. Handling Devices.



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = - 20°C to + 105°C	3.92	4	4.08	MHz	When trimming *1
		T_J = - 40°C to + 125°C	3.88	4	4.12		
		T_J = - 40°C to + 125°C	3	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

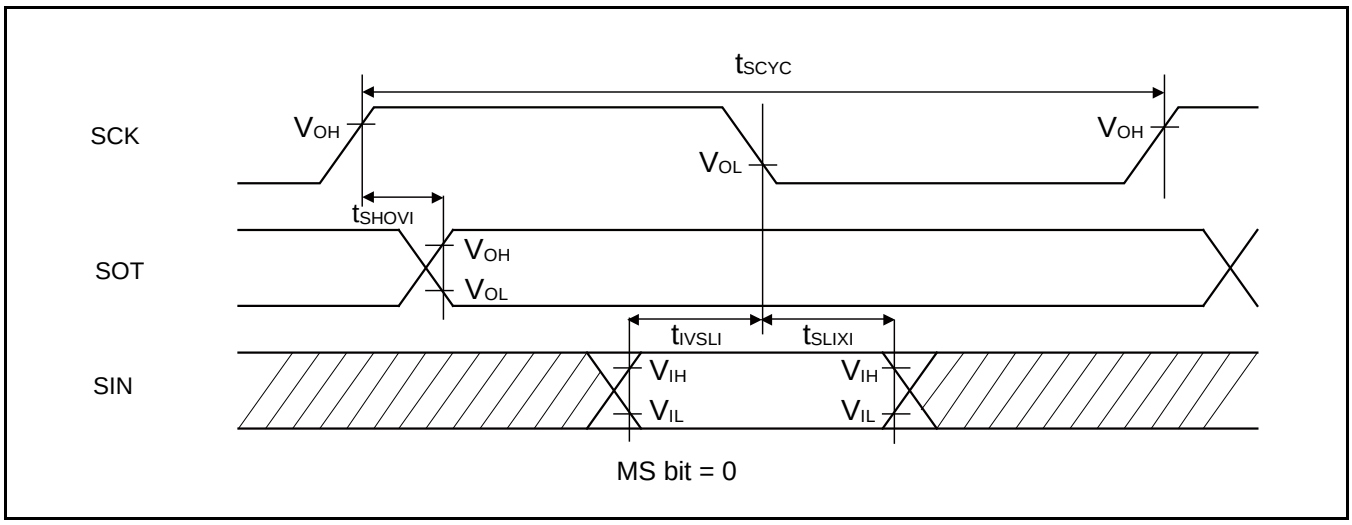
*1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

*2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

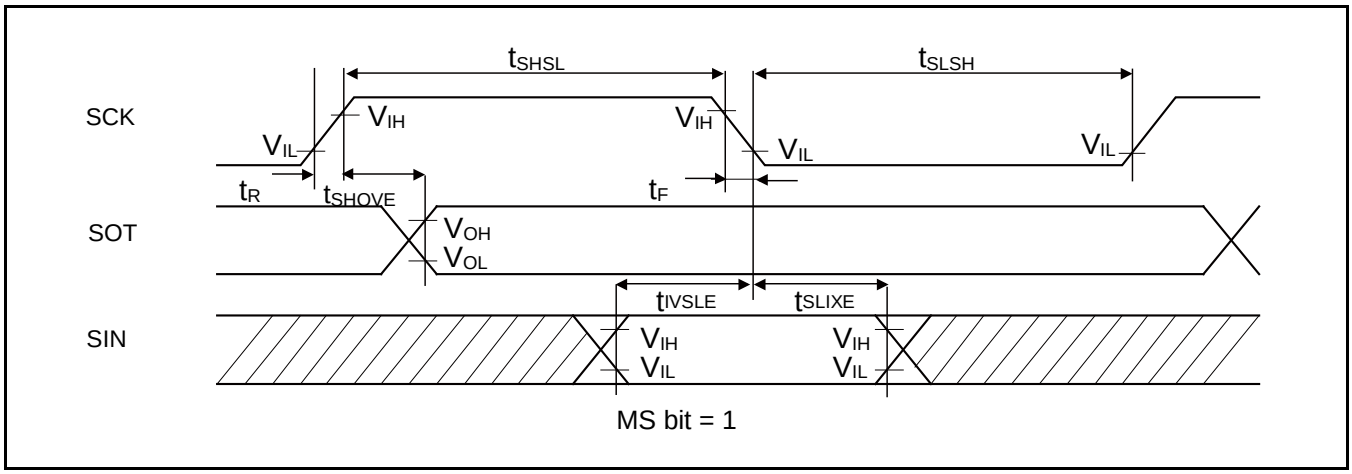
Built-In Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

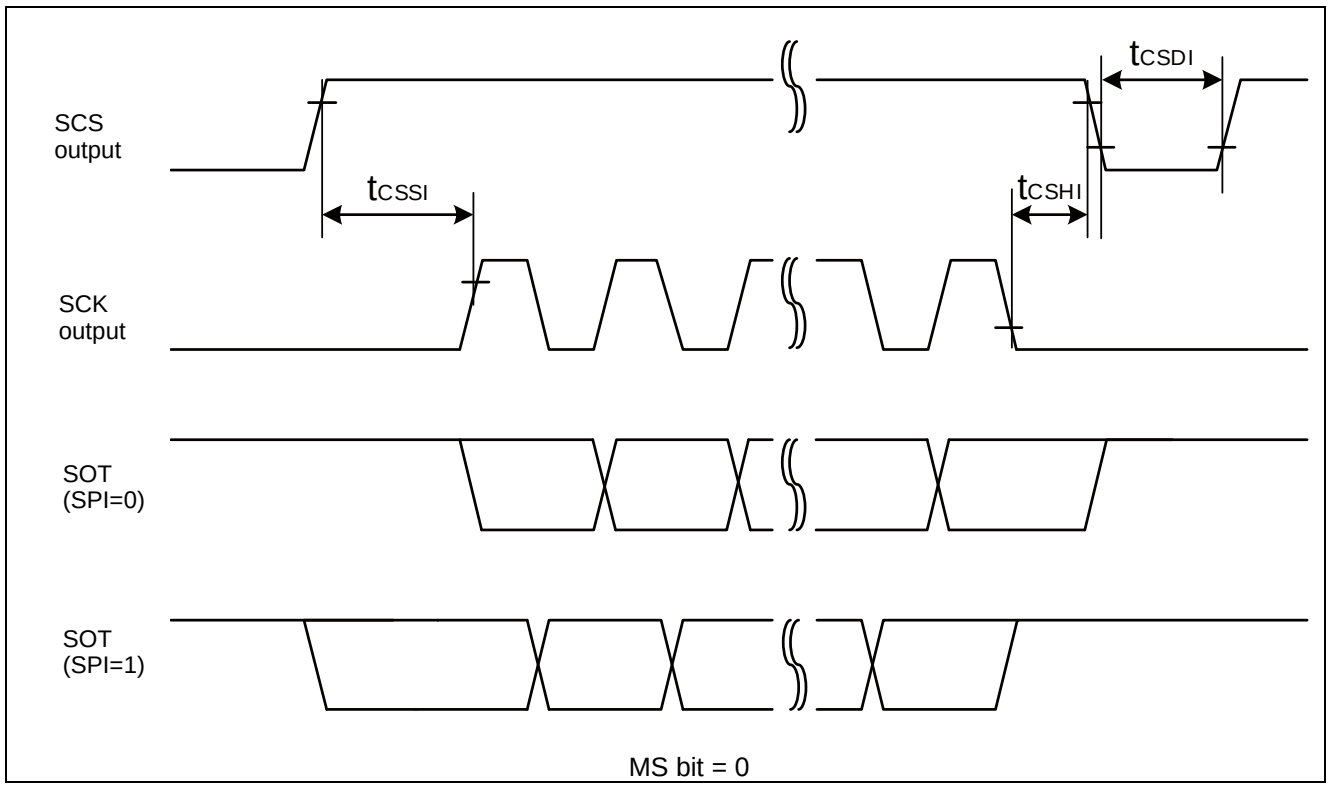
Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	



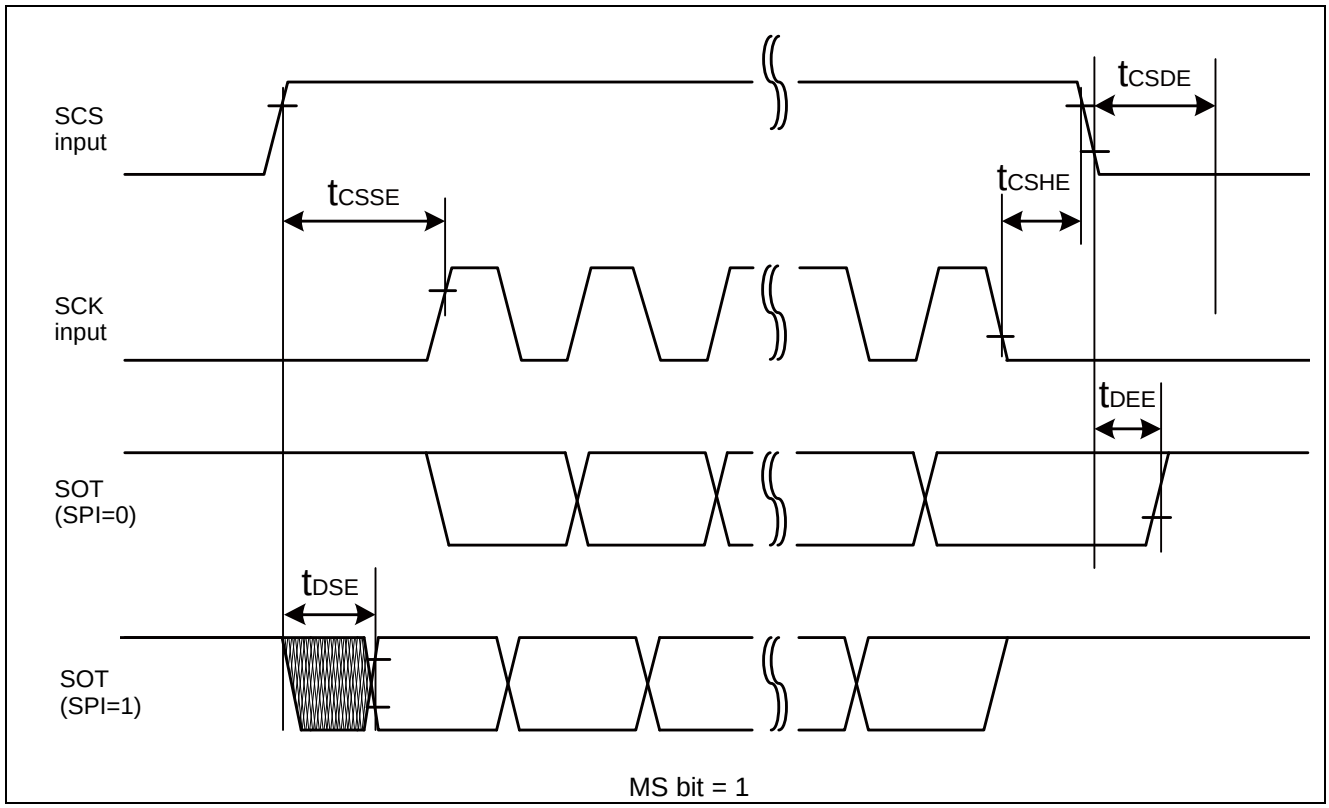
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

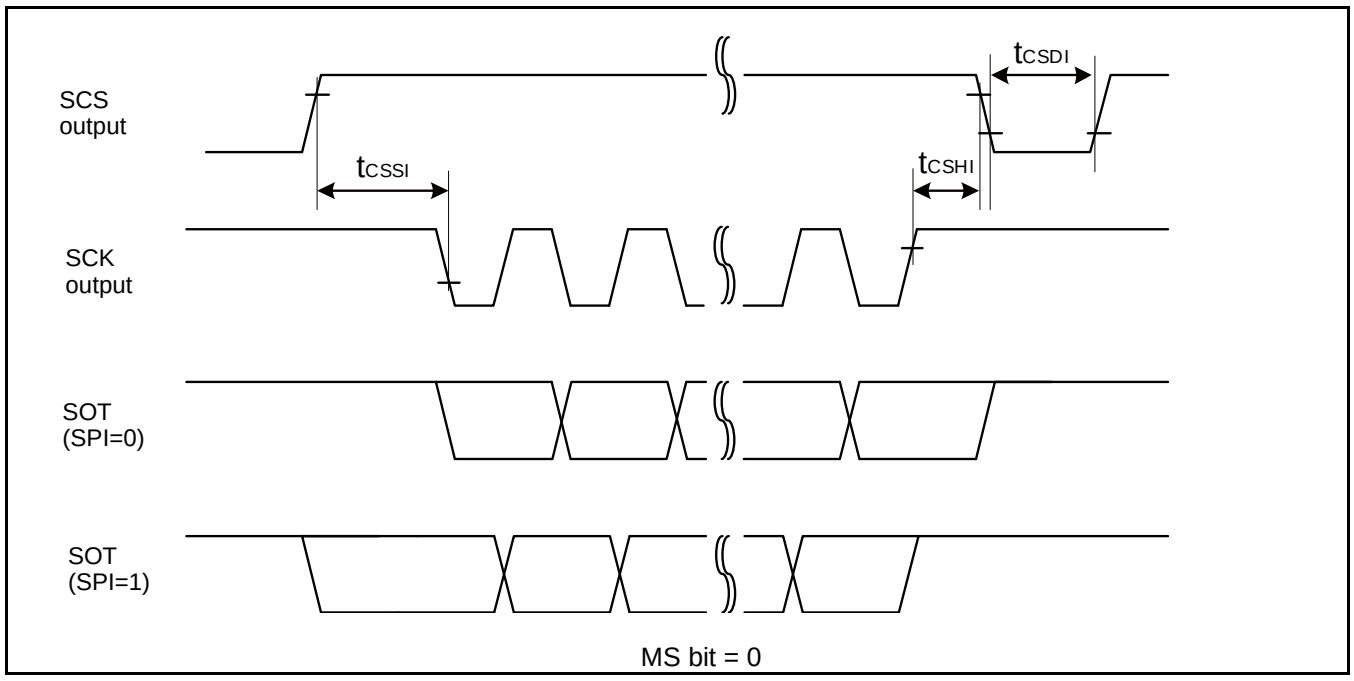
High-Speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

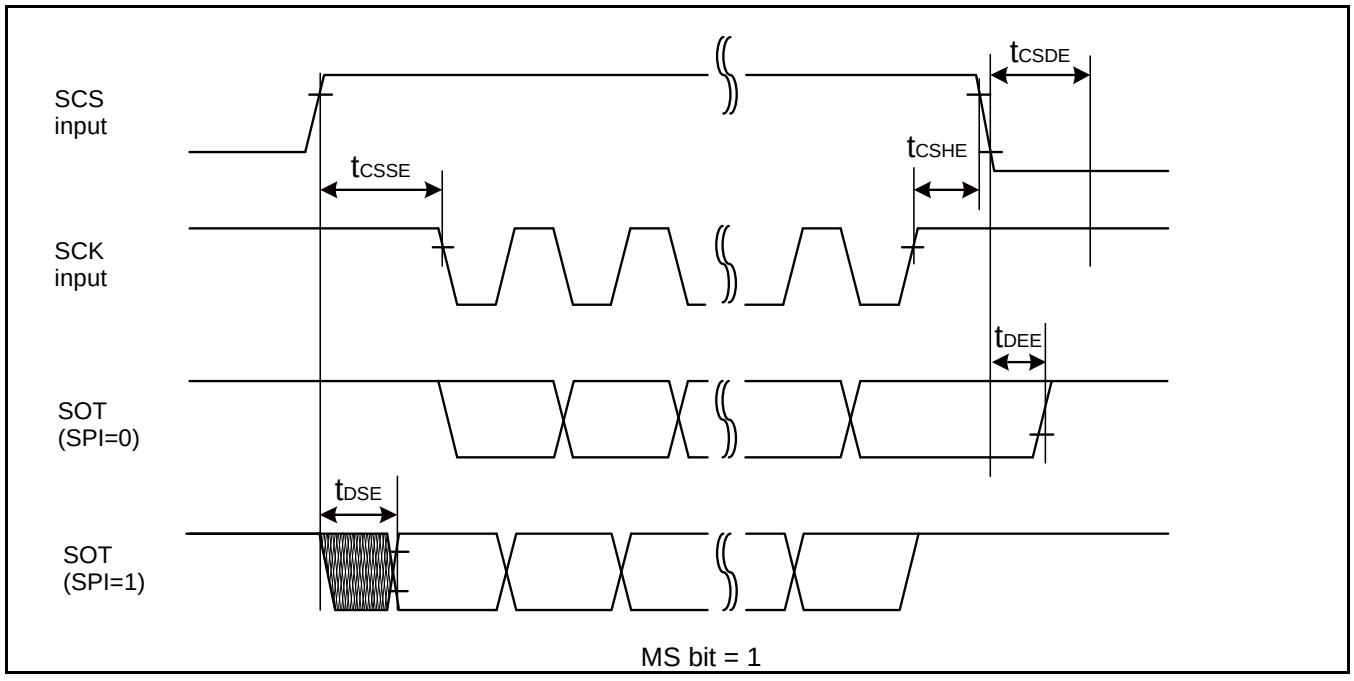
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*
  No chip select: SIN4_0, SOT4_0, SCK4_0
  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (for *, when C_L = 10 pF)*



MS bit = 0

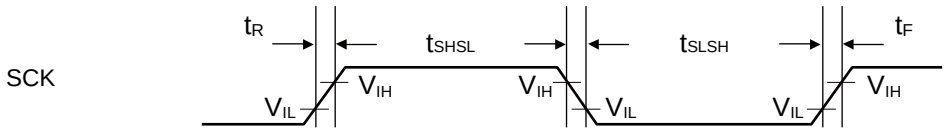


MS bit = 1

External Clock (EXT = 1): When in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	t_F		-	5	ns	
SCK rise time	t_R		-	5	ns	



High-speed mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1card)	0	50	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rise time	t_{TLH}	S_CLK		-	3	ns
Clock fall time	t_{THL}	S_CLK		-	3	ns

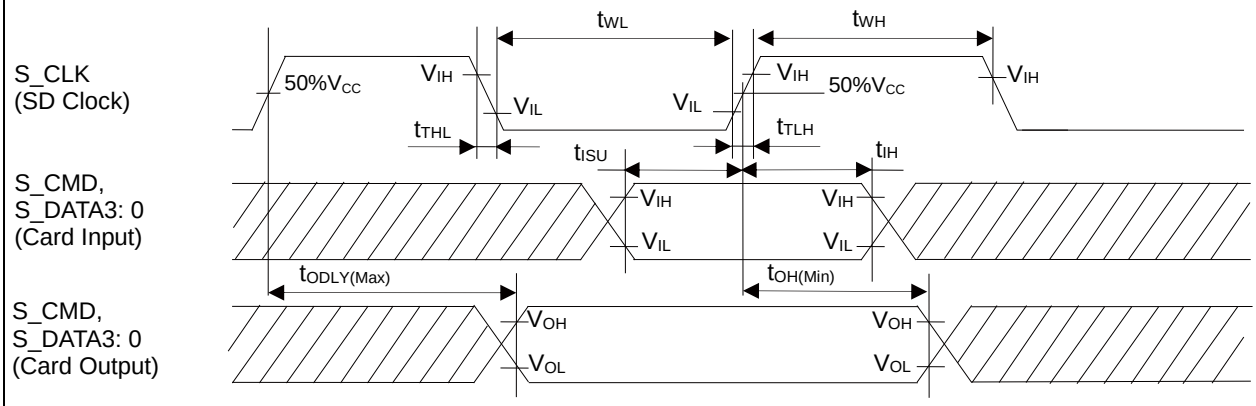
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1card)	6	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output delay time during data transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_L ≤ 40 pF (1card)	0	14	ns
Output hold time	t_{OH}	S_CMD, S_DATA3: 0	C_L ≥ 15 pF (1card)	2.5	-	ns
Total system capacitance for each line*	C_L	-	1card	-	40	pF

*: In order to satisfy severe timing, host shall drive only one card.



High-speed mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH – 15	-	AVRH + 15	mV	
			AV_{CC} - 15	-	AV_{CC} + 15	mV	
Conversion time	-	-	0.5*1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

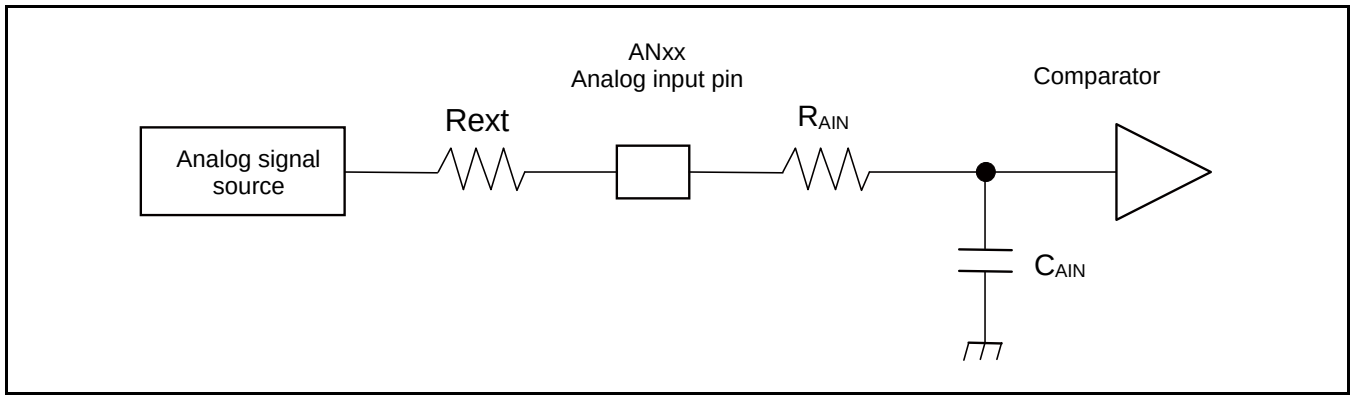
The condition of the minimum conversion time is when the value of Ts = 150 ns and Tc = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 8. Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.2 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V

Input resistance of A/D = 1.8 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 12.05 pF at 2.7 V ≤ AV_{CC} ≤ 5.5 V

R_{ext}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

12.8.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	$6000 \times t_{CYCP}$ *	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

Page	Section	Change Results
123-124	14.3.2. Pin Characteristics	Added the characteristic of external bus in H level input voltage (hysteresis input). Added the characteristic of 10mA type.
127	14.4.5. Operating Conditions of USB/Ethernet PLL・I2S PLL (in the case of using main clock for input clock of PLL)	Modified the maximum of I2S PLL macro oscillation clock frequency. (307.2MHz→384MHz)
196	14.5.12-bit A/D Converter	Modified the minimum of Sampling time. Modified the characteristic of State transition time to operation permission Added AVRL in Analog reference voltage.
204	14.8.2. Interrupt of Low-Voltage Detection	Modified the SVHI values in Conditions

NOTE: Please see “Document History” about later revised information.