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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	192-LFBGA
Supplier Device Package	192-FBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2cc8jfagb1000a

Low-power Consumption mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32-kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Crypto Assist Function

These features are enabled for the crypto assist function. The dedicated middleware is necessary for this calculator operation.

- PKA (Public Key Accelerator)
 - PKA (Public Key Accelerator) is modular exponentiation calculation accelerator used of RSA Public Key crypto and so on.
 - Available bit length: Up to 2048-bit
- AES calculator
 - AES (Advanced Encryption Standard) calculator is a AES common key crypto accelerator which is compliant with FIPS (Federal Information Processing Standard Publication) 197.
 - Available key length: 128/192/256-bit
 - CBC mode and ECB mode support
- SHA-256 calculator
 - SHA-256 calculator is a SHA-256 hash function accelerator which is compliant with FIPS180-2.
- External Bus Data Scramble
 - It enables to scramble input/output data of External Bus Interface.

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

- Five power supplies
 - Wide range voltage:
VCC = 2.7 V to 5.5 V
 - Power supply for USB ch 0 I/O:
USBVCC0 = 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
 - Power supply for USB ch 1 I/O:
USBVCC1 = 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
 - Power supply for Ethernet-MAC I/O:
ETHVCC = 3.0 V to 5.5 V (when Ethernet is used.)
= 2.7 V to 5.5 V (when GPIO is used)
 - Power supply for VBAT:
VBAT = 1.65 V to 5.5 V

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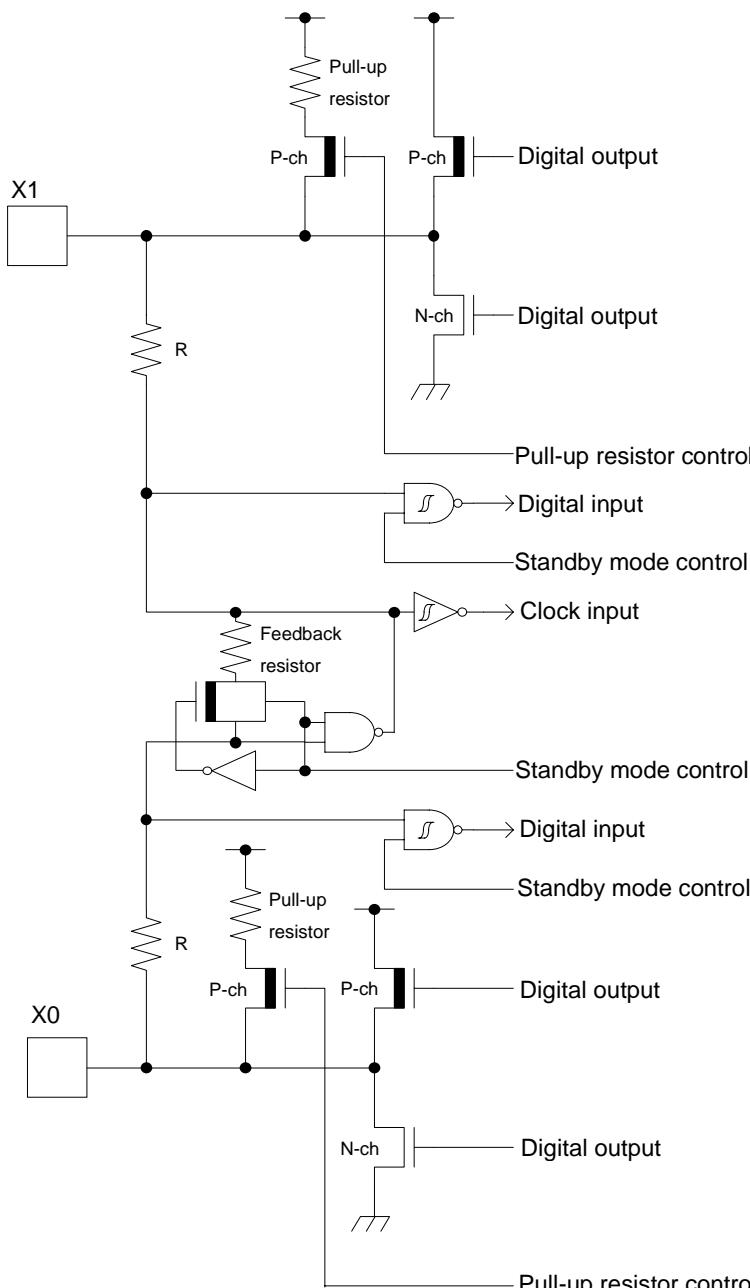
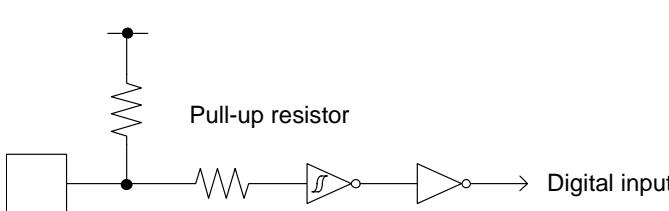
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
69	-	-	-	P4E	E	I
				SCS73_1		
				TX2_2		
70	55	47	L5	P7D	L	Q
				SCK1_1 (SCL1_1)		
				RX2_0		
				DTTI1X_0		
				INT05_0		
				WKUP2		
				MCSX1_0		
71	56	48	M5	P7E	L	I
				ADTG_7		
				TX2_0		
				FRCK1_0		
				MCSX0_0		
72	57	49	N5	INITX	B	C
73	58	50	P5	P46	P	S
				X0A		
74	59	51	P6	P47	Q	T
				X1A		
75	60	52	P8	VBAT	-	-
76	61	53	N6	P48	O	U
				VREGCTL		
77	62	54	M6	P49	O	U
				VWAKEUP		
78	63	-	K5	PF0	E	K
				SCS63_0		
				RX2_1		
				FRCK1_1		
				TIOA15_1		
				INT22_1		
79	64	-	K6	PF1	E	K
				SCS62_0		
				TX2_1		
				TIOB15_1		
				INT23_1		
80	65	55	L6	P70	I	K
				ADTG_8		
				SIN1_1		
				INT06_0		
				MRDY_0		
81	66	56	J6	P71	E	I
				SOT1_1 (SDA1_1)		
				MAD00_0		
				P72		
82	67	57	L8	SIN9_0	E	K
				TIOB0_0		
				INT07_0		
				MAD01_0		
				P73		
83	68	58	K8	SOT9_0 (SDA9_0)	E	I
				TIOB1_0		
				MAD02_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
216	176	144	B1	VSS	-	-
-	-	-	E1		-	-
-	-	-	G1		-	-
-	-	-	P7		-	-
-	-	-	P11		-	-
-	-	-	L14		-	-
-	-	-	A11		-	-
-	-	-	A5		-	-
-	-	-	N7		-	-
-	-	-	M7		-	-
-	-	-	L7		-	-
-	-	-	K7		-	-
-	-	-	J7		-	-
--	-	-	G7		-	-
-	-	-	H7		-	-
-	-	-	H8		-	-
-	-	-	G8		-	-

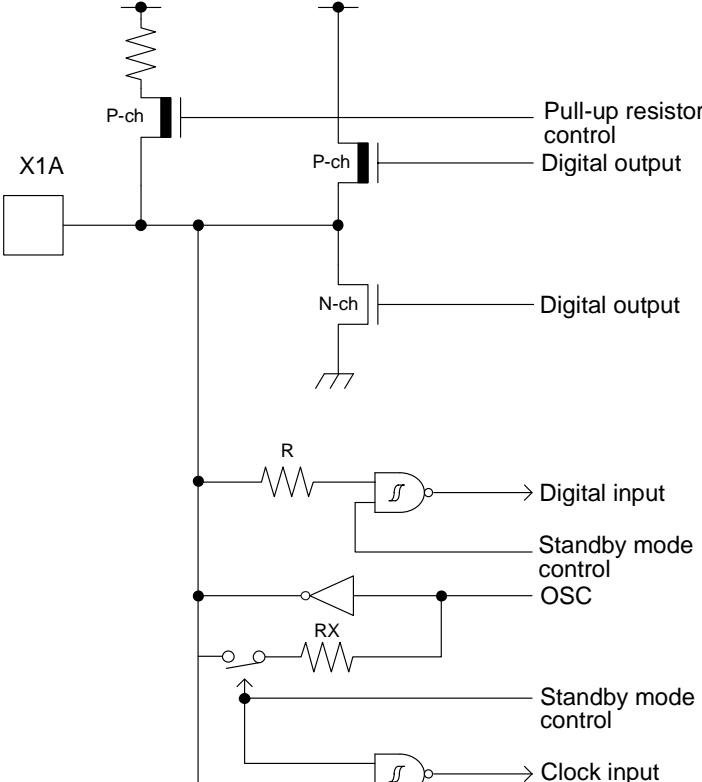
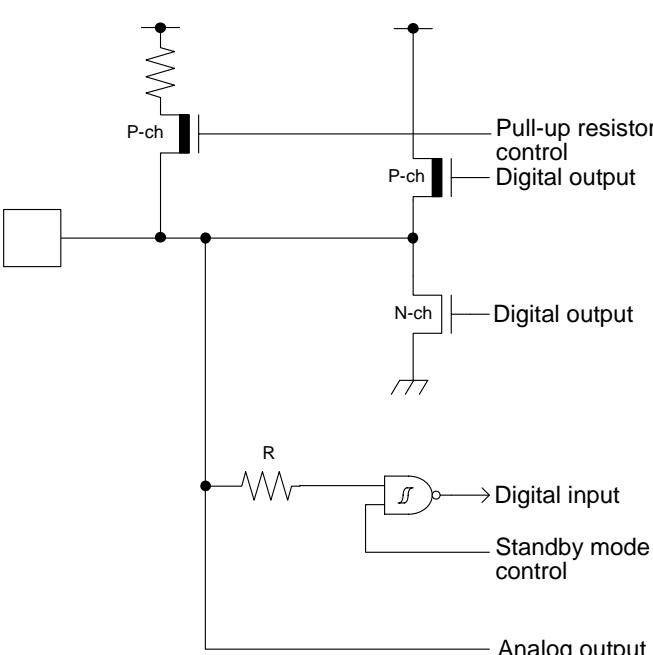
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi- Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I ² C (operation mode 4).	146	120	96	F12
	SOT5_1 (SDA5_1)		171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I ² C (operation mode 4).	145	119	95	F11
	SCK5_1 (SCL5_1)		172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi- Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I ² C (operation mode 4).	97	80	64	K10
	SOT6_1 (SDA6_1)		118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I ² C (operation mode 4).	98	81	65	M10
	SCK6_1 (SCL6_1)		126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi- Function Timer 0	DTTIOX_0	Input signal controlling waveform generator outputs RTO00 to RTO05 of Multi-Function Timer 0.	44	34	29	J3
	DTTIOX_1		21	-	-	-
	FRCK0_0	16-bit free-run timer ch 0 external clock input pin	37	27	22	J1
	FRCK0_1		29	-	-	-
	IC00_0	16-bit input capture input pin of Multi-Function Timer 0. ICxx describes channel number.	43	33	28	J4
	IC00_1		22	-	-	-
	IC01_0		42	32	27	J5
	IC01_1		26	-	-	-
	IC02_0		41	31	26	H6
	IC02_1		27	-	-	-
	IC03_0		38	28	23	H3
	IC03_1		28	-	-	-
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	45	35	30	J2
	RTO00_1 (PPG00_1)		10	10	-	E2
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	46	36	31	K1
	RTO01_1 (PPG00_1)		11	11	-	E3
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	47	37	32	K2
	RTO02_1 (PPG02_1)		12	12	-	E4
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	48	38	33	K3
	RTO03_1 (PPG02_1)		13	-	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	49	39	34	K4
	RTO04_1 (PPG04_1)		19	-	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	50	40	35	L1
	RTO05_1 (PPG04_1)		20	-	-	-

5. I/O Circuit Type

Type	Circuit	Remarks
A	 <p>Detailed description of Type A circuit:</p> <ul style="list-style-type: none"> X1 Oscillator: Input X1 is connected to a feedback resistor R. The output of the oscillator is connected to a digital output (P-ch and N-ch PMOS transistors), a pull-up resistor control, a digital input, a standby mode control, and a clock input. X0 Oscillator: Input X0 is connected to a feedback resistor R. The output of the oscillator is connected to a digital output (P-ch and N-ch PMOS transistors), a pull-up resistor control, a digital input, and a standby mode control. Feedback Resistors: Feedback resistors R are connected between the outputs of X1 and X0. Pull-up Resistor Control: Pull-up resistor control logic is present between the two oscillators. Digital Inputs: Digital inputs are present between the two oscillators. Standby Mode Control: Standby mode control logic is present between the two oscillators. Clock Input: Clock input logic is present between the two oscillators. 	<p>It is possible to select the main oscillation/GPIO function.</p> <p>When the main oscillation is selected:</p> <ul style="list-style-type: none"> Oscillation feedback resistor: approximately 1 MΩ Standby mode control <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> CMOS level output. CMOS level hysteresis input Pull-up resistor control Standby mode control Pull-up resistor: approximately 50 kΩ $I_{OH} = -4 \text{ mA}, I_{OL} = 4 \text{ mA}$
B	 <p>Detailed description of Type B circuit:</p> <ul style="list-style-type: none"> Pull-up Resistor: A pull-up resistor is connected to the digital input. Digital Input: The digital input is connected through a buffer to a digital output. 	<ul style="list-style-type: none"> CMOS level hysteresis input Pull-up resistor: approximately 50 kΩ

Type	Circuit	Remarks
C	<p>Digital input</p> <p>Digital output</p>	<ul style="list-style-type: none"> Open drain output CMOS level hysteresis input
E	<p>Digital output</p> <p>N-ch</p> <p>P-ch</p> <p>P-ch</p> <p>Digital output</p> <p>Pull-up resistor control</p> <p>Digital input</p> <p>Standby mode control</p>	<ul style="list-style-type: none"> CMOS level output CMOS level hysteresis input Pull-up resistor control Standby mode control Pull-up resistor: approximately 50 kΩ $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
F	<p>Digital output</p> <p>N-ch</p> <p>P-ch</p> <p>P-ch</p> <p>Digital output</p> <p>Pull-up resistor control</p> <p>Digital input</p> <p>Standby mode control</p> <p>R</p> <p>Analog input</p> <p>Input control</p> <p>Digital output</p> <p>Standby mode control</p>	<ul style="list-style-type: none"> CMOS level output CMOS level hysteresis input Input control Analog input Pull-up resistor control Standby mode control Pull-up resistor: approximately 50 kΩ $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ When this pin is used as an I²C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
Q	 <p>The circuit diagram for Type Q shows a dual-channel digital output stage. Each channel consists of a P-channel MOSFET and an N-channel MOSFET connected to a common drain. A pull-up resistor is connected between the drains and ground. The gates of the P-channel MOSFETs are connected to the outputs of two inverters. The inputs of these inverters are connected to a digital input through a resistor, a standby mode control path, and an oscillator (OSC) path. The oscillator path includes an inverter, a transmission gate, and a resistor labeled RX. There is also a feedback path from the oscillator output back to the digital input. The outputs of the inverter gates are labeled "Digital output".</p>	<p>It is possible to select the sub oscillation/GPIO function.</p> <p>When the sub oscillation is selected:</p> <ul style="list-style-type: none"> • Oscillation feedback resistor: approximately 10 MΩ <p>When the GPIO is selected:</p> <ul style="list-style-type: none"> • CMOS level output. • CMOS level hysteresis input • Pull-up resistor control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856).
R	 <p>The circuit diagram for Type R is similar to Type Q but includes an additional analog output stage. The analog output is generated by a transmission gate controlled by a digital signal. The rest of the circuit is identical to Type Q, featuring a dual-channel digital output stage with pull-up resistors, a digital input stage with hysteresis, and various control and oscillation paths.</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • Analog output • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ (4.5V to 5.5V) • $I_{OH} = -2 \text{ mA}$, $I_{OL} = 2 \text{ mA}$ (2.7V to 4.5V)

Notes on Power-On

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(B) in FM4 Family Peripheral Manual Main Part(002-04856).

Turning on: VBAT → VCC → USBVCC0
 VBAT → VCC → USBVCC1
 VBAT → VCC → EHVCC
 VCC → AVCC → AVRH
Turning off: AVRH → AVCC → VCC
 EHVCC → VCC → VBAT
 USBVCC1 → VCC → VBAT
 USBVCC0 → VCC → VBAT

Serial Communication

There is a possibility of receiving incorrect data as a result of noise or other issues introduced by the serial communication. Take care to design the printed circuit board to minimize noise.

Consider the case of introducing error as a result of noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Characteristics within the Product Line

The electric characteristics including power consumption, ESD, latch-up, noise, and oscillation differ among members of the product line because chip layout and memory structures are not the same; for example, different sizes, flash versus ROM, etc. If you are switching to a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Pin Doubled as Debug Function

The pin doubled as TDO/TMS/TDI/TCK/TRSTX, SWO/SWDIO/SWCLK should be used as output only. Do not use as input.

12.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V _{CC}	-	2.7 ^{*9}	5.5	V	
Power supply voltage (for USB ch 0)	USBV _{CC0}	-	3.0	3.6 (≤V _{CC})	V	*1
			2.7	5.5 (≤V _{CC})		*2
Power supply voltage (for USB ch 1)	USBV _{CC1}	-	3.0	3.6 (≤V _{CC})	V	*3
			2.7	5.5 (≤V _{CC})		*4
Power supply voltage (for Ethernet-MAC)	ETHV _{CC}	-	3.0	3.6 (≤V _{CC})	V	*5
			4.5	5.5 (≤V _{CC})		*5
			2.7	5.5 (≤V _{CC})		*6
Power supply voltage (VBAT)	V _{BAT}	-	1.65	5.5	V	
Analog power supply voltage	A _{VCC}	-	2.7	5.5	V	A _{VCC} = V _{CC}
Analog reference voltage	AVRH	-	*8	A _{VCC}	V	
	AVRL	-	A _{VSS}	A _{VSS}	V	
Operating temperature	Junction temperature	T _J	- 40	+ 125	°C	
	Ambient temperature	T _A	-40	*7	°C	

*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0)

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80)

*3: When P83/UDP1 and P82/UDM1 pins are used as USB (UDP1, UDM1)

*4: When P83/UDP1 and P82/UDM1 pins are used as GPIO (P83, P82)

*5: When the pins in Ethernet-MAC Pins, except P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pin

*6: When the pins in Ethernet-MAC Pins, except P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pin

*7: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).

The calculation formula of the ambient temperature (T_A) is:

$$T_A(\text{Max}) = T_J(\text{Max}) - P_d(\text{Max}) \times \theta_{JA}$$

Pd: Power dissipation (W)

θ_{JA}: Package thermal resistance (°C/W)

$$P_d(\text{Max}) = V_{CC} \times I_{CC}(\text{Max}) + \sum (I_{OL} \times V_{OL}) + \sum ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current

I_{OH}: H level output current

V_{OL}: L level output voltage

V_{OH}: H level output voltage

*8: The minimum value of analog reference voltage depends on the value of compare clock cycle (T_{cck}). See 12.5. 12-bit A/D Converter for the details.

*9: For the voltage range between V_{CC(min)} and the low voltage detection reset (VDH), the MCU must be clocked from either the High-speed CR or the low-speed CR.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$P_d = V_{cc} \times I_{cc} + \sum (I_{OL} \times V_{OL}) + \sum ((V_{cc} - V_{OH}) \times (-I_{OH}))$$

I_{OL} : L level output current

I_{OH} : H level output current

V_{OL} : L level output voltage

V_{OH} : H level output voltage

I_{cc} is the current drawn by the device.

It can be analyzed as follows.

$$I_{cc} = I_{cc} (\text{INT}) + \sum I_{cc} (\text{IO})$$

I_{cc} (INT): Current drawn by internal logic and memory, etc. through the regulator

$\sum I_{cc}$ (IO): Sum of current (I/O switching current) drawn by the output pin

For I_{cc} (INT), it can be anticipated by "(1) Current Rating" in "12.3. DC Characteristics" (This rating value does not include I_{cc} (IO) for a value at pin fixed).

For I_{cc} (IO), it depends on system used by customers.

The calculation formula is shown below.

$$I_{cc} (\text{IO}) = (C_{\text{INT}} + C_{\text{EXT}}) \times V_{cc} \times f_{sw}$$

C_{INT} : Pin internal load capacitance
 C_{EXT} : External load capacitance of output pin
 f_{sw} : Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{cc} (Max) as follows when the power dissipation can be evaluated by yourself:

Measure current value I_{cc} (Typ) at normal temperature (+25°C).

Add maximum leakage current value I_{cc} (leak_max) at operating on a value in (1).

$$I_{cc}(\text{Max}) = I_{cc}(\text{Typ}) + I_{cc}(\text{leak_max})$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	$I_{cc}(\text{leak_max})$	$T_J = +125^{\circ}\text{C}$	79.2 mA
		$T_J = +105^{\circ}\text{C}$	39.4 mA
		$T_J = +85^{\circ}\text{C}$	26.5 mA

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, TIMER Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks	
					Typ* ¹	Max* ²			
Power supply current	I _{CCH}	V _{CC}	Stop mode	-	0.56	3.01	mA	* ³ , * ⁴ $T_A = +25^\circ C$	
					-	27.03	mA	* ³ , * ⁴ $T_A = +85^\circ C$	
					-	39.92	mA	* ³ , * ⁴ $T_A = +105^\circ C$	
	I _{CCT}		Timer mode ^{*⁵} (main oscillation)	4 MHz	1.40	3.85	mA	* ³ , * ⁴ $T_A = +25^\circ C$	
					-	27.87	mA	* ³ , * ⁴ $T_A = +85^\circ C$	
					-	40.76	mA	* ³ , * ⁴ $T_A = +105^\circ C$	
	I _{CR}		Timer mode (built-in High-speed CR)	4 MHz	0.95	3.40	mA	* ³ , * ⁴ $T_A = +25^\circ C$	
					-	27.42	mA	* ³ , * ⁴ $T_A = +85^\circ C$	
					-	40.31	mA	* ³ , * ⁴ $T_A = +105^\circ C$	
	I _{CL}		Timer mode ^{*⁶} (sub oscillation)	32 kHz	0.57	3.02	mA	* ³ , * ⁴ $T_A = +25^\circ C$	
					-	27.04	mA	* ³ , * ⁴ $T_A = +85^\circ C$	
					-	39.93	mA	* ³ , * ⁴ $T_A = +105^\circ C$	
	I _{CR}		Timer mode (built-in low-speed CR)	100 kHz	0.58	3.03	mA	* ³ , * ⁴ $T_A = +25^\circ C$	
					-	27.05	mA	* ³ , * ⁴ $T_A = +85^\circ C$	
					-	39.94	mA	* ³ , * ⁴ $T_A = +105^\circ C$	
	I _{CCR}		RTC mode ^{*⁵} (sub oscillation)	32 kHz	0.57	3.02	mA	* ³ , * ⁴ $T_A = +25^\circ C$	
					-	27.04	mA	* ³ , * ⁴ $T_A = +85^\circ C$	
					-	39.93	mA	* ³ , * ⁴ $T_A = +105^\circ C$	

*¹: V_{CC} = 3.3 V

*²: V_{CC} = 5.5 V

*³: When all ports are fixed

*⁴: When LVD is off

*⁵: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

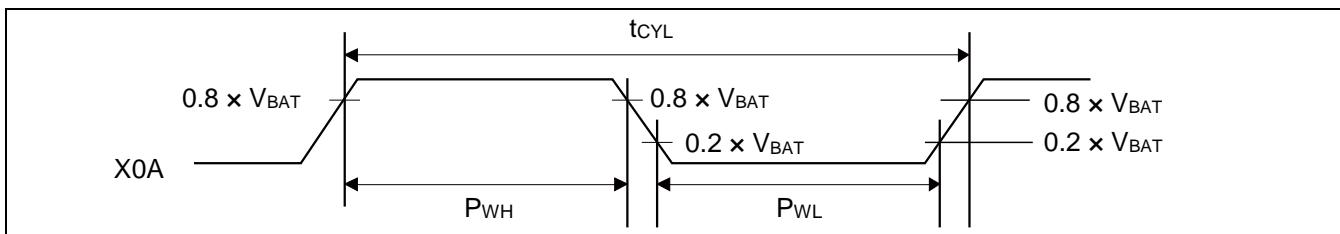
*⁶: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.4.2 Sub Clock Input Characteristics

($V_{BAT} = 1.65V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/tCYLL	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
			-	10	-	31.25	μs	When using external clock
Input clock pulse width	-		PWH/tCYLL, PWL/tCYLL	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 7. Handling Devices.



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	$T_J = -20^{\circ}C$ to $+105^{\circ}C$	3.92	4	4.08	MHz	When trimming *1
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	3.88	4	4.12		
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	3	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	μs	*2

*1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

*2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

Built-In Low-speed CR

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

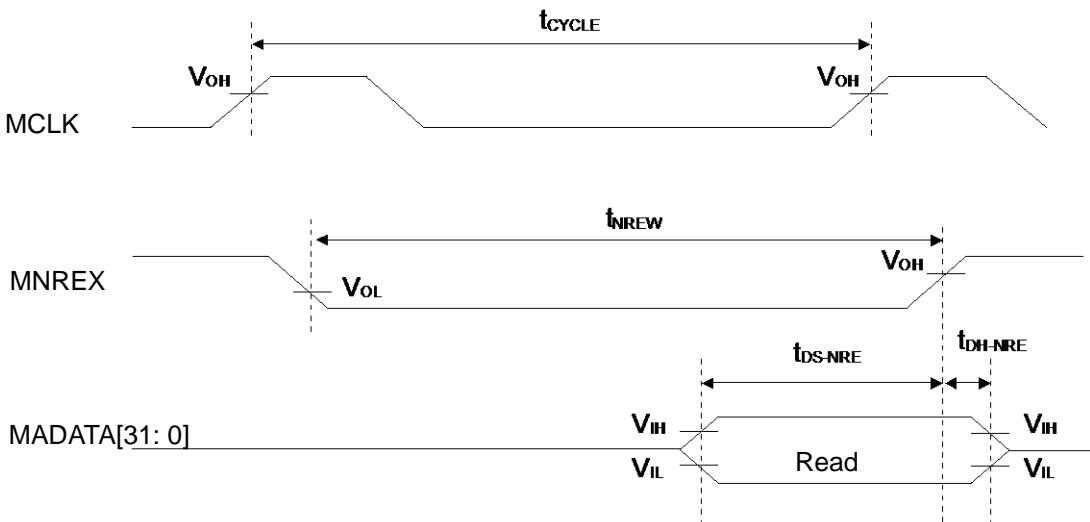
Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

NAND Flash Mode
 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t_{NREW}	MNREX	-	MCLK $\times n$ -3	-	ns	
Data set up \rightarrow MNREX \uparrow time	t_{DS-NRE}	MNREX, MADATA[31: 0]	-	20	-	ns	
MNREX \uparrow \rightarrow Data hold time	t_{DH-NRE}	MNREX, MADATA[31: 0]	-	0	-	ns	
MNALE \uparrow \rightarrow MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	-	MCLK $\times m$ -9	MCLK $\times m$ +9	ns	
MNALE \downarrow \rightarrow MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	-	MCLK $\times m$ -9	MCLK $\times m$ +9	ns	
MNCLE \uparrow \rightarrow MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	-	MCLK $\times m$ -9	MCLK $\times m$ +9	ns	
MNWEX \uparrow \rightarrow MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	-	0	MCLK $\times m$ +9	ns	
MNWEX Min pulse width	t_{NWEW}	MNWEX	-	MCLK $\times n$ -3	-	ns	
MNWEX \downarrow \rightarrow Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[31: 0]	-	-9	9	ns	
MNWEX \uparrow \rightarrow Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[31: 0]	-	0	MCLK $\times m$ +9	ns	

Note:

- When the external load capacitance $C_L = 30 \text{ pF}$ ($m = 0 \text{ to } 15, n = 1 \text{ to } 16$)

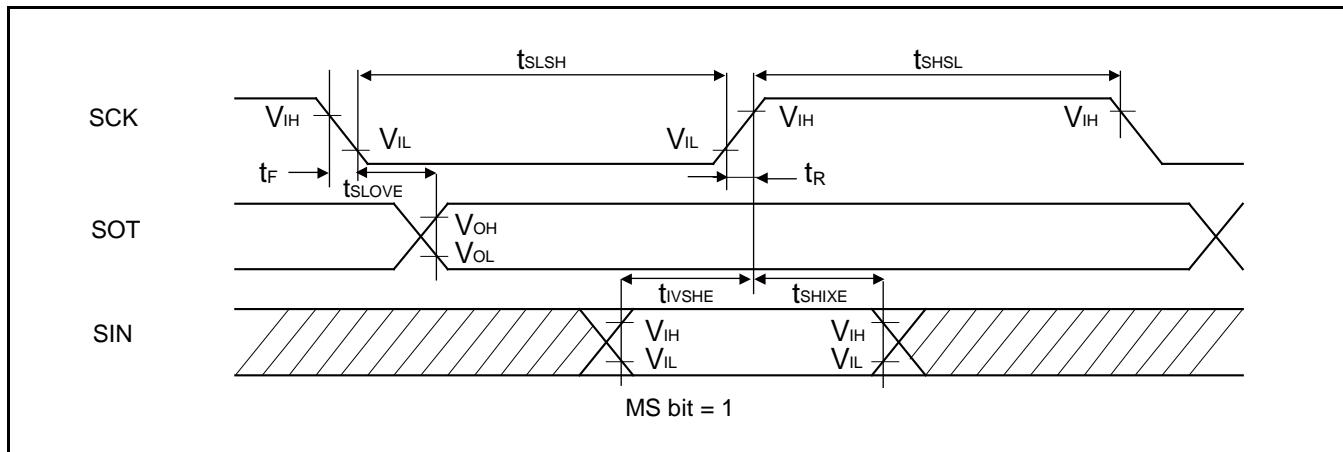
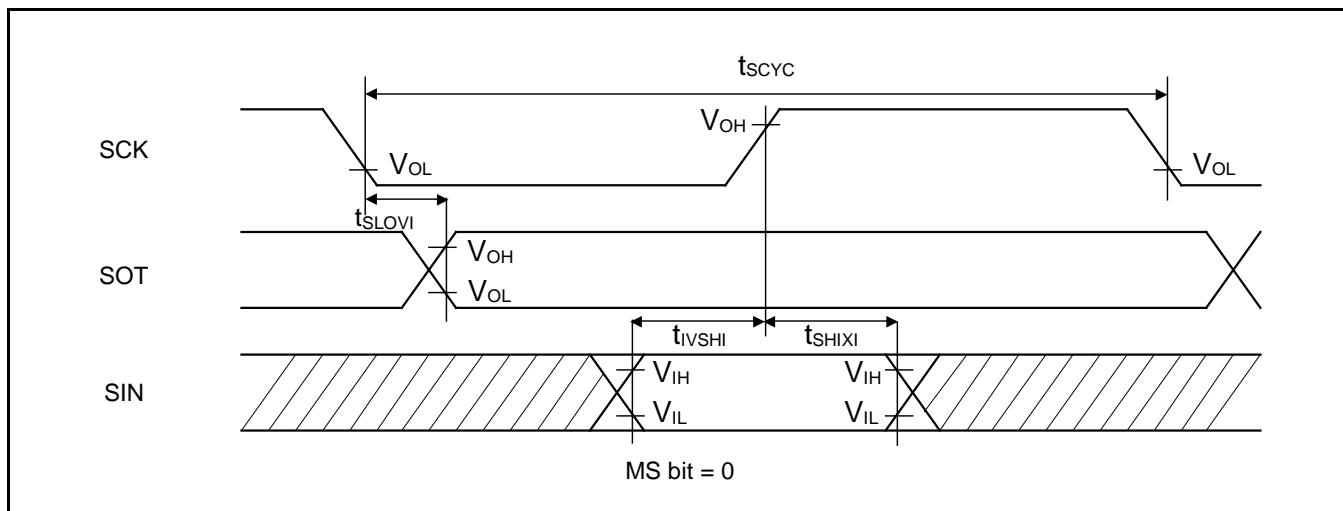
NAND Flash Read


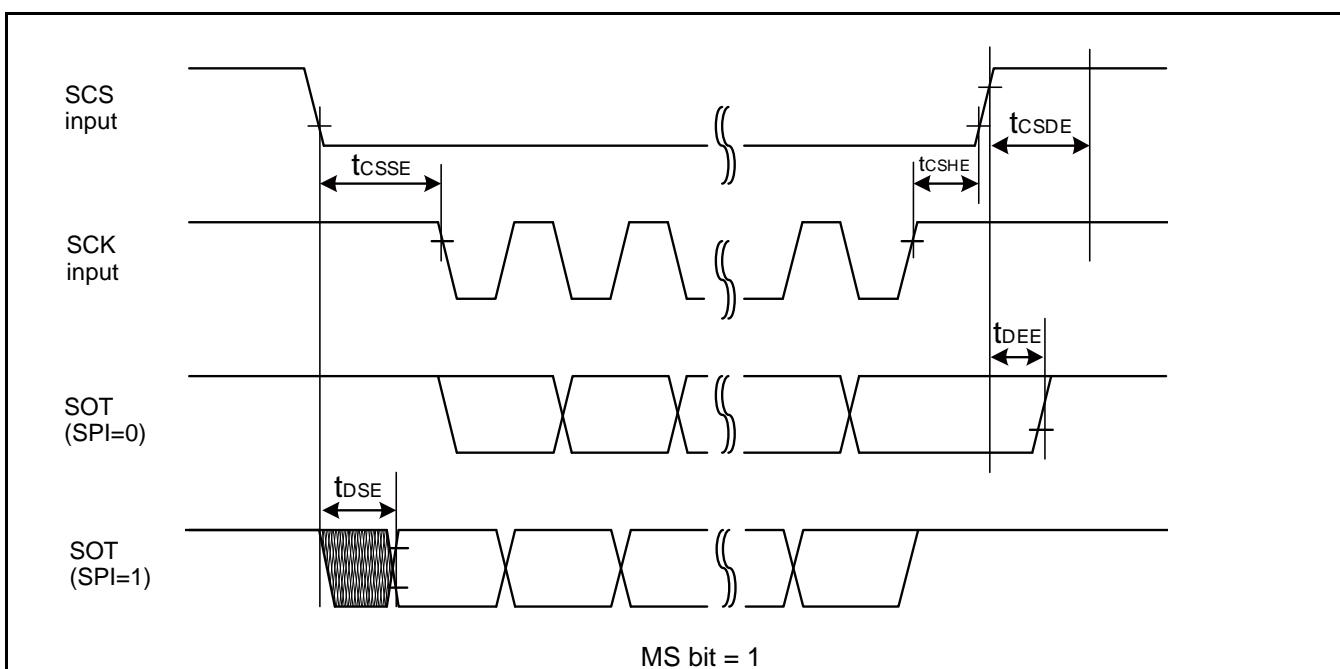
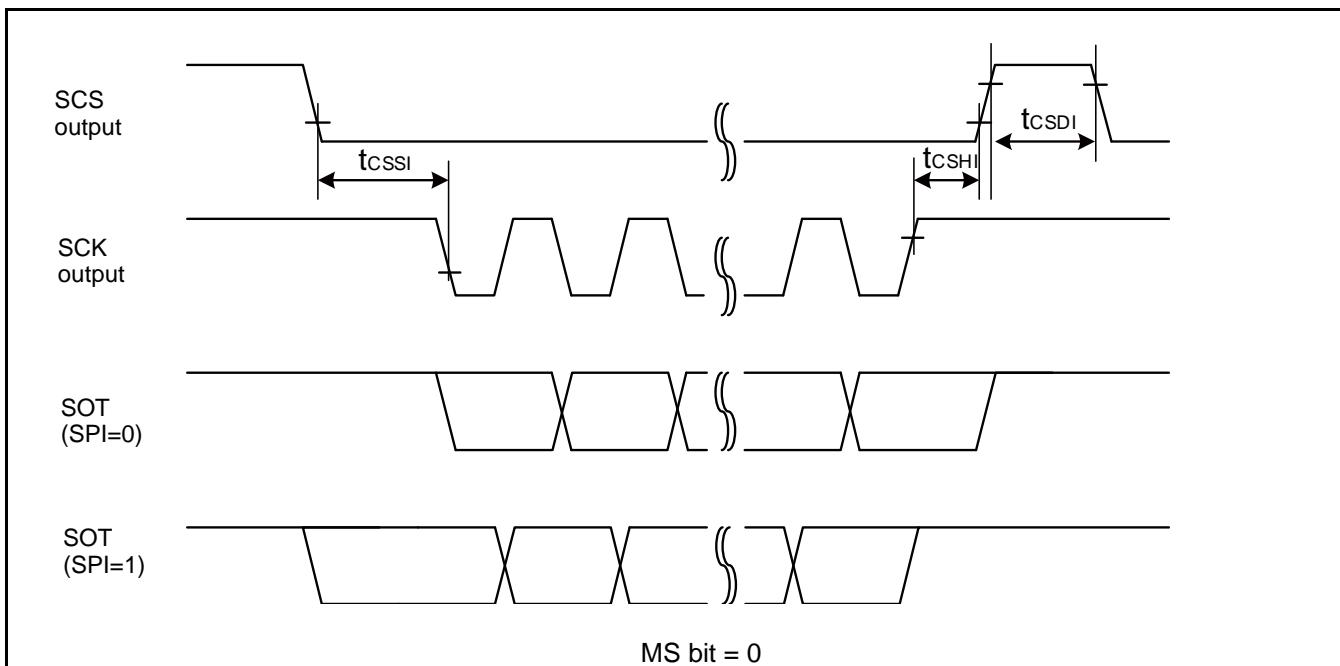
12.4.12 CSIO (SPI) Timing
Synchronous Serial (SPI = 0, SCINV = 0)
 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V)$

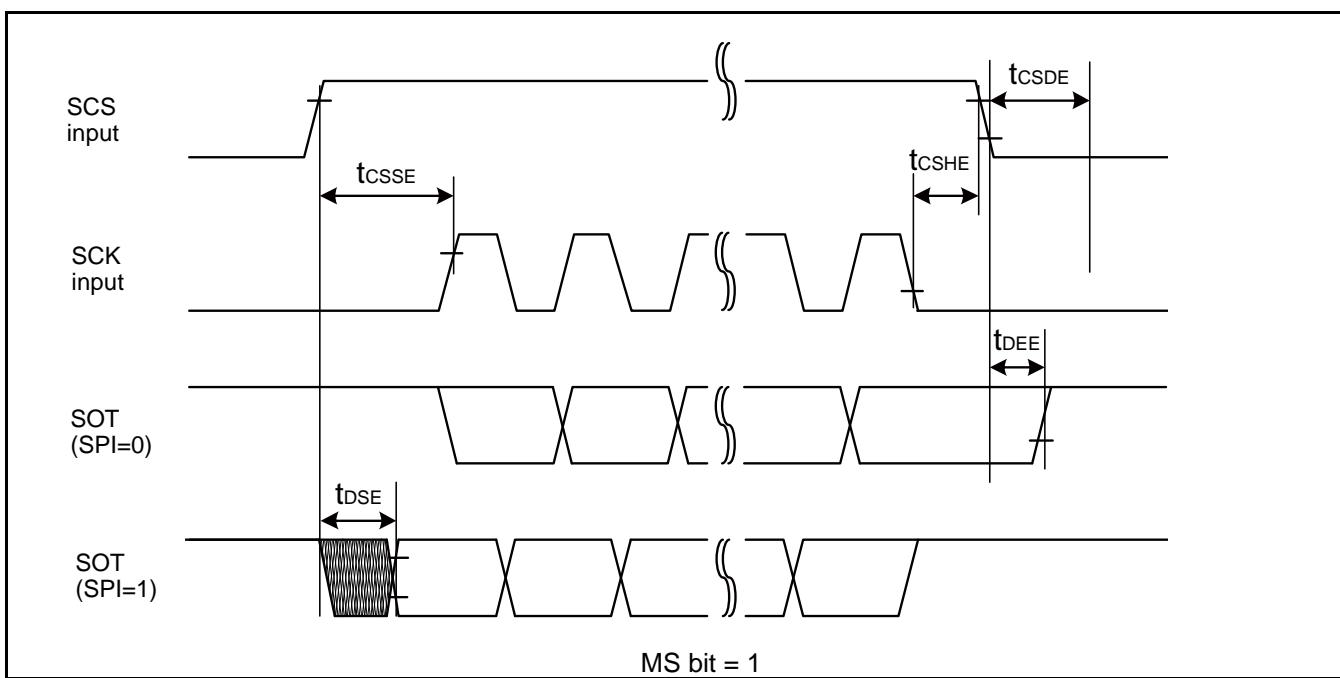
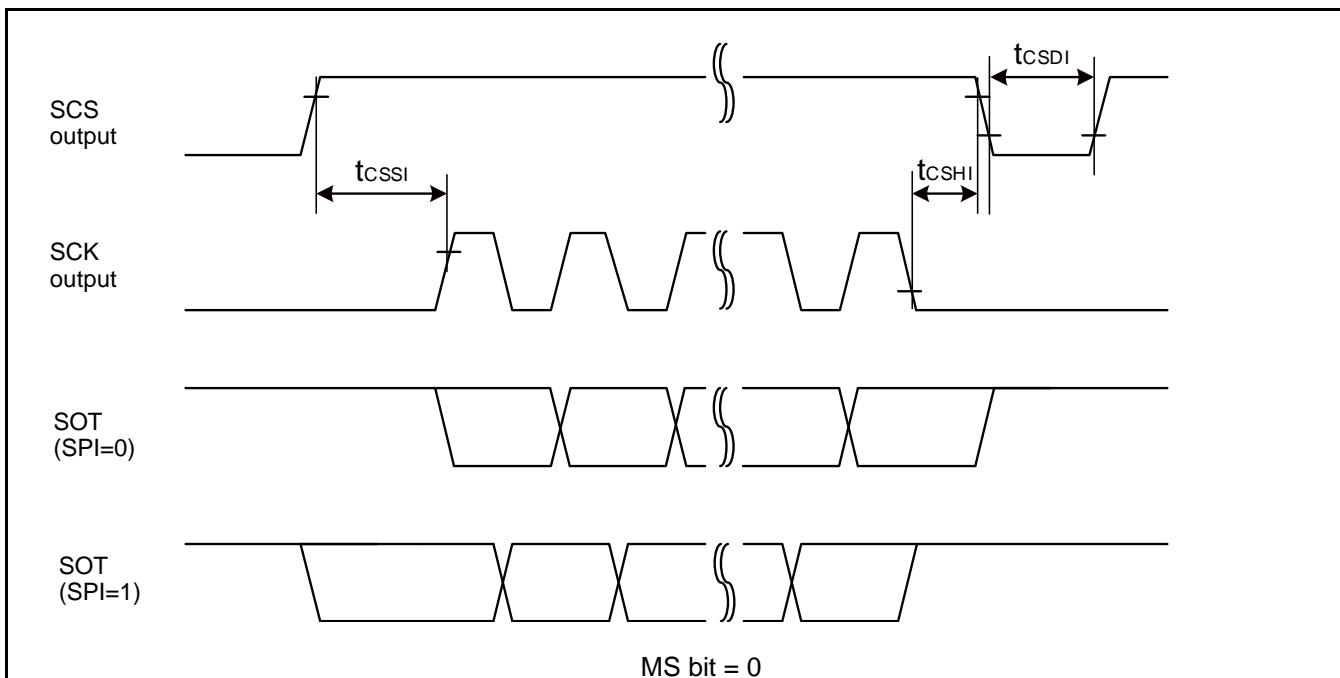
Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	
Baud rate	-	-		-	8	-	8	Mbps
Serial clock cycle time	t _{SCYC}	SCKx		4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↓→SOT delay time	t _{SLOVI}	SCKx, SOTx	Internal shift clock operation	- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t _{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t _{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx		2t _{CYCP} - 10	-	2t _{CYCP} - 10	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx	External shift clock operation	t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↓→SOT delay time	t _{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t _{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t _{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.







12.11 Standby Recovery Time

12.11.1 Recovery Cause: Interrupt/WKUP

The time from the interrupt occurring to the time of program operation start is shown.

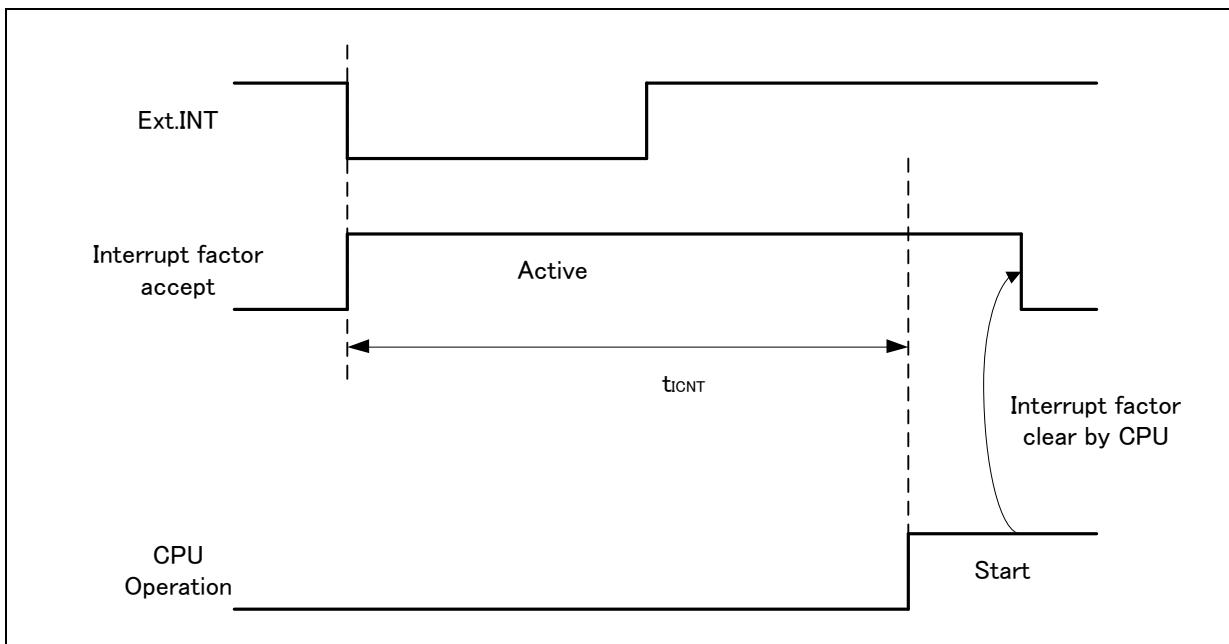
Recovery Count Time

($V_{cc} = 2.7V$ to $5.5V$, $V_{ss} = 0V$)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	tICNT	HCLKx1		μs	
High-speed CR Timer mode		40	80	μs	
Main Timer mode		450	900	μs	
PLL Timer mode		896	1136	μs	
Low-speed CR Timer mode		316	581	μs	
Sub Timer mode		270	540	μs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		365	667	μs	without RAM retention
RTC mode Stop mode (Low-speed CR/sub Run mode return)		365	667	μs	with RAM retention
Deep Standby RTC mode with RAM retention					
Deep Standby Stop mode with RAM retention					

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.