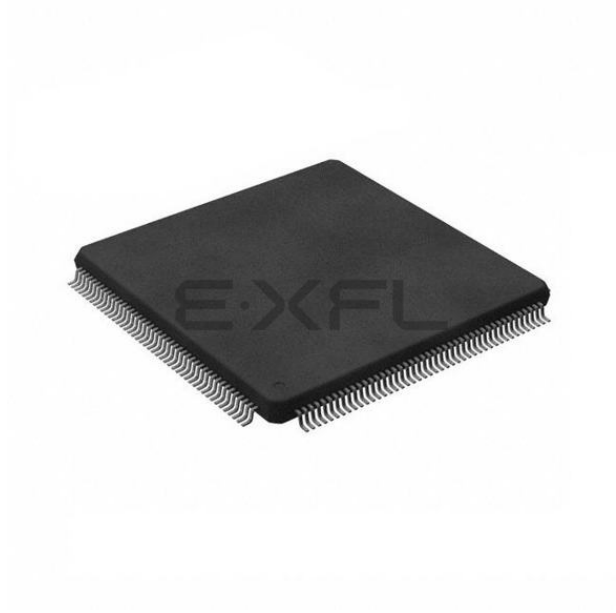

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2cc9j0agv2000a

1. Product Lineup

Memory Size

Product Name		S6E2CC8H/J/L	S6E2CC9H/J/L	S6E2CCAH/J/L
On-chip flash memory		1024 Kbytes	1536 Kbytes	2048 Kbytes
On-chip	SRAM	128 Kbytes	192 Kbytes	256 Kbytes
	SRAM0	64 Kbytes	128 Kbytes	192 Kbytes
	SRAM1	32 Kbytes	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes	32 Kbytes

Function

Product Name			S6E2CC8H0A S6E2CC9H0A S6E2CCAH0A S6E2CC8HHA S6E2CC9HHA S6E2CCAHHA	S6E2CC8J0A S6E2CC9J0A S6E2CCAJ0A S6E2CC8JHA S6E2CC9JHA S6E2CCAJHA	S6E2CC8L0A S6E2CC9L0A S6E2CCAL0A S6E2CC8LHA S6E2CC9LHA S6E2CCALHA
Pin count			144	176/192	216
CPU			Cortex-M4F, MPU, NVIC 128 ch		
	Freq.		200 MHz		
Power supply voltage range			2.7 V to 5.5 V		
USB2.0 (device/host)			2 ch		
Ethernet-MAC			1ch.(Max) MII: 1 ch /RMII: 1 ch (Max)		
CAN			2 ch (Max)		
CAN-FD (non-ISO CAN FD)			1 ch		
DMAC			8ch		
DSTC			256 ch		
External bus interface			Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash NAND flash	Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash , NAND flash SDRAM	Addr: 25-bit (Max), Data: 8-/16-/32-bit CS: 9 (Max), SRAM, NOR flash , NAND flash, SDRAM
Multi-function serial interface (UART/CSIO/LIN/I^{2}C)			16ch (Max) ch 0 to ch 7 : FIFO, ch 8 to ch 15 : No FIFO		
Base timer (PWC/Reload timer/PWM/PPG)			16 ch (Max)		
MF timer	A/D activation compare	6 ch	3 units (Max)		
	Input capture	4 ch			
	Free-run timer	3 ch			
	Output compare	6 ch			
	Waveform generator	3 ch			
	PPG	3 ch			
SD card interface			1 unit		
I^{2}S			-	1 unit	
Product Name			S6E2CC8H0A S6E2CC9H0A S6E2CCAH0A S6E2CC8HHA S6E2CC9HHA S6E2CCAHHA	S6E2CC8J0A S6E2CC9J0A S6E2CCAJ0A S6E2CC8JHA S6E2CC9JHA S6E2CCAJHA	S6E2CC8L0A S6E2CC9L0A S6E2CCAL0A S6E2CC8LHA S6E2CC9LHA S6E2CCALHA
High-speed quad SPI			-	1 unit	
QPRC			4 ch (Max)		
Dual timer			1 unit		
Real-time clock			1 unit		
Watch counter			1 unit		
CRC accelerator			Yes (fixed, programmable)		
Watchdog timer			1 ch (SW) + 1 ch (HW)		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
8	8	8	D3	PA6 SOT1_0 (SDA1_0)) DTTI2X_0 MADATA06_0	E	I
9	9	9	D4	PA7 SCK1_0 (SCL1_0) IC20_0 MADATA07_0	E	I
10	10	-	E2	P50 SCS72_0 RTO00_1 (PPG00_1) TIOA8_2 MADATA16_0	E	I
11	11	-	E3	P51 SCS73_0 RTO01_1 (PPG00_1) TIOB8_2 MADATA17_0	E	I
12	12	-	E4	P52 RTO02_1 (PPG02_1) TIOA9_2 MADATA18_0	E	I
13	-	-	-	P53 RTO03_1 (PPG02_1) TIOB9_2 MADATA19_0	E	I
14	13	10	E5	PA8 SIN7_0 IC21_0 INT02_0 WKUP1 MADATA08_0	I	Q
15	14	11	F1	PA9 SOT7_0 (SDA7_0) IC22_0 MADATA09_0	N	I
16	15	12	F2	PAA SCK7_0 (SCL7_0) IC23_0 MADATA10_0	N	I
17	16	13	F3	PAB SCS70_0 RX0_0 FRCK2_0 INT03_0 MADATA11_0	E	K

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 0	TIOA0_0	Base Timer ch 0 TIOA pin	56	46	38	N2
	TIOA0_1		45	35	30	J2
	TIOA0_2		114	94	78	L11
	TIOB0_0	Base Timer ch 0 TIOB pin	82	67	57	L8
	TIOB0_1		21	-	-	-
	TIOB0_2		115	95	79	K13
Base Timer 1	TIOA1_0	Base Timer ch 1 TIOA pin	57	47	39	N3
	TIOA1_1		46	36	31	K1
	TIOA1_2		116	96	80	K12
	TIOB1_0	Base Timer ch 1 TIOB pin	83	68	58	K8
	TIOB1_1		22	-	-	-
	TIOB1_2		123	99	83	J13
Base Timer 2	TIOA2_0	Base Timer ch 2 TIOA pin	58	48	40	M3
	TIOA2_1		47	37	32	K2
	TIOA2_2		124	100	84	J12
	TIOB2_0	Base Timer ch 2 TIOB pin	84	69	59	J8
	TIOB2_1		26	-	-	-
	TIOB2_2		125	101	85	J11
Base Timer 3	TIOA3_0	Base Timer ch 3 TIOA pin	59	49	41	L4
	TIOA3_1		48	38	33	K3
	TIOA3_2		130	106	86	H9
	TIOB3_0	Base Timer ch 3 TIOB pin	91	76	60	K9
	TIOB3_1		27	-	-	-
	TIOB3_2		131	107	87	H12
Base Timer 4	TIOA4_0	Base Timer ch 4 TIOA pin	60	50	42	M4
	TIOA4_1		49	39	34	K4
	TIOA4_2		132	108	88	H14
	TIOB4_0	Base Timer ch 4 TIOB pin	92	77	61	P10
	TIOB4_1		28	-	-	-
	TIOB4_2		133	109	89	G14
Base Timer 5	TIOA5_0	Base Timer ch 5 TIOA pin	61	51	43	N4
	TIOA5_1		50	40	35	L1
	TIOA5_2		134	110	90	H13
	TIOB5_0	Base Timer ch 5 TIOB pin	93	78	62	N10
	TIOB5_1		29	-	-	-
	TIOB5_2		135	111	91	H11
Base Timer 6	TIOA6_0	Base Timer ch 6 TIOA pin	179	147	117	D9
	TIOA6_1		85	70	-	N8
	TIOA6_2		200	-	-	-
	TIOB6_0	Base Timer ch 6 TIOB pin	178	146	116	B8
	TIOB6_1		86	71	-	M8
	TIOB6_2		199	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7	7	D1
	TIOA13_1		154	124	100	E12
	TIOA13_2		34	24	-	G6
	TIOB13_0	Base Timer ch 13 TIOB pin	31	22	19	G4
	TIOB13_1		155	125	101	E13
	TIOB13_2		35	25	-	H4
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	183	151	121	D8
	TIOA14_1		89	74	-	M9
	TIOA14_2		204	-	-	-
	TIOB14_0	Base Timer ch 14 TIOB pin	182	150	120	C8
	TIOB14_1		90	75	-	L9
	TIOB14_2		203	-	-	-
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	187	155	125	B7
	TIOA15_1		78	63	-	K5
	TIOA15_2		206	-	-	-
	TIOB15_0	Base timer ch 15 TIOB pin	186	154	124	F8
	TIOB15_1		79	64	-	K6
	TIOB15_2		205	-	-	-
CAN 0	TX0_0	CAN interface ch 0 TX output pin	18	17	14	F4
	TX0_1		35	25	-	H4
	TX0_2		176	-	-	-
	RX0_0	CAN interface ch 0 RX output pin	17	16	13	F3
	RX0_1		34	24	-	G6
	RX0_2		175	-	-	-
CAN 1	TX1_0	CAN interface ch 1 TX output pin	152	122	98	E10
	TX1_1		118	98	82	K11
	TX1_2		148	-	-	-
	RX1_0	CAN interface ch 1 RX output pin	153	123	99	E11
	RX1_1		117	97	81	K14
	RX1_2		149	-	-	-
CAN 2 (CAN-FD)	TX2_0	CAN-FD interface ch 2 TX output pin	71	56	48	M5
	TX2_1		79	64	-	K6
	TX2_2		69	-	-	-
	RX2_0	CAN-FD interface ch 2 RX input pin	70	55	47	L5
	RX2_1		78	63	-	K5
	RX2_2		68	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PA0	General-purpose I/O port A	2	2	2	B2
	PA1		3	3	3	C2
	PA2		4	4	4	C3
	PA3		5	5	5	D5
	PA4		6	6	6	D2
	PA5		7	7	7	D1
	PA6		8	8	8	D3
	PA7		9	9	9	D4
	PA8		14	13	10	E5
	PA9		15	14	11	F1
	PAA		16	15	12	F2
	PAB		17	16	13	F3
	PAC		18	17	14	F4
	PAD		23	18	15	F5
	PAE		24	19	16	F6
	PAF		25	20	17	G2
	PB0	General-purpose I/O port B	126	102	-	J10
	PB1		127	103	-	J9
	PB2		128	104	-	H10
	PB3		129	105	-	J14
	PB4		138	112	-	G13
	PB5		139	113	-	F14
	PB6		140	114	-	G12
	PB7		141	115	-	G11
	PB8		119	-	-	-
	PB9		120	-	-	-
	PBA		121	-	-	-
	PBB		122	-	-	-
	PBC		148	-	-	-
	PBD		149	-	-	-
	PBE		150	-	-	-
	PBF		151	-	-	-

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

7. Handling Devices

Power-Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. All of these pins should be connected externally to the power supply or ground lines, however, in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Be sure to connect the current-supply source with the power pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

A malfunction may occur when the power-supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane, as this is expected to produce stable operation.

Evaluate the oscillation introduced by the use of the crystal oscillator by your mount board.

Sub Crystal Oscillator

The sub-oscillator circuit for devices in this family is low gain to keep current consumption low. To stabilize the oscillation, Cypress recommends a crystal oscillator that meets the following conditions:

- Surface mount type
  Size: More than 3.2 mm × 1.5 mm
  Load capacitance: approximately 6 pF to 7 pF
- Lead type
  Load capacitance: approximately 6 pF to 7 pF

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	200 MHz	128	236	mA	*3 When all peripheral clocks are on
					192 MHz	123	230	mA	
					180 MHz	116	221	mA	
				*6	160 MHz	102	205	mA	
					144 MHz	93	193	mA	
					120 MHz	79	175	mA	
					100 MHz	67	161	mA	
					80 MHz	54	145	mA	
					60 MHz	42	130	mA	
					40 MHz	30	115	mA	
					20 MHz	17	99	mA	
					8 MHz	9.2	90.0	mA	
					4 MHz	6.7	86.9	mA	
				*5	200 MHz	74	170	mA	*3 When all peripheral clocks are off
					192 MHz	71	167	mA	
					180 MHz	67	162	mA	
				*6	160 MHz	59	152	mA	
					144 MHz	53	145	mA	
					120 MHz	45	135	mA	
					100 MHz	39	127	mA	
					80 MHz	32	118	mA	
					60 MHz	25	110	mA	
					40 MHz	18	101	mA	
					20 MHz	11	92	mA	
					8 MHz	6.5	86.8	mA	
					4 MHz	5.1	85.0	mA	

*1: T_A = +25 °C, V_{CC} = 3.3 V

*2: T_J = +125 °C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 0)

*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

*7: With data access to a MainFlash memory.

*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-10 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/Erase

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
MainFlash memory write/erase current	$I_{CCFLASH}$		At write/erase	-	13.4	15.9	mA	*1

*1: When programming or erase in flash memory, Flash Memory Write/Erase current ($I_{CCFLASH}$) is added to the Power supply current (I_{CC}).

Peripheral Current Dissipation

Clock System	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			50	100	200		
HCLK	GPIO	All ports	0.39	0.81	1.56	mA	
	DMAC	-	0.99	1.97	3.82		
	DSTC	-	0.73	1.49	2.86		
	External bus I/F	-	0.25	0.48	0.97		
	SD card I/F	-	0.74	1.47	2.90		
	CAN	1 ch	0.06	0.08	0.16		
	CAN-FD	1 ch	0.77	1.50	2.95		
	USB	1 ch	0.48	0.95	1.89		
	Ethernet-MAC	-	1.85	3.63	7.20		
	I^2S	-	0.51	1.02	1.99		
	High-speed Quad SPI	-	0.48	0.97	1.49		
	Programmable CRC	-	0.05	0.10	0.22		
PCLK1	Base timer	4 ch	0.21	0.42	0.83	mA	
	Multi-functional timer/PPG	1 unit/4 ch	0.83	1.65	3.25		
	Quadrature position/revolution counter	1 unit	0.07	0.13	0.27		
	A/D converter	1 unit	0.31	0.60	1.17		
PCLK2	Multi-function serial	1 ch	0.41	0.81	-	mA	

Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Minimum pulse width	t_{OEW}	MOEX	-	MCLK×n-3	-	ns	
MCSX ↓ →Address output delay time	t_{CSL-AV}	MCSX[7: 0], MAD[24: 0]	-	-9	+9	ns	
MOEX ↑ →Address hold time	t_{OEH-AX}	MOEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7: 0]	-	MCLK×m-9	MCLK×m+9	ns	
MOEX ↑ → MCSX ↑ time	$t_{OEH-CSH}$		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[3: 0]	-	MCLK×m-9	MCLK×m+9	ns	
Data set up→MOEX ↑ time	t_{DS-OE}	MOEX, MADATA[31: 0]	-	20	-	ns	
MOEX ↑ → Data hold time	t_{DH-OE}	MOEX, MADATA[31: 0]	-	0	-	ns	
MWEX Minimum pulse width	t_{WEW}	MWEX	-	MCLK×n-3	-	ns	
MWEX ↑ →Address output delay time	t_{WEH-AX}	MWEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH-CSH}$		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[3: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MCSX ↓ → Data output time	t_{CSL-DX}	MCSX, MADATA[31: 0]	-	MCLK-9	MCLK+9	ns	
MWEX ↑ → Data hold time	t_{WEH-DX}	MWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

Note:

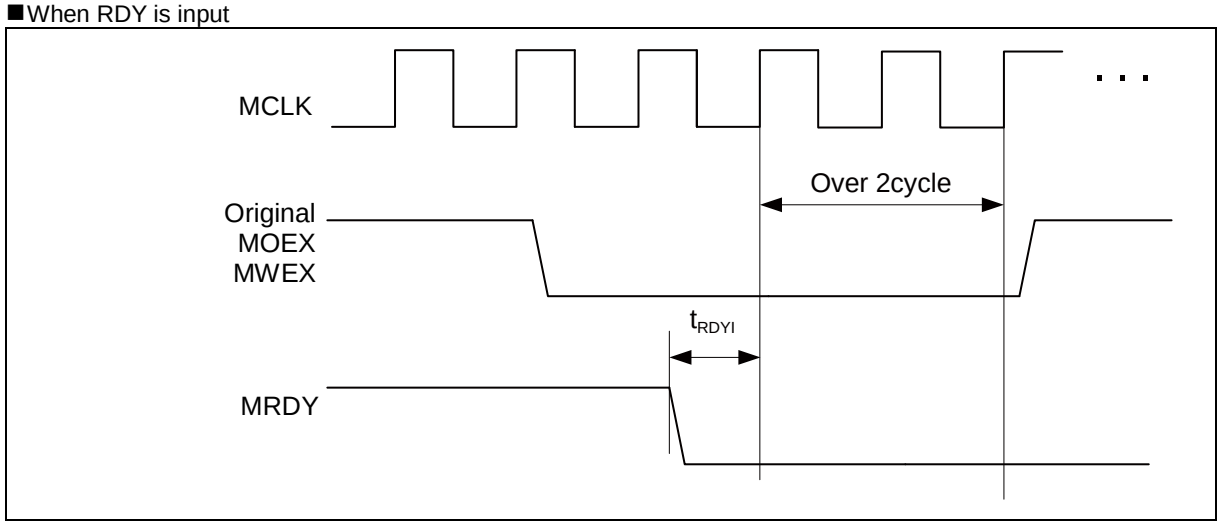
- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*

External Ready Input Timing

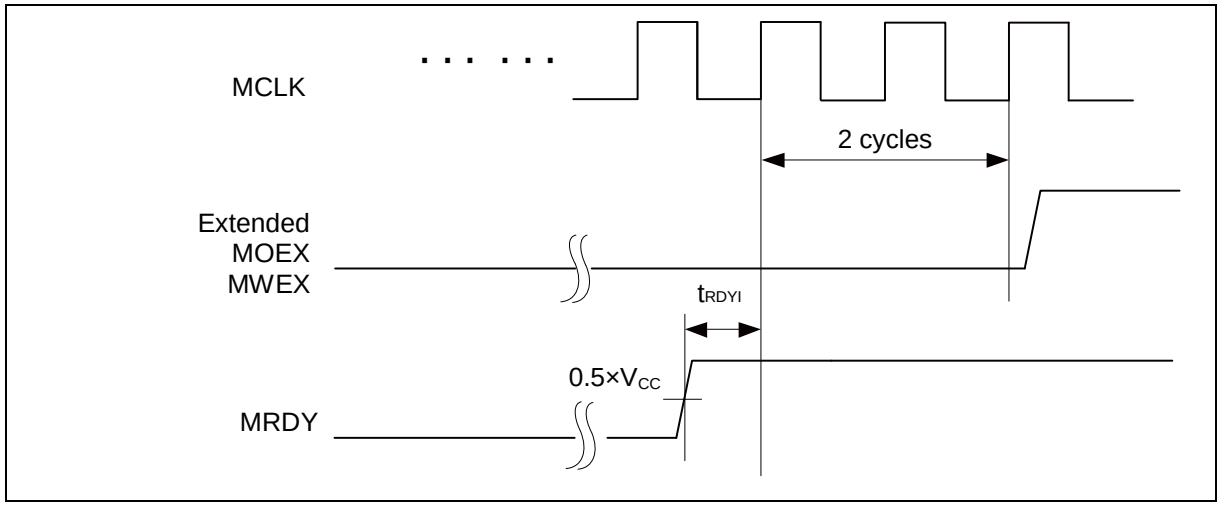
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

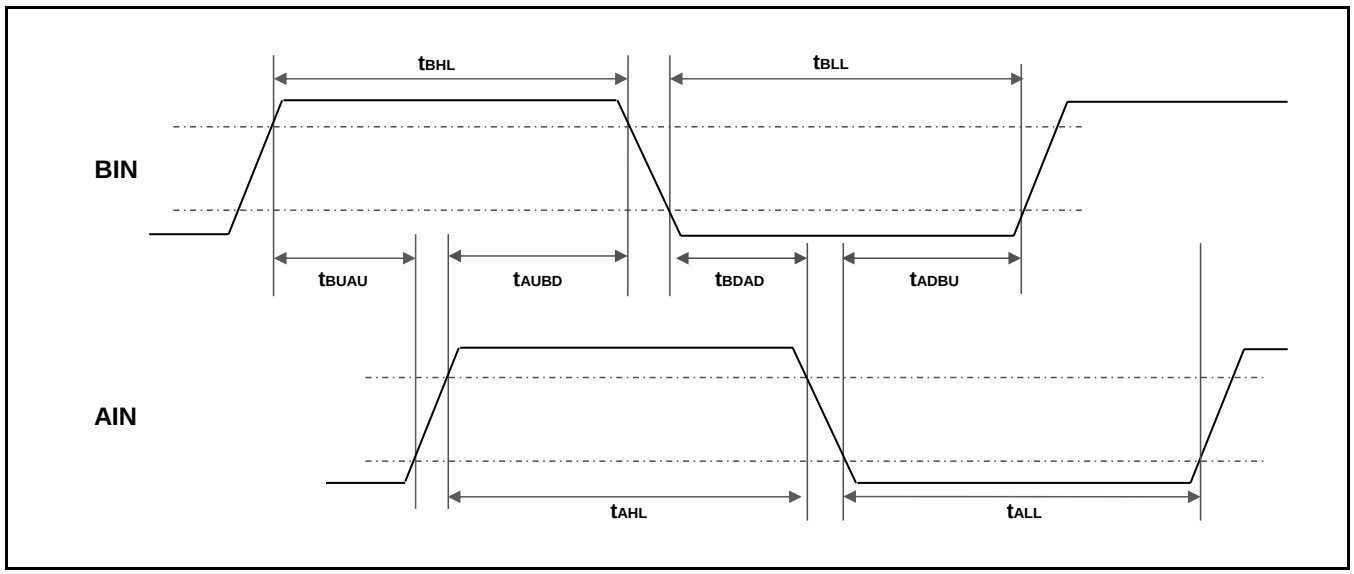
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■When RDY is input



■When RDY is released

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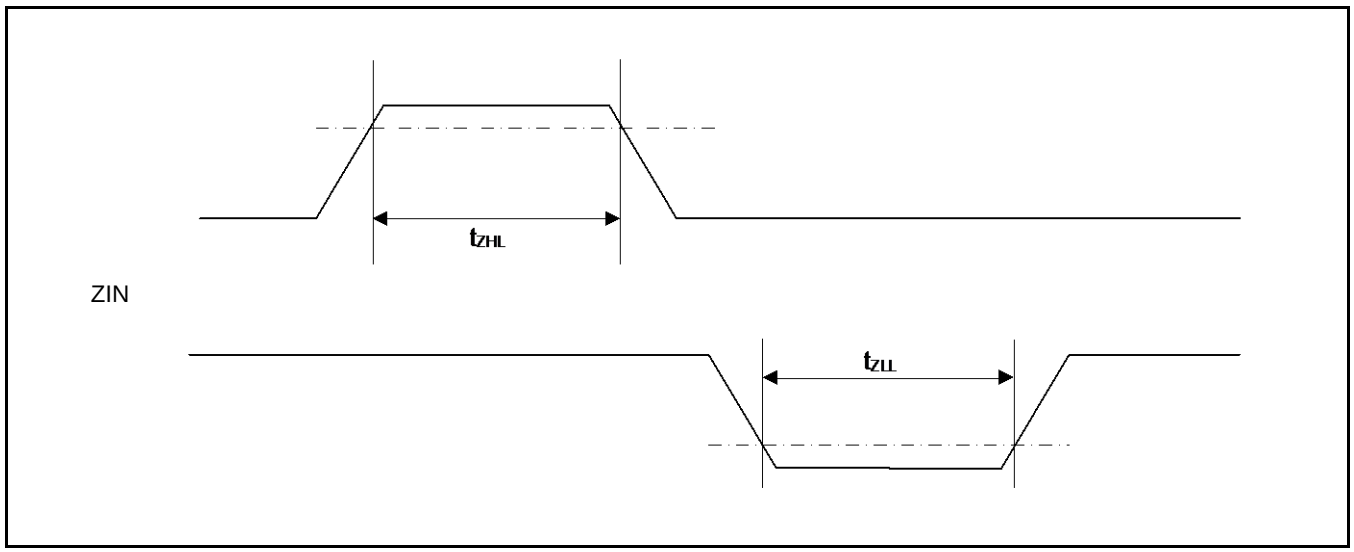
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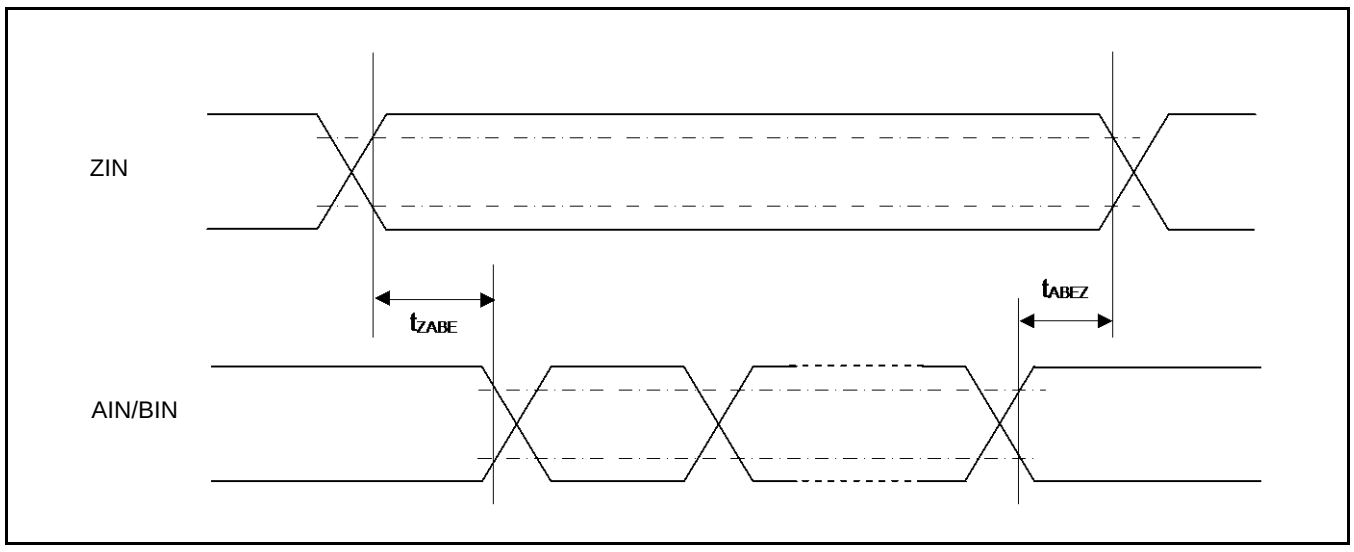

ZIN
AIN/BIN
tZABE
tABEZ

Fast mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
SCL clock frequency	t_{SUSTA}		0.26	-	µs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between "Stop condition" and "START condition"	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

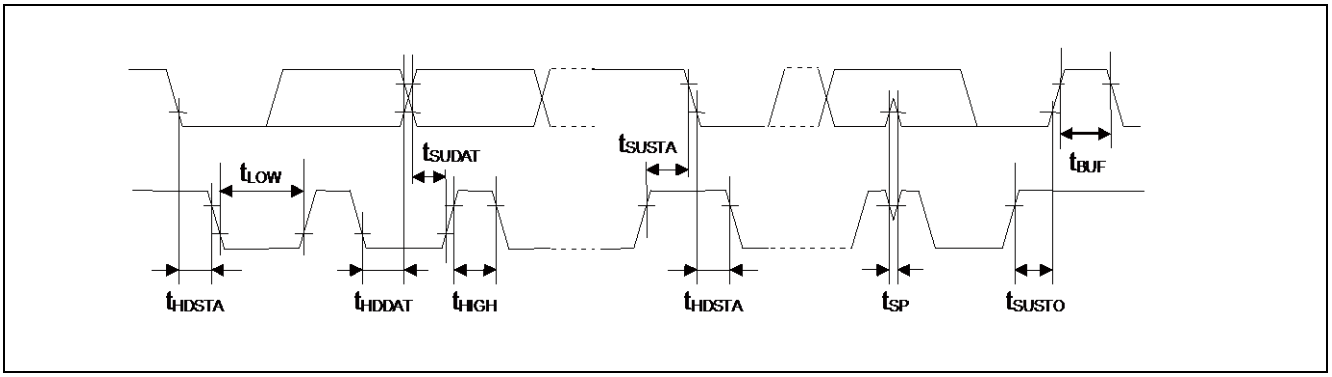
*2: The maximum t_{HDDT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

*3: The Fast mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns."

*4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I^2C is connected, see 8.Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

*6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register. See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.



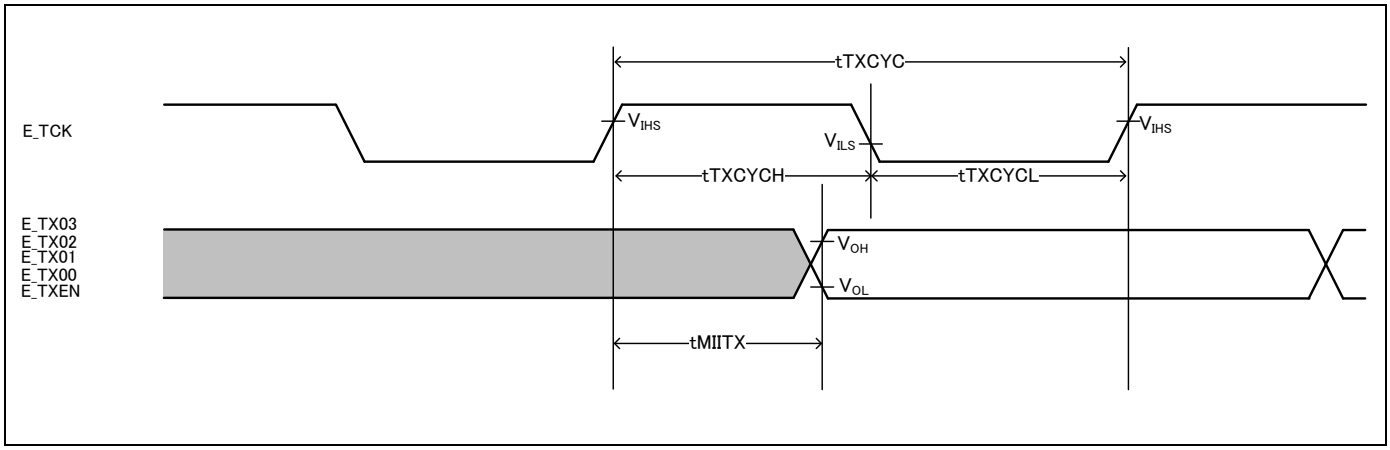
MII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V*1, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Transmission clock Cycle time*2	t_{TXCYC}	E_TCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Transmission clock High-pulse-width duty cycle	t_{TXCYCH}	E_TCK	t_{TXCYCH}/t_{TXCYC}	35	65	%
Transmission clock Low-pulse-width duty cycle	t_{TXCYCL}	E_TCK	t_{TXCYCL}/t_{TXCYC}	35	65	%
TXCK ↑ → Transmitted data delay time	t_{MIITX}	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	24	ns

*1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

*2: The transmission clock is fixed to 25 MHz or 2.5 MHz in the MII specifications. The clock accuracy should meet the PHY-device specifications.

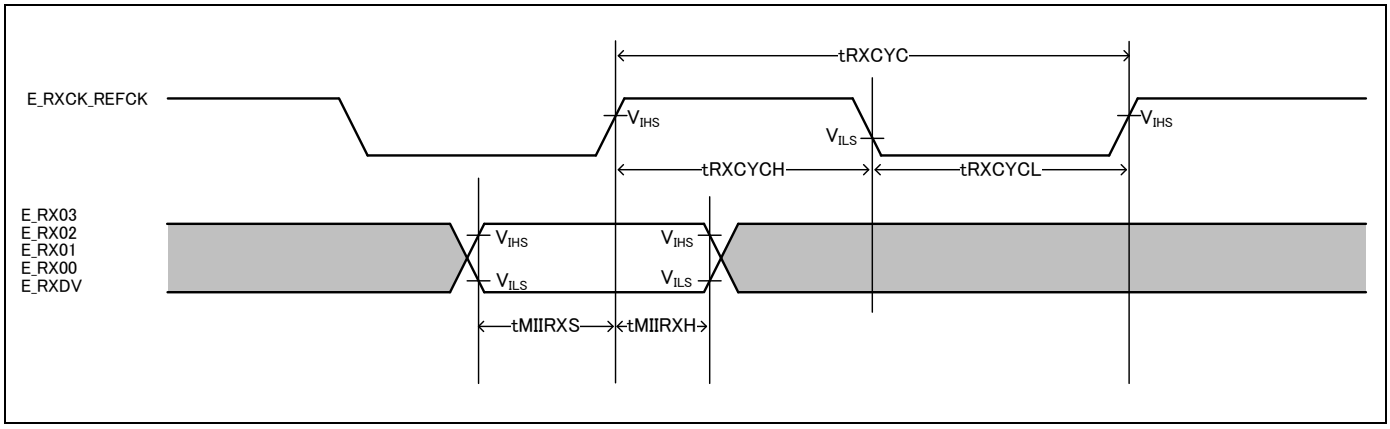


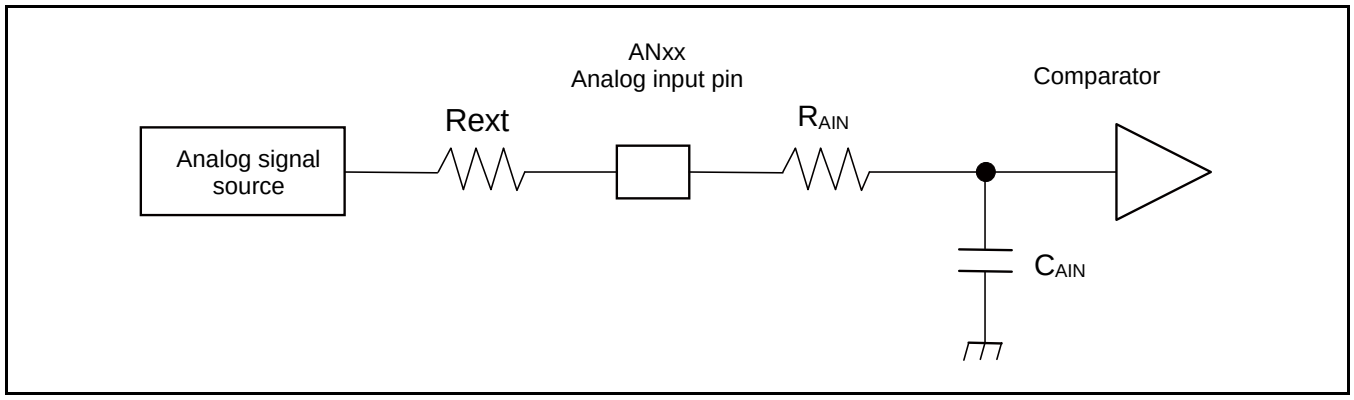
MII Receiving (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Receiving clock cycle time*	t_{RXCYC}	E_RXCK_REFCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Receiving clock High pulse width duty cycle	t_{RXCYCH}	E_RXCK_REFCK	t_{RXCYCH}/t_{RXCYC}	35	65	%
Receiving clock Low pulse width duty cycle	t_{RXCYCL}	E_RXCK_REFCK	t_{RXCYCL}/t_{RXCYC}	35	65	%
Received data → REFCK ↑Setup time	t_{MIIRXS}	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	5	-	ns
REFCK ↑ → Received data Hold time	t_{MIIRXH}	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns

*: The reference clock is fixed to 50 MHz in the RMII specifications.
The clock accuracy should meet the PHY-device specifications.





(Equation 1) $t_S \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.2 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V

Input resistance of A/D = 1.8 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 12.05 pF at 2.7 V ≤ AV_{CC} ≤ 5.5 V

R_{ext}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

12.11 Standby Recovery Time

12.11.1 Recovery Cause: Interrupt/WKUP

The time from the interrupt occurring to the time of program operation start is shown.

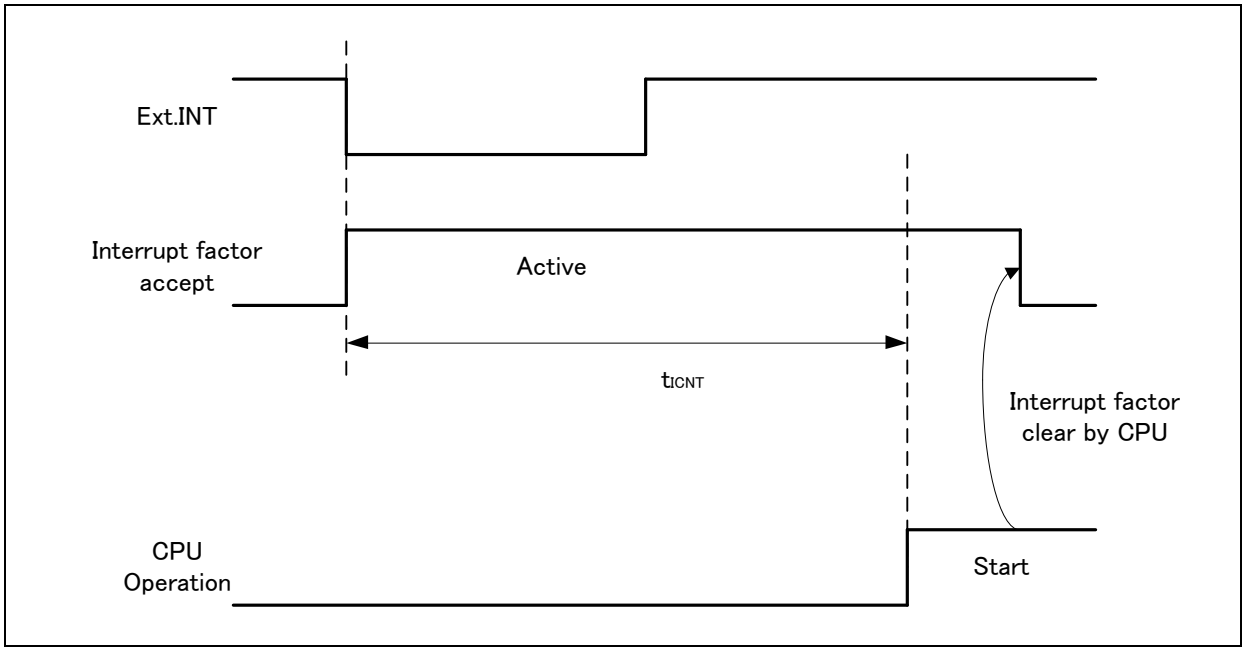
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		450	900	µs	
Sub Timer mode		896	1136	µs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	µs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	µs	
Deep Standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		365	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

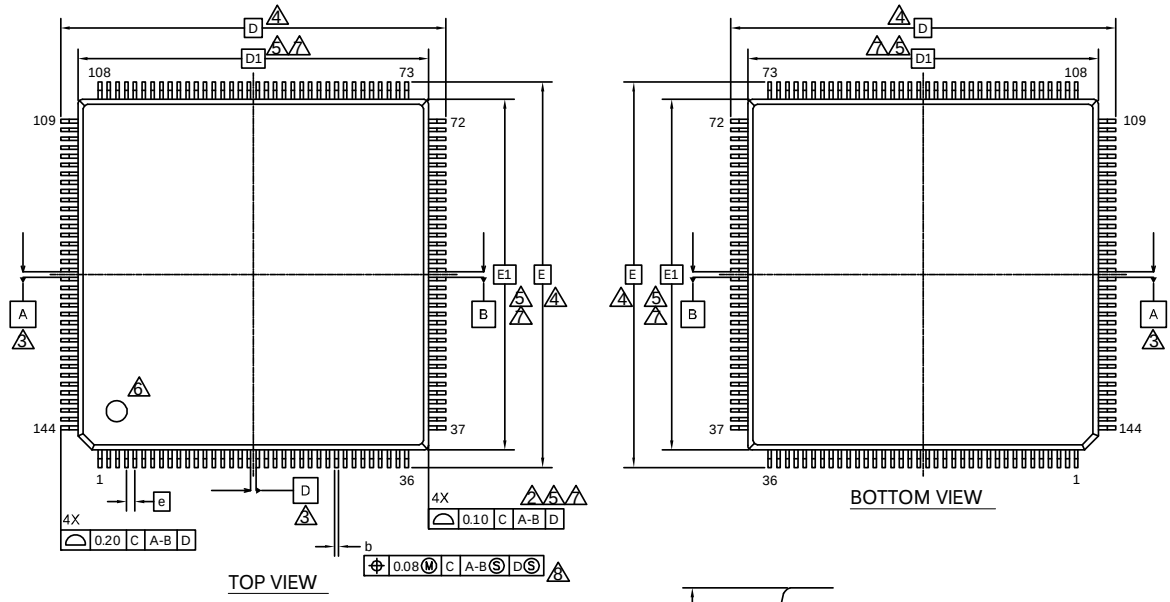
Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS 144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

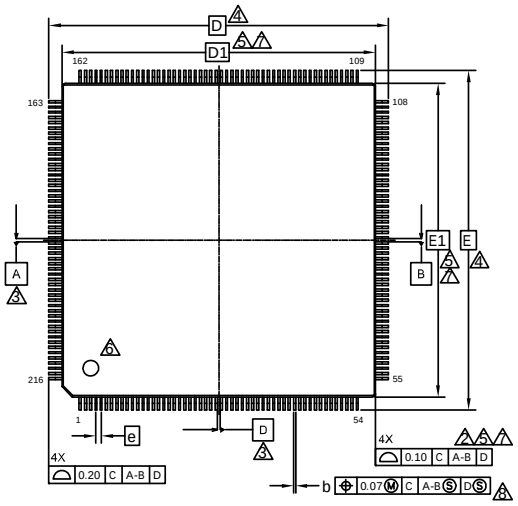
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

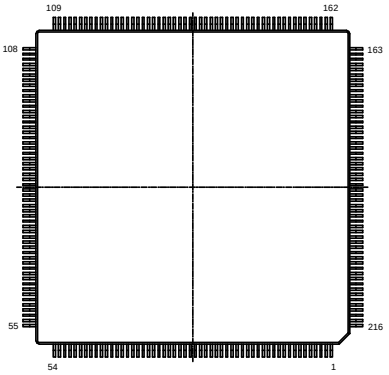
002-13015 **

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 Rev**

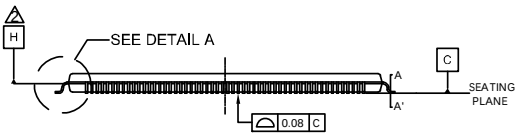
Package Type	Package Code
LQFP 216	LQQ 216



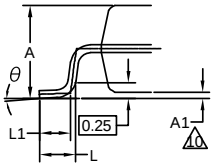
TOP VIEW



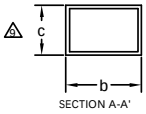
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.13	0.18	0.23
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.40 BSC		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15153 **

PACKAGE OUTLINE, 216 LEAD LQFP
24.0X24.0X1.7 MM LQQ216 REV**

15. Major Changes

Spansion Publication Number: DS709-00009

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 0.2		
1, 3	Title	Added the following products. S6E2CC8HHA/S6E2CC9HHA/S6E2CCAHHA/ S6E2CC8JHA/S6E2CC9JHA/S6E2CCAJHA/ S6E2CC8LHA/S6E2CC9LHA/S6E2CCALHA
14	2.Feature	Added “Crypto Assist Function”
16, 17	3.Product Lineup	Added “Crypto Assist Function”
18	4.Packages	Added the following products. S6E2CC8HHA/S6E2CC9HHA/S6E2CCAHHA/ S6E2CC8JHA/S6E2CC9JHA/S6E2CCAJHA/ S6E2CC8LHA/S6E2CC9LHA/S6E2CCALHA
212	15.ORDERING INFORMATION	Added the following part numbers. S6E2CC8HHAGV20000/S6E2CC9HHAGV20000/S6E2CCAHHAGV20000/ S6E2CC8JHAGV20000/S6E2CC9JHAGV20000/S6E2CCAJHAGV20000/ S6E2CC8JHAGB10000/S6E2CC9JHAGB10000/S6E2CCAJHAGB10000/ S6E2CC8LHAGL20000/S6E2CC9LHAGL20000/S6E2CCALHAGL20000
Revision 0.3		
1, 3	Title	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
14	2.Features	Added Voice Function
15, 16	3.Product Lineup	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
17	4.Packages	Added the following products. S6E2CCAJGA /S6E2CC8JGA/S6E2CC8JFA/S6E2CCAJFA
211	15.Ordering Information	Added the following products. S6E2CCAJGAGV20000/ S6E2CC8JGAGB10000/ S6E2CC8JFAGB10000 S6E2CCAJGAGB10000/ S6E2CCAJFAGB10000
Revision 1.0		
7 15	2. Features 3. Product Lineup	Added that CAN-FD Interface supported non-CAN FD.
12 15 90 91	2. Features 3. Product Lineup 10. Block Diagram 12. Memory Map	Deleted HDM-CEC/Remote Control Receiver.
18-20	5. Pin Assignments	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Modified the pin name of I2S. (MI2S*_0→MI2S*0_0) Deleted the pin of IGTRG0_0.
22-24	6. Pin Descriptions	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Modified the pin name of I2S. (MI2S*_0→MI2S*0_0) Modified the pin number of PF7 in LQFP216.(91→90) Modified the pin number of X1. (73, 58, 50, P5→107, 87, 71, P13) Modified the pin number of X0A. (107, 87, 71, P13→73, 58, 50, P5)
75-82	7. I/O Circuit Type	Modified IOH/IOL of Type S.(IOH=-12mA→-10mA, IOL=12mA→10mA) Added the case of using I2C in Type E, F, G, L, N, S.
97-105	13. Pin Status In Each CPU State	Deleted X and Y in Pin Status Type.
106-107	14.1. Absolute Maximum Ratings	Added 10mA type.
108-112	14.2. Recommended Operating Conditions	Added AVRL in Analog reference voltage. Modified the mistake in Ethernet-MAC Pins. Modified the leakage current in Maximum leakage current at operating
113-122	14.3.1. Current Rating	Modified the maximum current of each category.