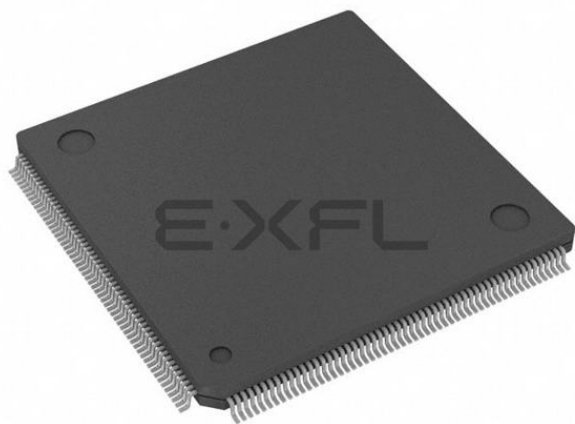




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I ² C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	190
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	216-LQFP
Supplier Device Package	216-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2cc9l0agl2000a

External interrupts		32 pins (Max)+ NMI × 1					
I/O ports		120 pins (Max)		152 pins (Max)		190 pins (Max)	
12-bit A/D converter		24 ch (3 units)		32 ch (3 units)			
12-bit D/A converter		2 units (Max)					
CSV (clock supervisor)		Yes					
LVD (low-voltage detector)		2 ch					
Built-in CR	High-speed	4 MHz					
	Low-speed	100 kHz					
Debug function		SWJ-DP/ETM/HTM					
Unique ID		Yes					
Crypto Assist Function		-	Yes ^{*1}	-	Yes ^{*1}	-	Yes ^{*1}

*1: Crypto Assist Function is built in following products.

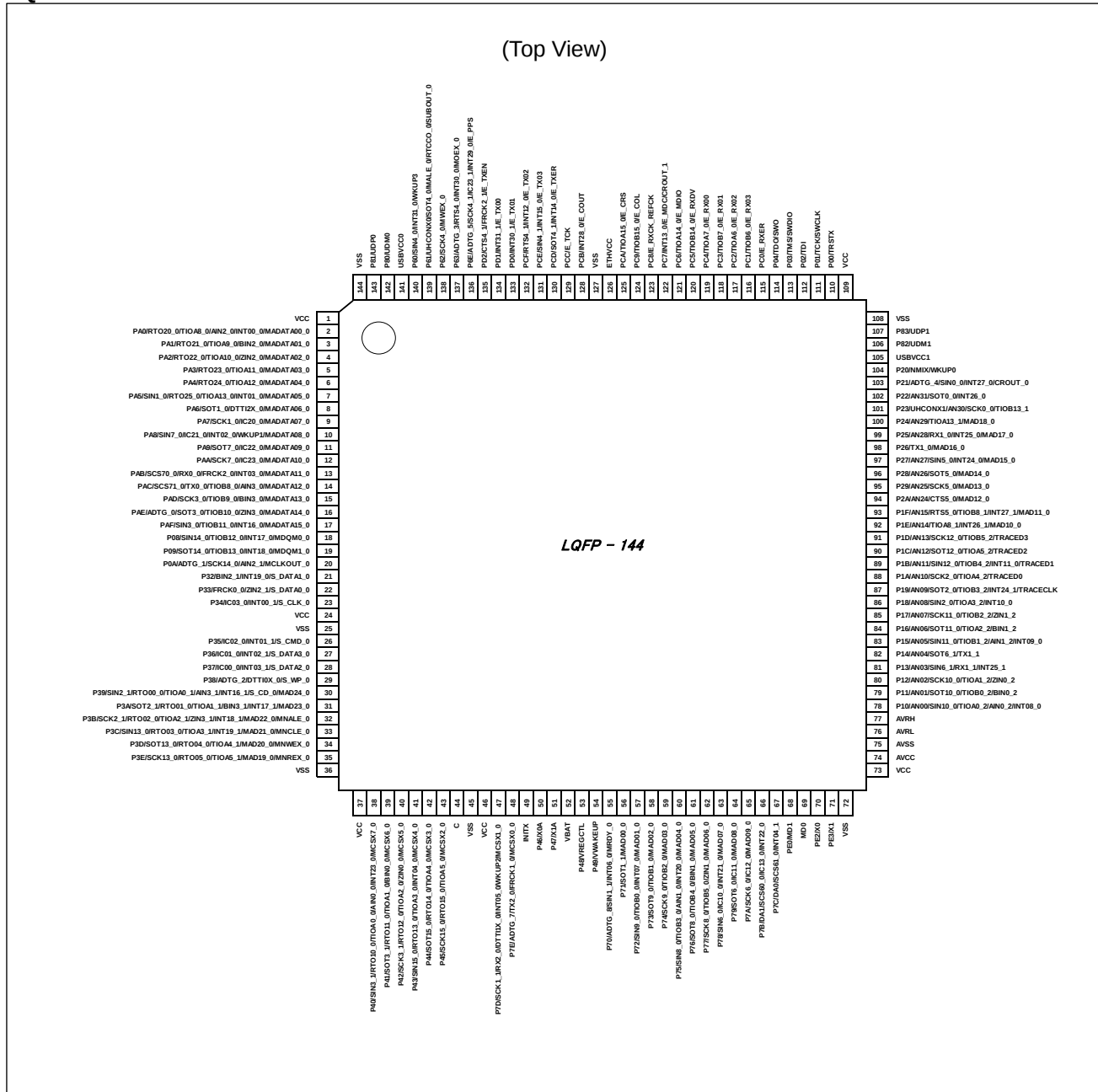
S6E2CC8HHA, S6E2CC9HHA, S6E2CCAHHA, S6E2CC8JHA, S6E2CC9JHA, S6E2CCAJHA,
S6E2CC8LHA, S6E2CC9LHA, S6E2CCALHA

Notes:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
- See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.

3. Pin Assignments

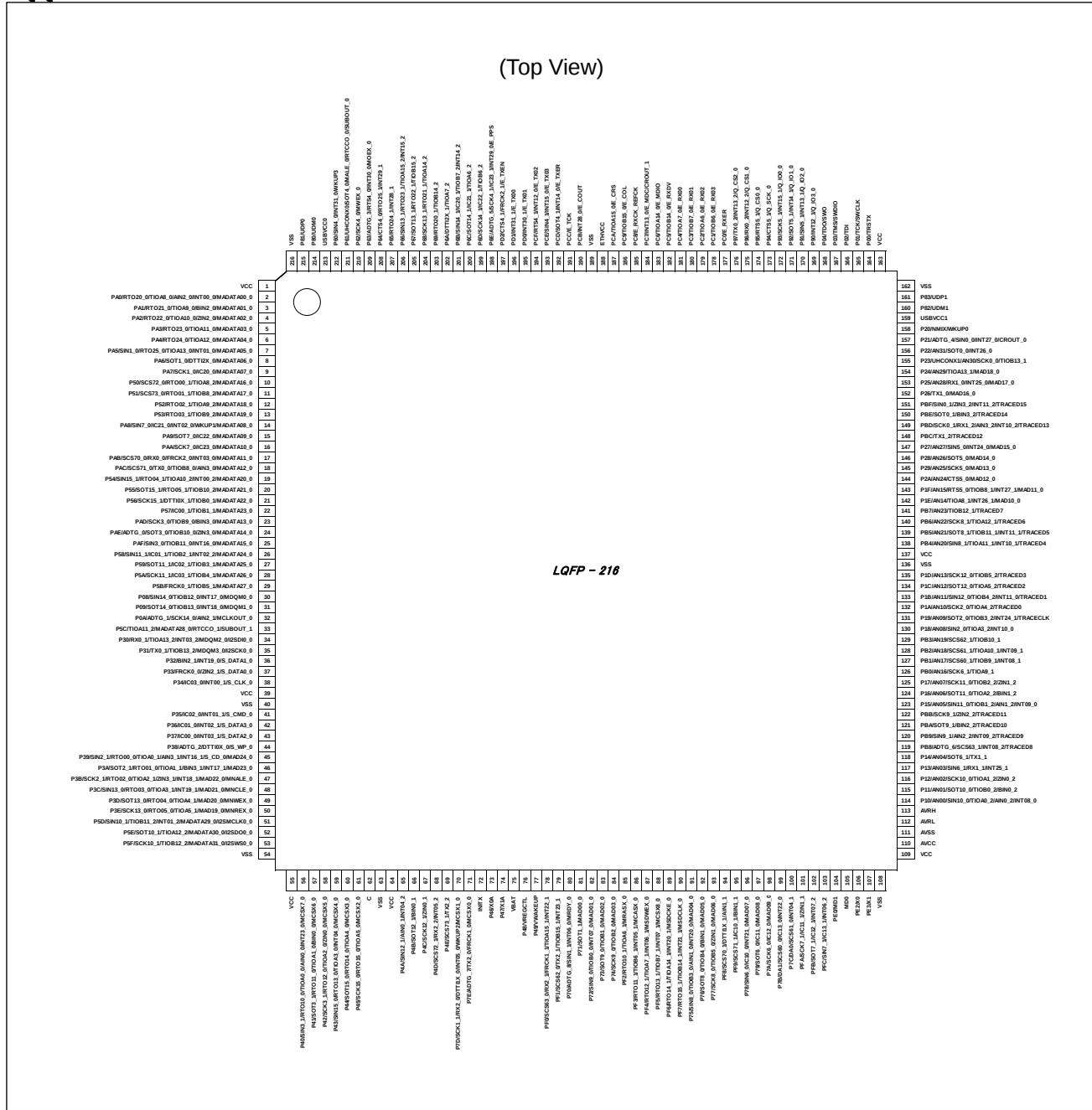
LQS144



Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LQ216



Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

4. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
1	1	1	C1	VCC	-	-
2	2	2	B2	PA0	G	K
				RTO20_0 (PPG20_0)		
				TIOA8_0		
				AIN2_0		
				INT00_0		
				MADATA00_0		
3	3	3	C2	PA1	G	I
				RTO21_0 (PPG20_0)		
				TIOA9_0		
				BIN2_0		
				MADATA01_0		
4	4	4	C3	PA2	G	I
				RTO22_0 (PPG22_0)		
				TIOA10_0		
				ZIN2_0		
				MADATA02_0		
5	5	5	D5	PA3	G	I
				RTO23_0 (PPG22_0)		
				TIOA11_0		
				MADATA03_0		
6	6	6	D2	PA4	G	I
				RTO24_0 (PPG24_0)		
				TIOA12_0		
				MADATA04_0		
7	7	7	D1	PA5	G	K
				SIN1_0		
				RTO25_0 (PPG24_0)		
				TIOA13_0		
				INT01_0		
				MADATA05_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
48	38	33	K3	P3C	G	K
				SIN13_0		
				RTO03_0 (PPG02_0)		
				TIOA3_1		
				INT19_1		
				MAD21_0		
				MNCLE_0		
49	39	34	K4	P3D	G	I
				SOT13_0 (SDA13_0)		
				RTO04_0 (PPG04_0)		
				TIOA4_1		
				MAD20_0		
				MNWEX_0		
50	40	35	L1	P3E	G	I
				SCK13_0 (SCL13_0)		
				RTO05_0 (PPG04_0)		
				TIOA5_1		
				MAD19_0		
				MNREX_0		
51	41	-	L2	P5D	E	K
				SIN10_1		
				TIOB11_2		
				INT01_2		
				MADATA29_0		
				I2SMCLK0_0		
52	42	-	L3	P5E	E	I
				SOT10_1 (SDA10_1)		
				TIOA12_2		
				MADATA30_0		
				I2SDO0_0		
53	43	-	M2	P5F	E	I
				SCK10_1 (SCL10_1)		
				TIOB12_2		
				MADATA31_0		
				I2SWS0_0		
54	44	36	M1	VSS	-	-
55	45	37	N1	VCC	-	-
56	46	38	N2	P40	G	K
				SIN3_1		
				RTO10_0 (PPG10_0)		
				TIOA0_0		
				AIN0_0		
				INT23_0		
				MCSX7_0		

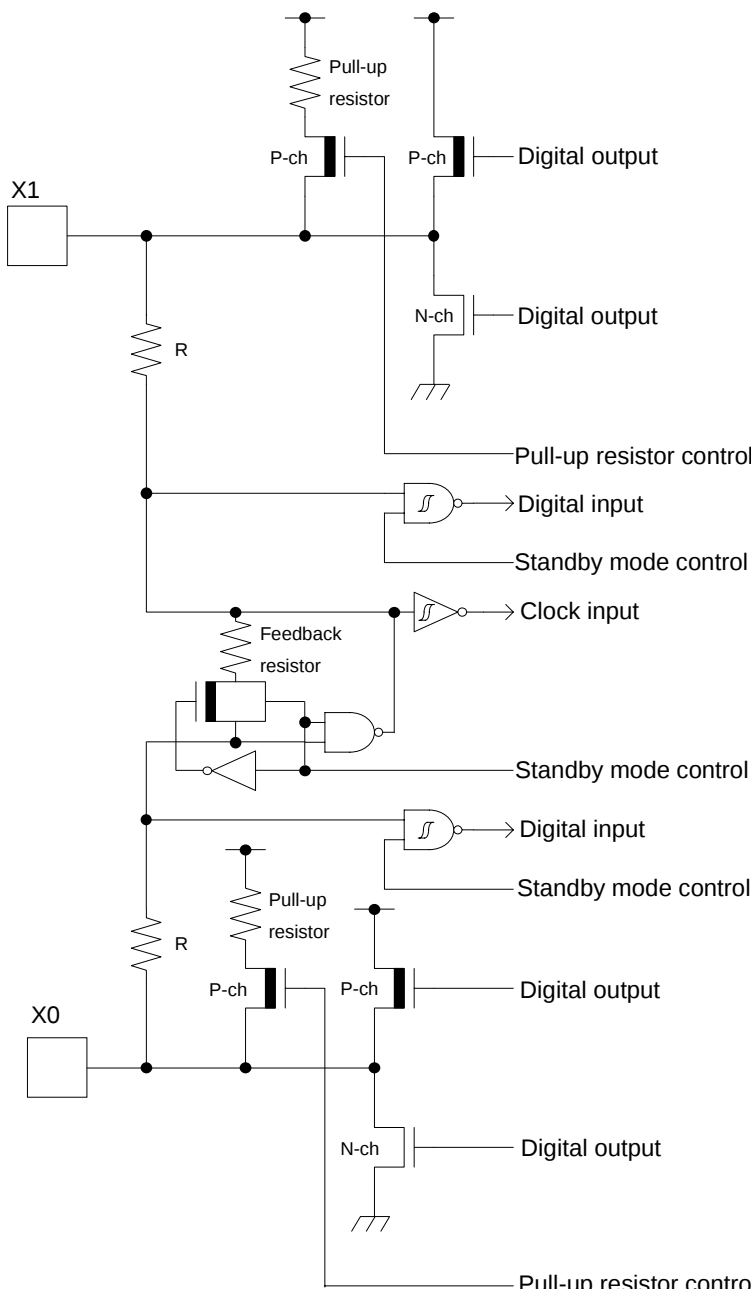
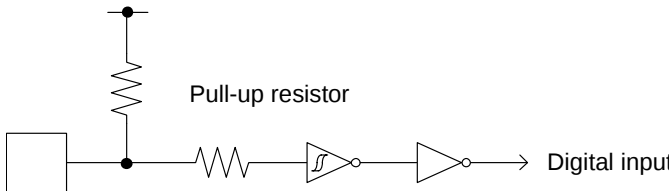
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	181	149	119	F9
	TIOA7_1		87	72	-	N9
	TIOA7_2		202	-	-	-
	TIOB7_0	Base Timer ch 7 TIOB pin	180	148	118	E9
	TIOB7_1		88	73	-	P9
	TIOB7_2		201	-	-	-
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2	2	B2
	TIOA8_1		142	116	92	G10
	TIOA8_2		10	10	-	E2
	TIOB8_0	Base Timer ch 8 TIOB pin	18	17	14	F4
	TIOB8_1		143	117	93	G9
	TIOB8_2		11	11	-	E3
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3	3	C2
	TIOA9_1		126	102	-	J10
	TIOA9_2		12	12	-	E4
	TIOB9_0	Base Timer ch 9 TIOB pin	23	18	15	F5
	TIOB9_1		127	103	-	J9
	TIOB9_2		13	-	-	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4	4	C3
	TIOA10_1		128	104	-	H10
	TIOA10_2		19	-	-	-
	TIOB10_0	Base Timer ch 10 TIOB pin	24	19	16	F6
	TIOB10_1		129	105	-	J14
	TIOB10_2		20	-	-	-
Base Timer 11	TIOA11_0	Base Timer ch 11 TIOA pin	5	5	5	D5
	TIOA11_1		138	112	-	G13
	TIOA11_2		33	-	-	-
	TIOB11_0	Base Timer ch 11 TIOB pin	25	20	17	G2
	TIOB11_1		139	113	-	F14
	TIOB11_2		51	41	-	L2
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6	6	D2
	TIOA12_1		140	114	-	G12
	TIOA12_2		52	42	-	L3
	TIOB12_0	Base Timer ch 12 TIOB pin	30	21	18	G3
	TIOB12_1		141	115	-	G11
	TIOB12_2		53	43	-	M2

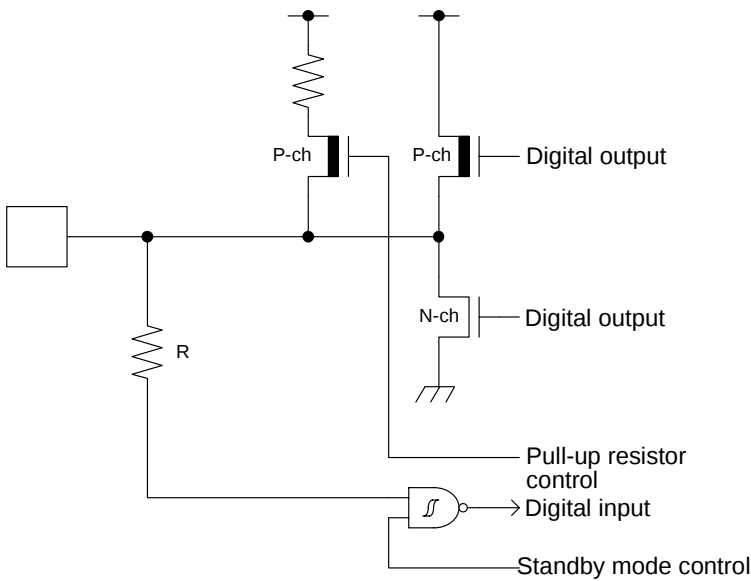
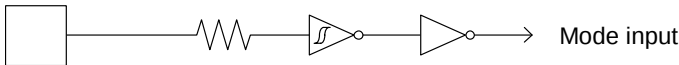
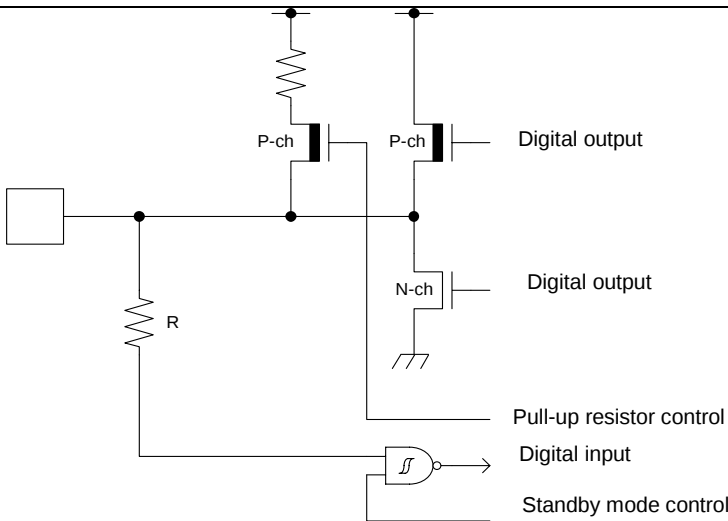
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin	146	120	96	F12
	SOT5_1 (SDA5_1)	This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I ² C (operation mode 4).	171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin	145	119	95	F11
	SCK5_1 (SCL5_1)	This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I ² C (operation mode 4).	172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin	97	80	64	K10
	SOT6_1 (SDA6_1)	This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I ² C (operation mode 4).	118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin	98	81	65	M10
	SCK6_1 (SCL6_1)	This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I ² C (operation mode 4).	126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 2	DTTI2X_0	Input signal controlling waveform generator outputs RTO20 to RTO25 of Multi-Function Timer 1.	8	8	8	D3
	DTTI2X_1		202	-	-	-
	FRCK2_0	16-bit free-run timer ch 2 external clock input pin	17	16	13	F3
	FRCK2_1		197	165	135	C6
	IC20_0	16-bit input capture input pin of Multi-Function Timer 2. ICxx describes channel number.	9	9	9	D4
	IC20_1		201	-	-	-
	IC21_0		14	13	10	E5
	IC21_1		200	-	-	-
	IC22_0		15	14	11	F1
	IC22_1		199	-	-	-
	IC23_0		16	15	12	F2
	IC23_1		198	166	136	D6
	RTO20_0 (PPG20_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	2	2	2	B2
	RTO20_1 (PPG20_1)		203	-	-	-
	RTO21_0 (PPG20_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	3	3	3	C2
	RTO21_1 (PPG20_1)		204	-	-	-
	RTO22_0 (PPG22_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	4	4	4	C3
	RTO22_1 (PPG22_1)		205	-	-	-
	RTO23_0 (PPG22_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	5	5	5	D5
	RTO23_1 (PPG22_1)		206	-	-	-
	RTO24_0 (PPG24_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	6	6	6	D2
	RTO24_1 (PPG24_1)		207	167	-	E6
	RTO25_0 (PPG24_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	7	7	7	D1
	RTO25_1 (PPG24_1)		208	168	-	B5

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation/GPIO function. When the main oscillation is selected: • Oscillation feedback resistor: approximately 1 MΩ • Standby mode control When the GPIO is selected: • CMOS level output. • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$
B		• CMOS level hysteresis input • Pull-up resistor: approximately 50 kΩ

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • Available to control of PZR registers (pseudo-open drain control) • For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856).
J		CMOS level hysteresis input
K		• CMOS level output • TTL level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$

Latch-Up

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic npnp junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

11. Pin Status In Each CPU State

The terms used for pin status have the following meanings:

■ **INITX = 0**

This is the period when the INITX pin is at the L level.

■ **INITX = 1**

This is the period when the INITX pin is at the H level.

■ **SPL = 0**

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

■ **SPL = 1**

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

■ **Input enabled**

Indicates that the input function can be used.

■ **Internal input fixed at 0**

This is the status that the input function cannot be used. Internal input is fixed at L.

■ **Hi-Z**

Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■ **Setting disabled**

Indicates that the setting is disabled.

■ **Maintain previous state**

Maintains the state that was immediately prior to entering the current mode.

If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

■ **Analog input is enabled**

Indicates that the analog input is enabled.

■ **Trace output**

Indicates that the trace function can be used.

■ **GPIO selected**

In Deep standby mode, pins switch to the general-purpose I/O port.

■ **Setting prohibition**

Prohibition of a setting by specification limitation

12.4 AC Characteristics

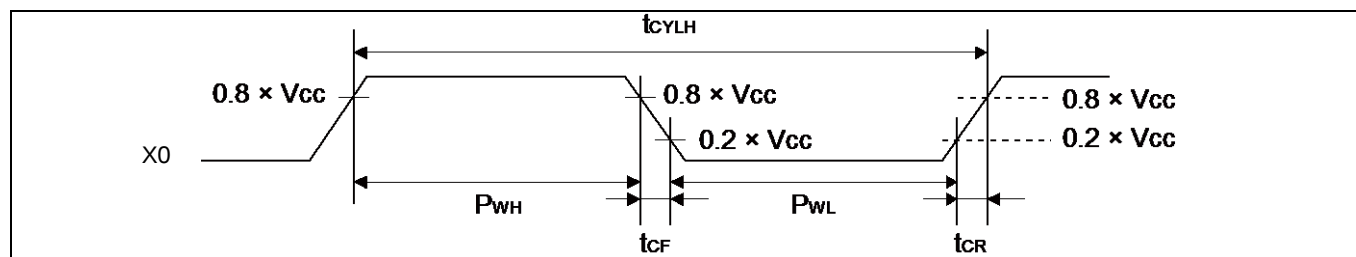
12.4.1 Main Clock Input Characteristics

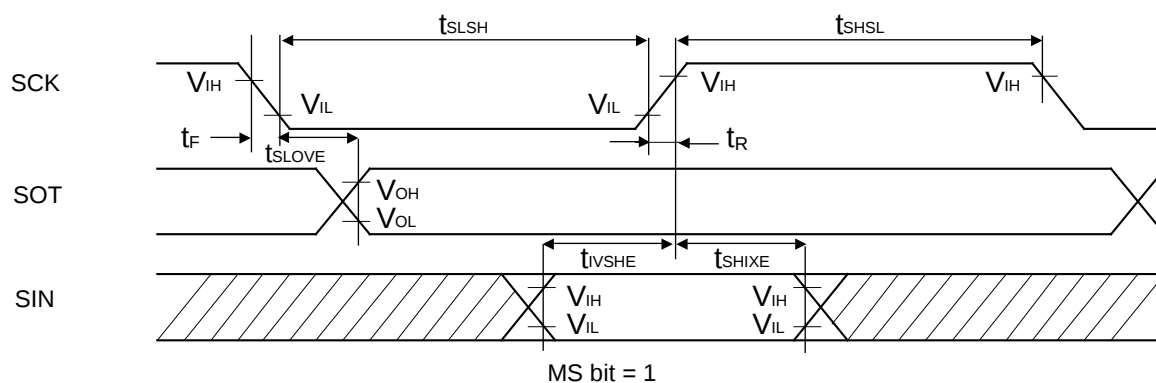
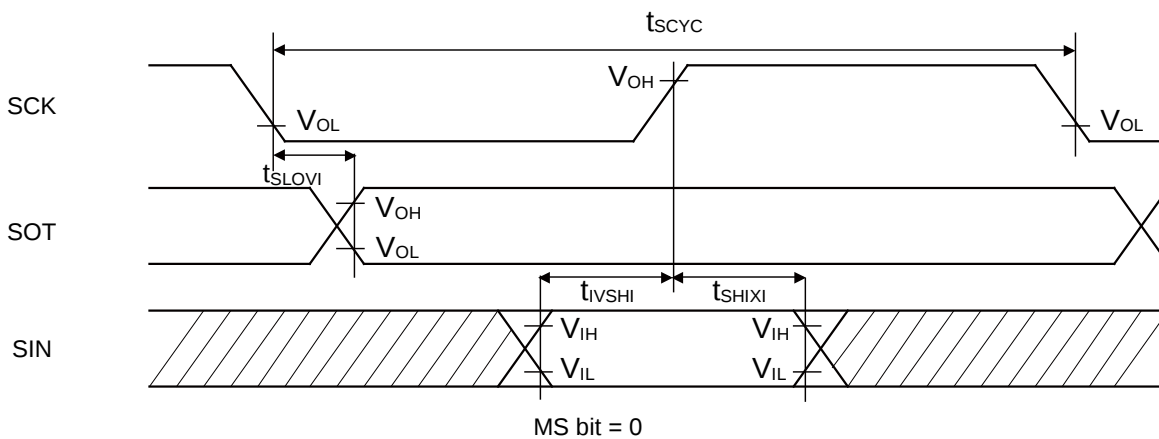
($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f _{CH}	X0, X1	V _{CC} ≥ 4.5 V	4	48	MHz	When crystal oscillator is connected
			V _{CC} < 4.5 V	4	20		
			V _{CC} ≥ 4.5 V	4	48	MHz	When using external clock
			V _{CC} < 4.5 V	4	20		
Input clock cycle	t _{CYLH}		V _{CC} ≥ 4.5 V	20.83	250	ns	When using external clock
			V _{CC} < 4.5 V	50	250		
Input clock pulse width	-		P _{WH} /t _{CYLH} , P _{WL} /t _{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t _{CF} , t _{CR}		-	-	5	ns	When using external clock
Internal operating clock *1 frequency	f _{CC}	-	-	-	200	MHz	Base clock (HCLK/FCLK)
	f _{CP0}	-	-	-	100	MHz	APB0bus clock *2
	f _{CP1}	-	-	-	200	MHz	APB1bus clock *2
	f _{CP2}	-	-	-	100	MHz	APB2bus clock *2
Internal operating clock *1 cycle time	t _{CYCC}	-	-	5	-	ns	Base clock (HCLK/FCLK)
	t _{CYCP0}	-	-	10	-	ns	APB0bus clock *2
	t _{CYCP1}	-	-	5	-	ns	APB1bus clock *2
	t _{CYCP2}	-	-	10	-	ns	APB2bus clock *2

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

*2: For more about each APB bus to which each peripheral is connected, see 8. Block Diagram in this data sheet.





High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5V		V _{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKX	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↓→SOT delay time	t _{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t _{IVSHI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↑→SIN hold time	t _{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t _{SLSH}	SCKX	External shift clock operation	2t _{CYCP} - 5	-	2t _{CYCP} - 5	-	ns
Serial clock H pulse width	t _{SHSL}	SCKX		t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↓→SOT delay time	t _{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t _{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t _{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t _F	SCKX		-	5	-	5	ns
SCK rise time	t _R	SCKX		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
No chip select: SIN4_0, SOT4_0, SCK4_0
Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)

12.4.13 External Input Timing

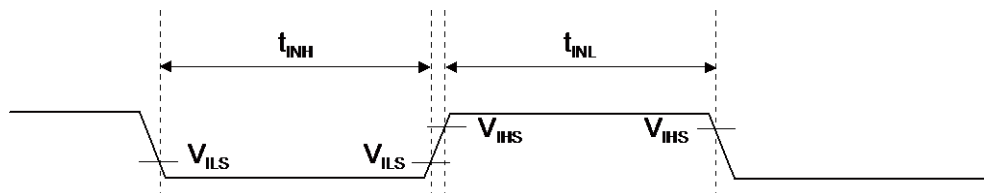
($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH} , t_{INL}	ADTGx	-	$2t_{CYCP}^{*1}$	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTlxX	-	$2t_{CYCP}^{*1}$	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP} + 100^{*1}$	-	ns	External interrupt, NMI
				500^{*2}	-	ns	
		WKUPx	-	500^{*3}	-	ns	Deep standby wake up

*1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 8. Block Diagram in this data sheet.

*2: When in Stop mode, in Timer mode

*3: When in Deep Standby RTC mode, in Deep Standby Stop mode



Fast mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f _{SCL}	C _L = 30 pF, R = (V _p /I _{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t _{HDSTA}		0.26	-	μs	
SCL clock L width	t _{LOW}		0.5	-	μs	
SCL clock H width	t _{HIGH}		0.26	-	μs	
SCL clock frequency	t _{SUSTA}		0.26	-	μs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t _{HDDAT}		0	0.45*2, *3	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t _{SUSTO}		0.26	-	μs	
Bus free time between "Stop condition" and "START condition"	t _{BUF}		0.5	-	μs	
Noise filter	t _{SP}	60 MHz ≤ t _{CYCP} < 80 MHz	6 t _{CYCP} *4	-	ns	*5
		80 MHz ≤ t _{CYCP} ≤ 100 MHz	8 t _{CYCP} *4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

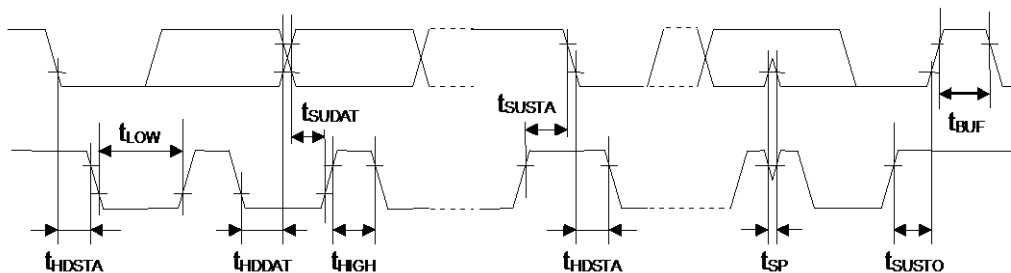
*2: The maximum t_{HDDT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

*3: The Fast mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns."

*4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see 8.Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

*6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I²C Fm+ in the EPFR register.
See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.



12.4.19 Ethernet-MAC Timing

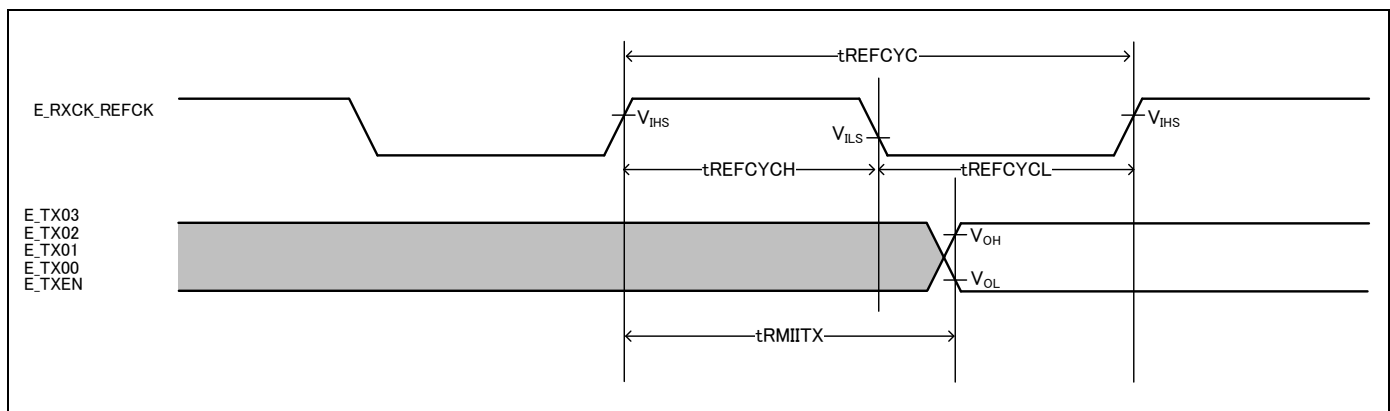
RMII Transmission (100 Mbps/10 Mbps)

(ETHV_{CC} = 3.0V to 3.6V, 4.5V to 5.5V*¹, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time* ²	t _{REFCYC}	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	t _{REFCYCH}	E_RXCK_REFCK	t _{REFCYCH} /t _{REFCYC}	35	65	%
Reference clock Low-pulse-width duty cycle	t _{REFCYCL}	E_RXCK_REFCK	t _{REFCYCL} /t _{REFCYC}	35	65	%
Transmitted data → REFCK ↑ delay time	t _{RMIITX}	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	12	ns

*1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

*2: The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.



RMII Receiving (100 Mbps/10 Mbps)

(ETHV_{CC} = 3.0V to 3.6V, 4.5V to 5.5V, V_{SS} = 0V, C_L = 25 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Reference clock cycle time*	t _{REFCYC}	E_RXCK_REFCK	20 ns (typical)	-	-	ns
Reference clock High-pulse-width duty cycle	t _{REFCYCH}	E_RXCK_REFCK	t _{REFCYCH} /t _{REFCYC}	35	65	%
Reference clock Low-pulse-width duty cycle	t _{REFCYCL}	E_RXCK_REFCK	t _{REFCYCL} /t _{REFCYC}	35	65	%
Received data → REFCK ↑ Setup time	t _{RMIIRXS}	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	4	-	ns
Received data → REFCK ↑ Hold time	t _{RMIIRXH}	E_RX03, E_RX02, E_RX01, E_RX00, E_RXDV	-	2	-	ns

*: The reference clock is fixed to 50 MHz in the RMII specifications.
The clock accuracy should meet the PHY-device specifications.

