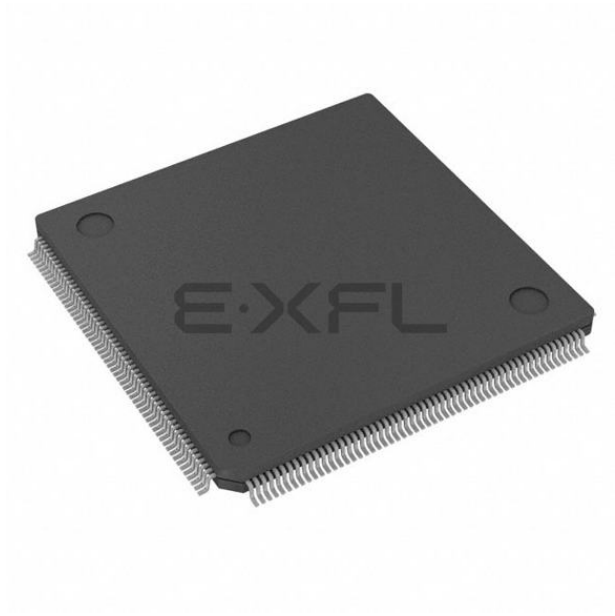

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	190
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	216-LQFP
Supplier Device Package	216-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2ccal0agl2000a

General Purpose I/O Port
This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144-pin package
- Some pins 5 V tolerant I/O.
  See "4. Pin Descriptions" and "5. I/O Circuit Type" for the corresponding pins.

Multi-function Timer (Max three units)
The multi-function timer is composed of the following blocks:

Minimum resolution: 5.00 ns

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 6 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)
The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC; Max four channels)
The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)
The dual timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

Watch Counter
The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

External Interrupt Controller Unit
- External interrupt input pin: Max 32 pins
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs: a "hardware" watchdog and a "software" watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. The hardware watchdog is thus active in any power saving mode except RTC mode and Stop mode.

Cyclic Redundancy Check (CRC) Accelerator
The CRC accelerator helps to verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

Table of Contents

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External interrupt	INT21_0	External interrupt request 21 input pin	96	79	63	L10
	INT21_1		90	75	-	L9
	INT22_0	External interrupt request 22 input pin	99	82	66	N11
	INT22_1		78	63	-	K5
	INT23_0	External interrupt request 23 input pin	56	46	38	N2
	INT23_1		79	64	-	K6
	INT24_0	External interrupt request 24 input pin	147	121	97	F13
	INT24_1		131	107	87	H12
	INT25_0	External interrupt request 25 input pin	153	123	99	E11
	INT25_1		117	97	81	K14
	INT26_0	External interrupt request 26 input pin	156	126	102	D12
	INT26_1		142	116	92	G10
	INT27_0	External interrupt request 27 input pin	157	127	103	D13
	INT27_1		143	117	93	G9
	INT28_0	External interrupt request 28 input pin	190	158	128	A7
	INT28_1		207	167	-	E6
	INT29_0	External interrupt request 29 input pin	198	166	136	D6
	INT29_1		208	168	-	B5
	INT30_0	External interrupt request 30 input pin	209	169	137	C5
	INT30_1		195	163	133	F7
	INT31_0	External interrupt request 31 input pin	212	172	140	B3
	INT31_1		196	164	134	B6
	NMIX	Non-maskable interrupt input pin	158	128	104	C13

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1,*2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1,*3	$USBV_{CC}0$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1,*3	$USBV_{CC}1$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for Ethernet-MAC) *1, *4	$ETHV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1 ,*5	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1 ,*6	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1 ,*6	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	Except for USB and Ethernet-MAC pin
		V_{SS} - 0.5	$USBV_{CC}0$ + 0.5 (≤ 6.5 V)	V	USB ch 0 pin
		V_{SS} - 0.5	$USBV_{CC}1$ + 0.5 (≤ 6.5 V)	V	USB ch 1 pin
		V_{SS} - 0.5	$ETHV_{CC}$ + 0.5 (≤ 6.5 V)	V	Ethernet-MAC Pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current *7	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	10 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current *8	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			10	mA	10 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total maximum output current *9	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *7	I_{OH}	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	10 mA type
			- 20	mA	12 mA type
H level average output current *8	I_{OHAV}	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 10	mA	10 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *9	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	200	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: $USBV_{CC}0$, $USBV_{CC}1$ must not drop below V_{SS} - 0.5 V.

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7 *9	5.5	V	
Power supply voltage (for USB ch 0)		$USBV_{CC}0$	-	3.0	3.6 ($\leqV_{CC}$)	V	*1
				2.7	5.5 ($\leqV_{CC}$)		*2
Power supply voltage (for USB ch 1)		$USBV_{CC}1$	-	3.0	3.6 ($\leqV_{CC}$)	V	*3
				2.7	5.5 ($\leqV_{CC}$)		*4
Power supply voltage (for Ethernet-MAC)		$ETHV_{CC}$	-	3.0	3.6 ($\leqV_{CC}$)	V	*5
				4.5	5.5 ($\leqV_{CC}$)		*5
				2.7	5.5 ($\leqV_{CC}$)		*6
Power supply voltage (VBAT)		V_{BAT}	-	1.65	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	$AV_{CC} = V_{CC}$
Analog reference voltage		AVRH	-	*8	AV_{CC}	V	
		AVRL	-	AV_{SS}	AV_{SS}	V	
Operating temperature	Junction temperature	T_J	-	- 40	+ 125	°C	
	Ambient temperature	T_A	-	-40	*7	°C	

*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0)

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80)

*3: When P83/UDP1 and P82/UDM1 pins are used as USB (UDP1, UDM1)

*4: When P83/UDP1 and P82/UDM1 pins are used as GPIO (P83, P82)

*5: When the pins in Ethernet-MAC Pins, except P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pin

*6: When the pins in Ethernet-MAC Pins, except P6E/ADTG_5/SCK4_1/IC23_1/INT29_0/E_PPS pin, are used as Ethernet-MAC pin

*7: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).
The calculation formula of the ambient temperature (T_A) is:

$T_A (Max) = T_J(Max) - Pd(Max) \times \theta_{JA}$

Pd: Power dissipation (W)
θ_{JA}: Package thermal resistance (°C/W)

$Pd (Max) = V_{CC} \times I_{CC} (Max) + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (- I_{OH}))$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

*8: The minimum value of analog reference voltage depends on the value of compare clock cycle (Tcck). See 12.5. 12-bit A/D Converter for the details.

*9: For the voltage range between V_{CC}(min) and the low voltage detection reset (VDH), the MCU must be clocked from either the High-speed CR or the low-speed CR.

12.4 AC Characteristics

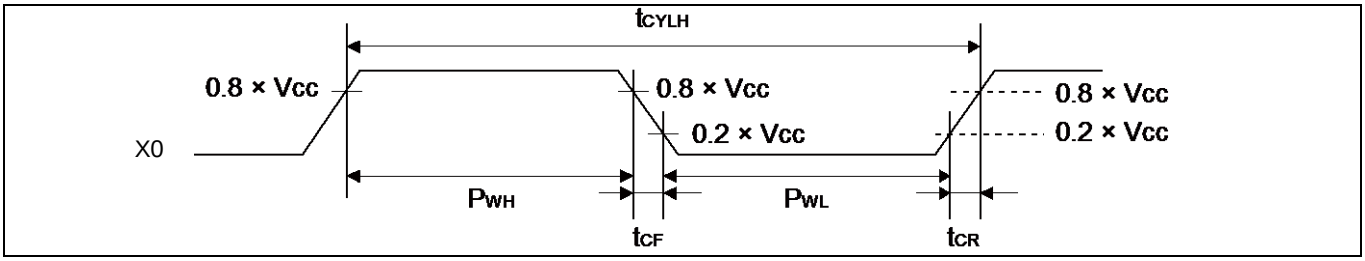
12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥4.5 V	4	48	MHz	When crystal oscillator is connected
			V_{CC} < 4.5 V	4	20		
			V_{CC} ≥4.5 V	4	48	MHz	When using external clock
			V_{CC} < 4.5 V	4	20		
Input clock cycle	t_{CYLH}		V_{CC} ≥4.5 V	20.83	250	ns	When using external clock
			V_{CC} < 4.5 V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock *1 frequency	f_{CC}	-	-	-	200	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	100	MHz	APB0bus clock *2
	f_{CP1}	-	-	-	200	MHz	APB1bus clock *2
	f_{CP2}	-	-	-	100	MHz	APB2bus clock *2
Internal operating clock *1 cycle time	t_{CYCC}	-	-	5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	10	-	ns	APB0bus clock *2
	t_{CYCP1}	-	-	5	-	ns	APB1bus clock *2
	t_{CYCP2}	-	-	10	-	ns	APB2bus clock *2

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

*2: For more about each APB bus to which each peripheral is connected, see 8. Block Diagram in this data sheet.



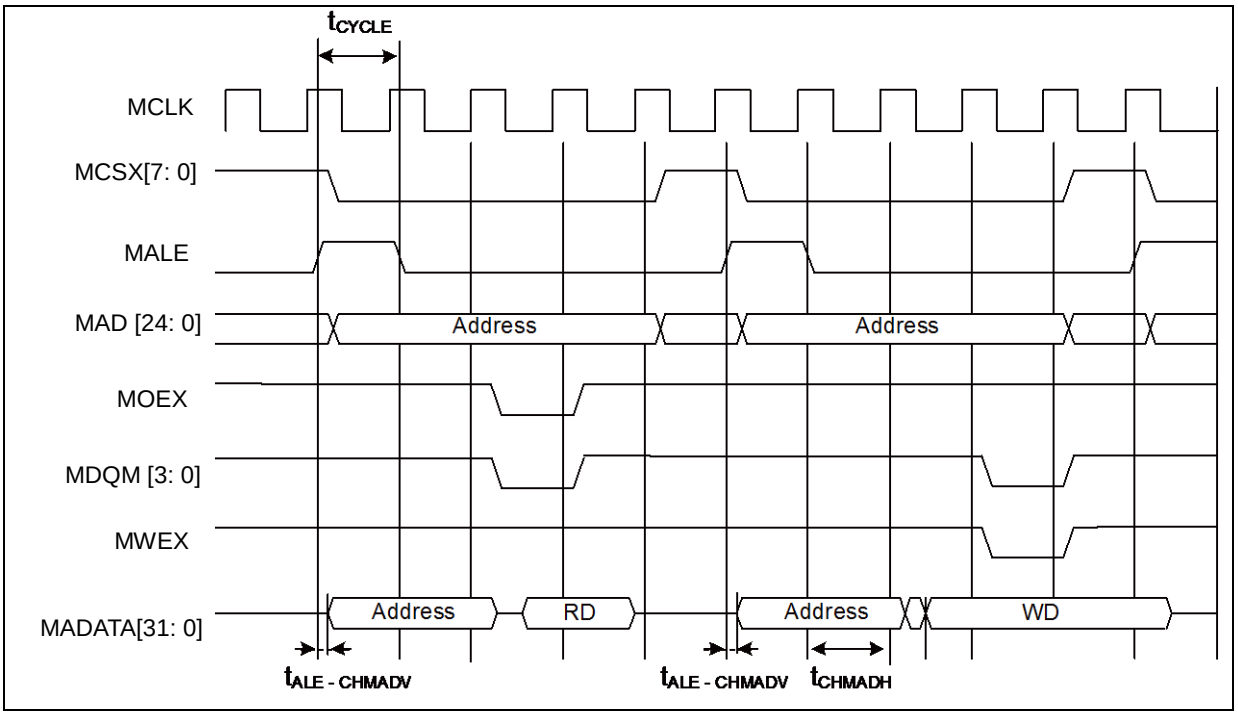
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24: 0]	-	0	10	ns	
Multiplexed address hold time	t_{CHMADH}		-	MCLK×n+0	MCLK×n+10	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*



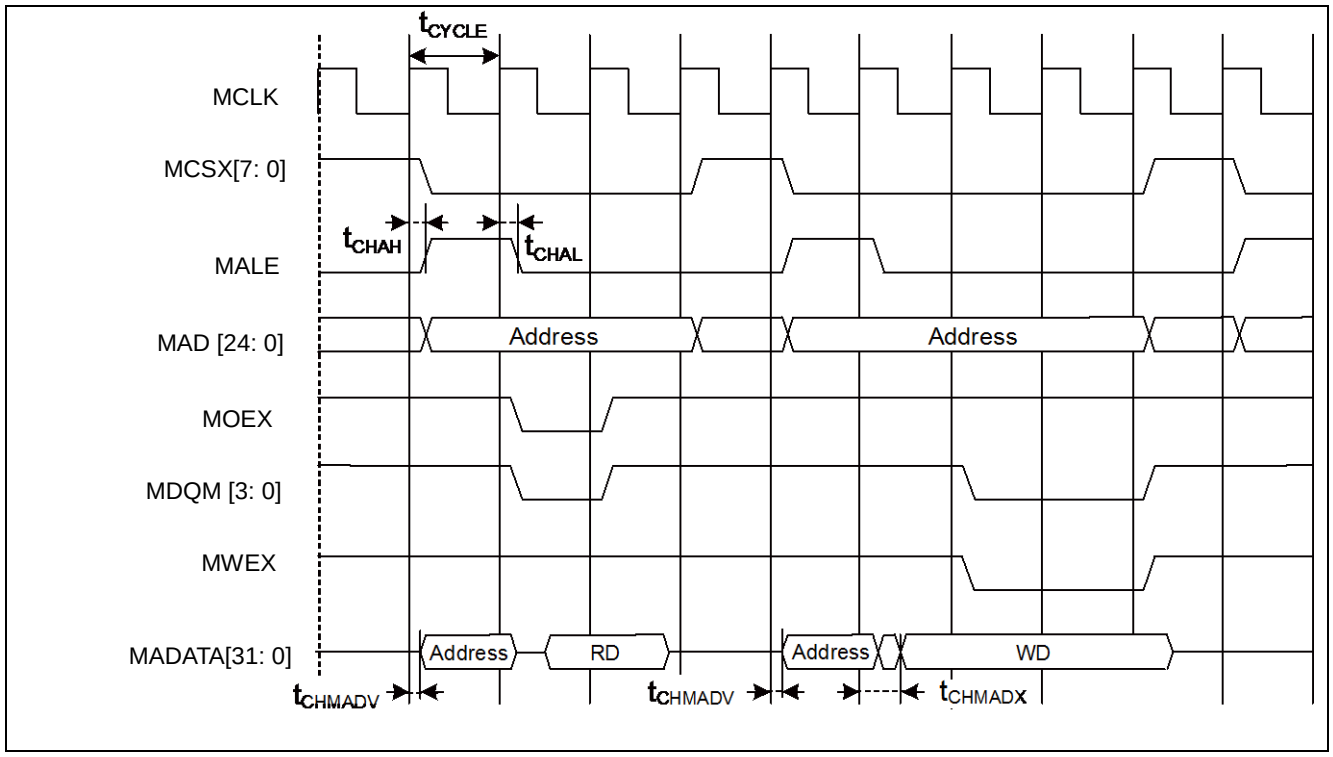
Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

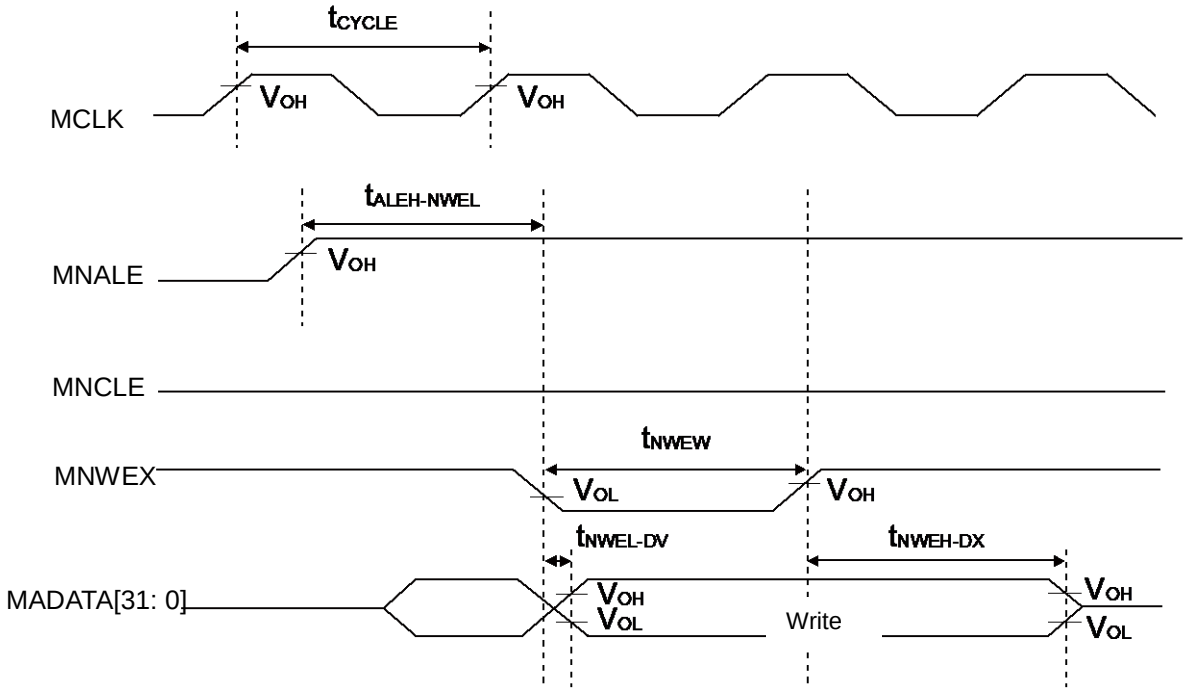
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, MALE	-	1	9		
	t_{CHAH}		-	1	9		
MCLK ↑ →Multiplexed address delay time	t_{CHMADV}	MCLK, MADATA[31: 0]	-	1	t_{OD}	ns	
MCLK ↑ →Multiplexed data output time	t_{CHMADX}		-	1	t_{OD}	ns	

Note:

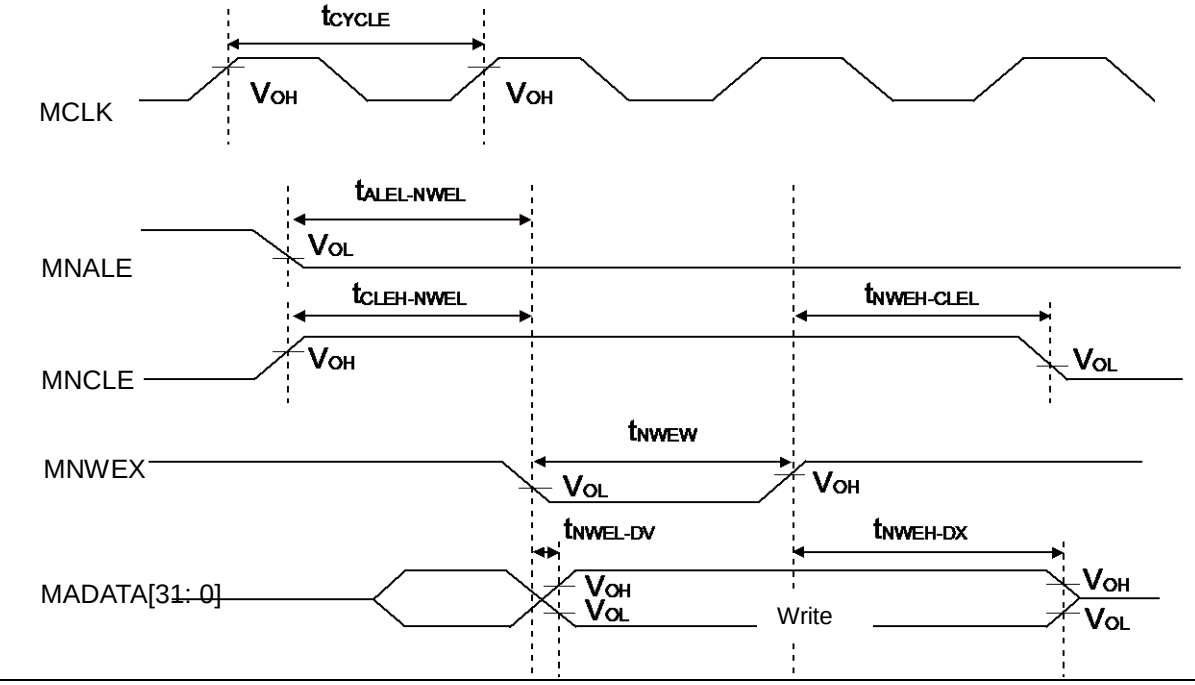
- *When the external load capacitance C_L = 30 pF*



NAND Flash Address Write



NAND Flash Command Write

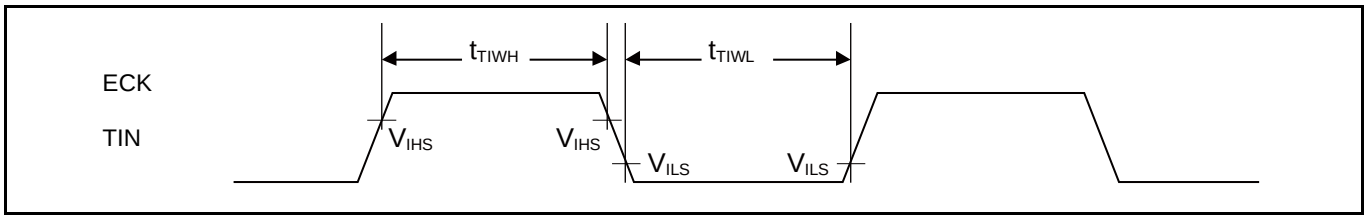


12.4.11 Base Timer Input Timing

Timer Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

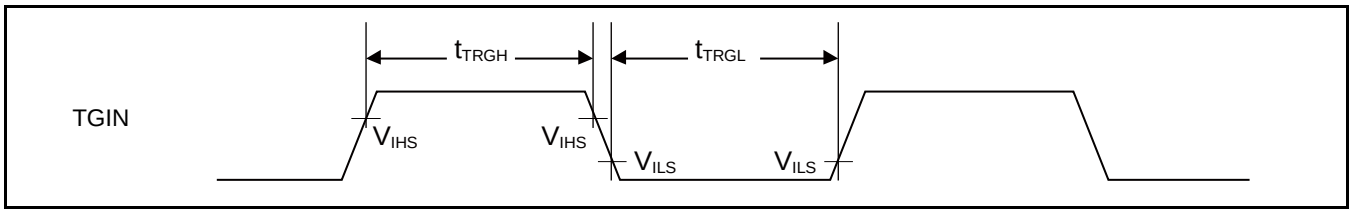
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the base timer is connected, see 8. Block Diagram in this data sheet.*

High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*
  No chip select: SIN4_0, SOT4_0, SCK4_0
  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

High-Speed Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*
  No chip select: SIN4_0, SOT4_0, SCK4_0
  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (for *, when C_L = 10 pF)*

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Min	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

12.4.15 I²C Timing

Standard-Mode, Fast-Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "Stop condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP} < 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz ≤ t_{CYCP} < 60 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	
		60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	6 t_{CYCP}*4	-	ns	
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

*3: Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns.

*4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see 8.Block Diagram in this data sheet.
When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.
When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.

*5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

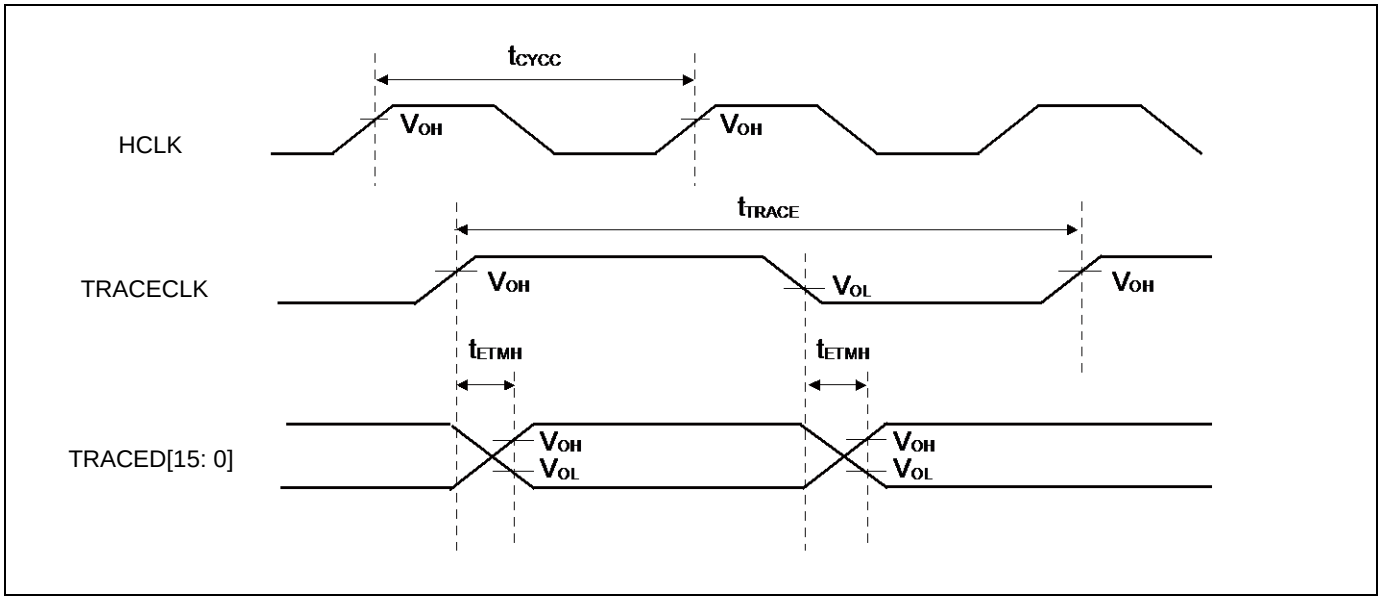
12.4.17 ETM/ HTM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	$V_{CC} \geq 4.5V$	2	9	ns	
			$V_{CC} < 4.5V$	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5V$		50	MHz	
			$V_{CC} < 4.5V$		32	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 4.5V$	20	-	ns	
			$V_{CC} < 4.5V$	31.25	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*



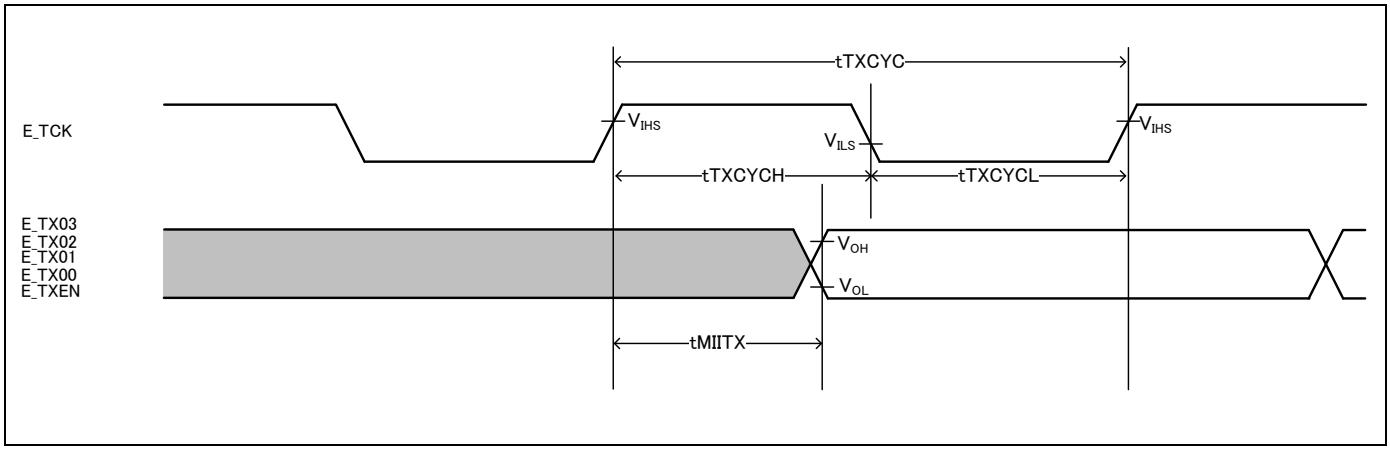
MII Transmission (100 Mbps/10 Mbps)

($ETHV_{CC}$ = 3.0V to 3.6V, 4.5V to 5.5V*1, V_{SS} = 0V, C_L = 25 pF)

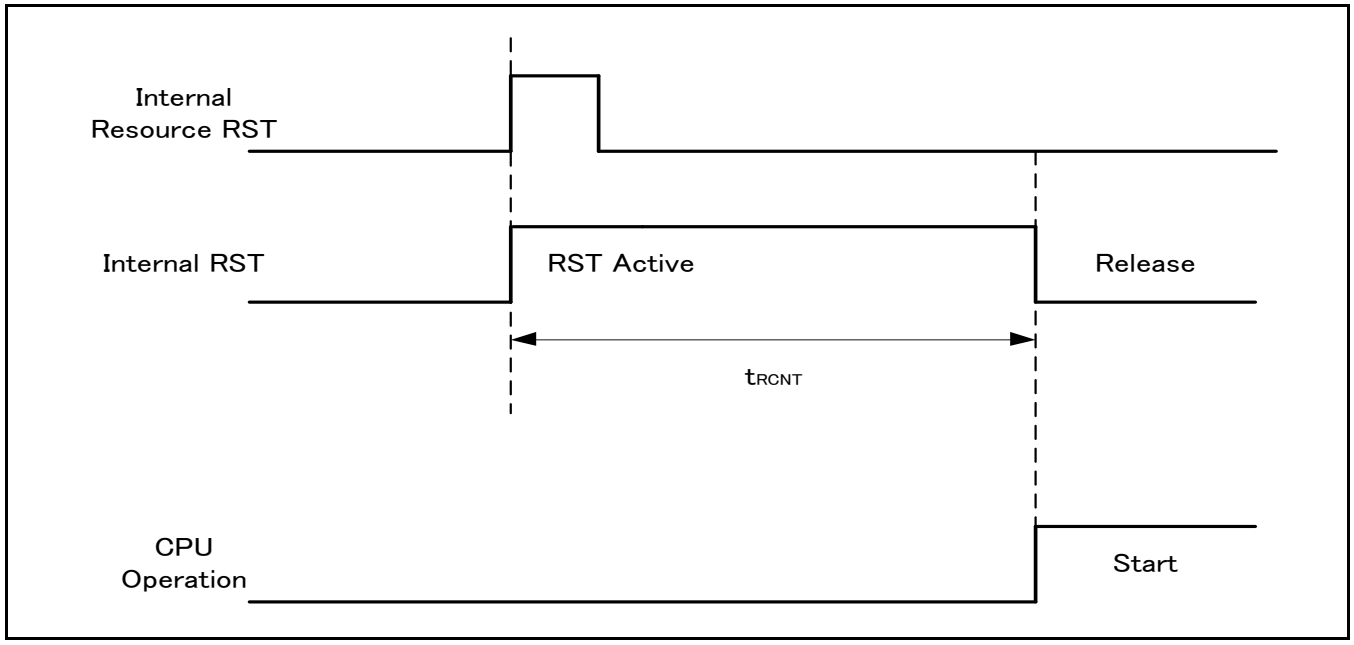
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Transmission clock Cycle time*2	t_{TXCYC}	E_TCK	100 Mbps 40 ns (typical)	-	-	ns
			100 Mbps 400 ns (typical)	-	-	ns
Transmission clock High-pulse-width duty cycle	t_{TXCYCH}	E_TCK	t_{TXCYCH}/t_{TXCYC}	35	65	%
Transmission clock Low-pulse-width duty cycle	t_{TXCYCL}	E_TCK	t_{TXCYCL}/t_{TXCYC}	35	65	%
TXCK ↑ → Transmitted data delay time	t_{MIITX}	E_TX03, E_TX02, E_TX01, E_TX00, E_TXEN	-	-	24	ns

*1: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

*2: The transmission clock is fixed to 25 MHz or 2.5 MHz in the MII specifications. The clock accuracy should meet the PHY-device specifications.



Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



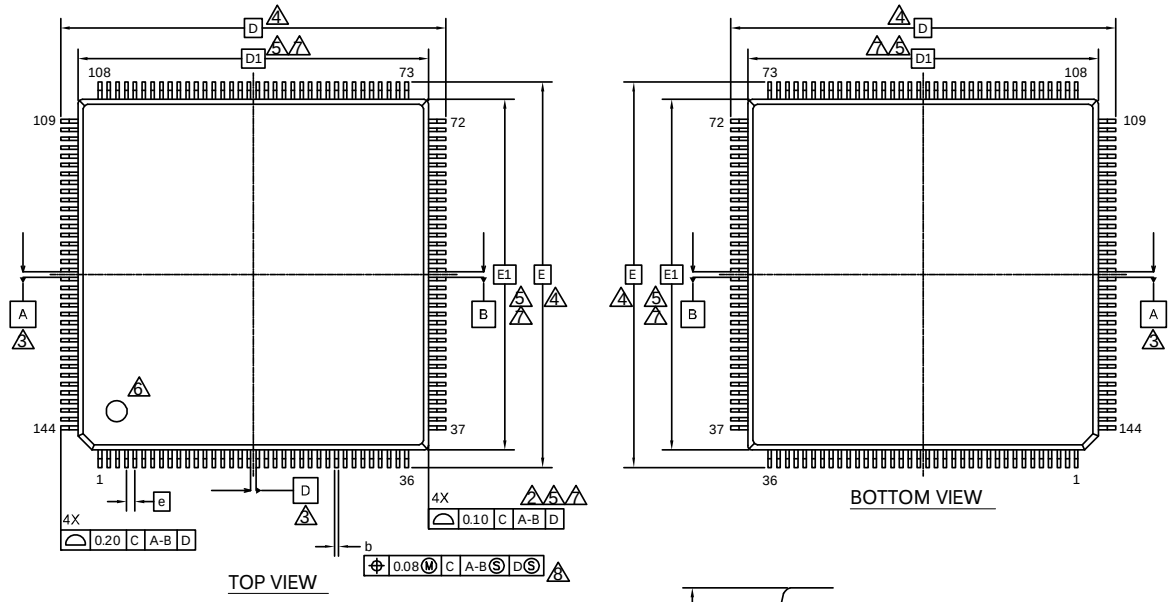
*: Depending on the low-power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each low power consumption mode.*
  See Chapter 6: Low Power Consumption mode and Operations of Standby modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-On Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS 144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 **

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 Rev**