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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/jn5148-z01-515

2.1 Pin Assignment

Pin No	Power supplies				Signal Type	Description
10, 12, 16, 18, 27, 35, 40	VB_SYNTH, VB_VCO, VB_RF2, VB_RF, VB_A, VB_RAM, VB_DIG				1.8V	Regulated supply voltage
13, 49	VDD1, VDD2				3.3V	Supplies: VDD1 for analogue, VDD2 for digital
32, 6, 3, 7, Paddle	VSS1, VSS2, VSS3, VSSS, VSSA				0V	Grounds (see appendix A.2 for paddle details)
28	NC					No connect
	General					
39	RESETN				CMOS	Reset input
8, 9	XTAL_OUT, XTAL_IN				1.8V	System crystal oscillator
	Radio					
11	VCOTUNE				1.8V	VCO tuning RC network
14	IBIAS				1.8V	Bias current control
17	RF_IN				1.8V	RF antenna
	Analogue Peripheral I/O					
21, 22, 23, 24	ADC1, ADC2, ADC3, ADC4				3.3V	ADC inputs
15	VREF				1.8V	Analogue peripheral reference voltage
29, 30	DAC1, DAC2				3.3V	DAC outputs
19, 20	COMP1M/EXT_PA_B, COMP1P/EXT_PA_C				3.3V	Comparator 1 inputs and external PA control
25, 26	COMP2M, COMP2P				3.3V	Comparator 2 inputs
	Digital Peripheral I/O					
	Primary	**Alternate Functions**				
33	SPICLK				CMOS	SPI Clock Output
36	SPIMOSI				CMOS	SPI Master Out Slave In Output
34	SPIMISO				CMOS	SPI Master In Slave Out Input
37	SPISEL0				CMOS	SPI Slave Select Output 0
38	DIO0	SPISEL1			CMOS	DIO0 or SPI Slave Select Output 1
41	DIO1	SPISEL2	PC0		CMOS	DIO1, SPI Slave Select Output 2 or Pulse Counter0 Input
42	DIO2	SPISEL3	RFRX		CMOS	DIO2, SPI Slave Select Output 3 or Radio Receive Control Output
43	DIO3	SPISEL4	RFTX		CMOS	DIO3, SPI Slave Select Output 4 or Radio Transmit Control Output
44	DIO4	CTS0	JTAG_TCK		CMOS	DIO4, UART 0 Clear To Send Input or JTAG CLK
45	DIO5	RTS0	JTAG_TMS		CMOS	DIO5, UART 0 Request To Send Output or JTAG Mode Select
46	DIO6	TXD0	JTAG_TDO		CMOS	DIO6, UART 0 Transmit Data Output or JTAG Data Output
47	DIO7	RXD0	JTAG_TDI		CMOS	DIO7, UART 0 Receive Data Input or JTAG Data Input
48	DIO8	TIM0CK_GT	PC1		CMOS	DIO8, Timer0 Clock/Gate Input or Pulse Counter1 Input
50	DIO9	TIM0CAP	32KXTALIN	32KIN	CMOS	DIO9, Timer0 Capture Input, 32K External Crystal Input or 32K Clock Input

At reset, the contents of this memory are copied into RAM by the software boot loader. The Flash memory devices that are supported as standard through the JN5148 bootloader are given in Table 1. NXP recommends that where possible one of these devices should be selected.

Manufacturer	Device Number
SST (Silicon Storage Technology)	25VF010A (1Mbit device)
Numonyx	M25P10-A (1Mbit device), M25P40 (4Mbit device)

Table 1: Supported Flash Memories

Applications wishing to use an alternate Flash memory device should refer to application note [2] JN-AN-1038 Programming Flash devices not supported by the JN51xx ROM-based bootloader. This application note provides guidance on developing an interface to an alternate device.

4.4.1 External Memory Encryption

The contents of the external serial memory may be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in eFuse.

When bootloading program code from external serial memory, the JN5148 automatically accesses the encryption key to execute the decryption process. User program code does not need to handle any of the decryption process; it is transparent.

With encryption enabled, the time taken to boot code from external flash is increased.

4.5 Peripherals

All peripherals have their registers mapped into the memory space. Access to these registers requires 3 clock cycles. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see the JN51xx Integrated Peripherals API User Guide (JN-UG-3066)[5].

4.6 Unused Memory Addresses

Any attempt to access an unpopulated memory area will result in a bus error exception (interrupt) being generated.

6 Reset

A system reset initialises the device to a pre-defined state and forces the CPU to start program execution from the reset vector. The reset process that the JN5148 goes through is as follows.

When power is applied, the 32kHz RC oscillator starts up and stabilises, which takes approximately 100μsec. At this point, the 32MHz crystal oscillator is enabled and power is applied to the processor and peripheral logic. The logic blocks are held in reset until the 32MHz crystal oscillator stabilises, typically this takes 0.75ms. Then the internal reset is removed from the CPU and peripheral logic and the CPU starts to run code beginning at the reset vector, consisting of initialisation code and the resident boot loader. [7] Section 22.3.1 provides detailed electrical data and timing.

The JN5148 has five sources of reset:

- Internal Power-on Reset
- External Reset
- Software Reset
- Watchdog timer
- Brown-out detect

Note: When the device exits a reset condition, device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, then the device must be held in reset until the operating conditions are met. (See section 22.3)

6.1 Internal Power-on Reset

For the majority of applications the internal power-on reset is capable of generating the required reset signal. When power is applied to the device, the power-on reset circuit monitors the rise of the VDD supply. When the VDD reaches the specified threshold, the reset signal is generated and can be observed as a rising edge on the RESETN pin. This signal is held internally until the power supply and oscillator stabilisation time has elapsed, when the internal reset signal is then removed and the CPU is allowed to run.

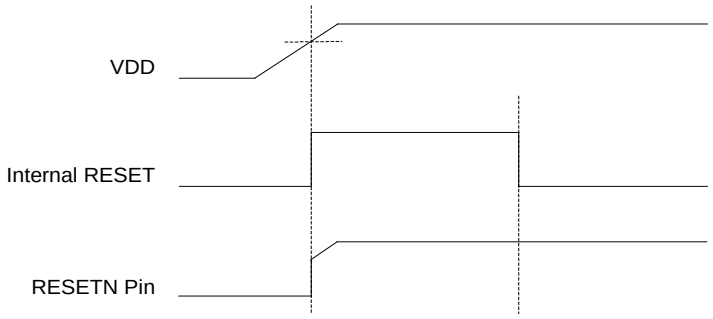


Figure 11: Internal Power-on Reset

When the supply drops below the power on reset ‘falling’ threshold, it will re-trigger the reset. Use of the external reset circuit show in Figure 12 is suggested.

8.1.1 Radio External Components

In order to realise the full performance of the radio it is essential that the reference PCB layout and BOM are carefully followed. See Appendix B.4.

The radio is powered from a number of internal 1.8V regulators fed from the analogue supply VDD1, in order to provide good noise isolation between the digital logic of the JN5148 and the analogue blocks. These regulators are also controlled by the baseband controller and protocol software to minimise power consumption. Decoupling for internal regulators is required as described in section 2.2.1, Power Supplies

For single ended antennas or connectors, a balun is not required, however a matching network is needed.

The RF matching network requires three external components and the IBIAS pin requires one external component as shown in schematic in B.4.1. These components are critical and should be placed close to the JN5148 pins and analogue ground as defined in Table 8: JN5148 Printed Antenna Reference Module Components and PCB Layout Constraints. Specifically, the output of the network comprising L2, C1 and L1 is designed to present an accurate match to a 50 ohm resistive network as well as provide a DC path to the final output stage or antenna. Users wishing to match to other active devices such as amplifiers should design their networks to match to 50 ohms at the output of L1

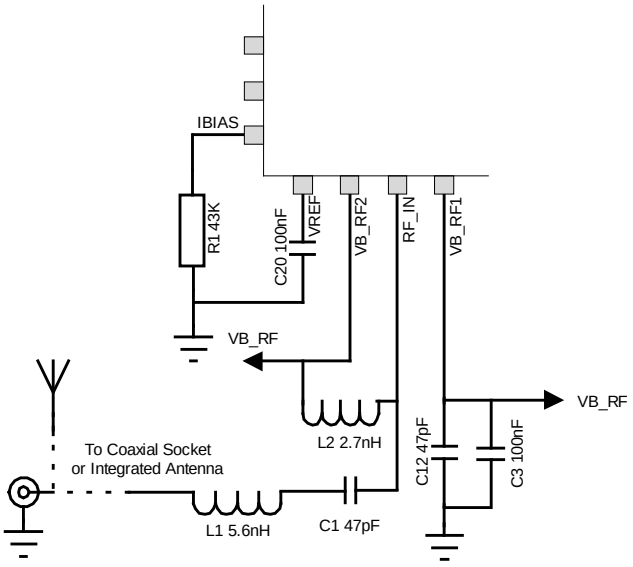


Figure 15 External Radio Components

8.1.2 Antenna Diversity

Support is provided for antenna diversity. Antenna diversity is a technique that maximises the performance of an antenna system. It allows the radio to switch between two antennas that have very low correlation between their received signals. Typically, this is achieved by spacing two antennas around 0.25 wavelengths apart or by using two orthogonal polarisations. So, if a packet is transmitted and no acknowledgement is received, the radio system can switch to the other antenna for the retry, with a different probability of success.

The JN5148 provides an output (ADO) on DIO12 that is asserted on odd numbered retries and optionally its complement (ADE) on DIO13, that can be used to control an antenna switch; this enables antenna diversity to be implemented easily (see Figure 16 and Figure 17).

16 Four-Wire Digital Audio Interface

The JN5148 includes a four-wire digital audio interface that can be used for interfacing to audio CODECs. The following features are supported:

- Compatible with the industry standard I²S interface
- Option to support I²S, left justified and right justified modes
- Optional support for connection to mono sample FIFO with data transferred on the left or right channel
- Master only
- Transmit on falling edge and receive on rising edge
- Up to 8MHz maximum clock range
- Maximum system size of 32-bits, allowing up to 16-bits per channel (left or right channels)
- Option for pad bit insertion, allowing length of transfer per channel to be anything from 16 to 32 bits
- Data Transfer size range of 1 to 16-bits per channel
- Option to invert WS (normally 0 for left, but allow 1 for left instead)
- Continuous clock output option to support CODECs which use it as a clock source
- Separate input and output data lines
- Option to invert idle state of WS (to indicate left or right)

The Word Select (WS), Data In (SDIN), Clock (SCK) and Data Out (SDOUT) lines are alternate functions of DIO lines 12,13,17 and 18 respectively.

Data transfer is always bidirectional. Data placed in the Data Buffer before a transfer command is issued will be transmitted on SDOUT whilst the data received on SDIN will be placed in the Data Buffer at the end of the transfer. Indication that a transfer has completed is by means of an interrupt or by polling a status bit.

Left channel data is always sent first, with MSB first on each channel. The interface will always transfer both left and right channel data. For mono data transfer, the user should pad out the unused channel with 0's, and ignore any data returned on the unused channel.

The length of a data transfer is derived as follows:

- When padding is disabled – Data Transfer Length = 2 x Data Transfer Size
- When padding is enabled – Data Transfer Length = 2 x (16 + Extra Pad Length)

Timing of the 3 main modes is shown in Figure 38, Figure 39 and Figure 40. The Data Buffer shows how the data is stored and how it will be transferred onto the interface. SD Max Size indicates how the maximum transfer size (16 with no additional padding) will transfer, whilst SD 3-bits indicates how 3 bits of data will be aligned when padding is enabled. Received data in the Data Buffer will always be padded out with 0's if the Data Transfer Size is less than 16-bits, and any bits received beyond 16-bits when extra padding is used, will be discarded. In the examples, the polarity of WS is shown with Left channel = 0, and the idle state is Right Channel.

17 Random Number Generator

A random number generator is provided which creates a 16-bit random number each time it is invoked. Consecutive calls can be made to build up any length of random number required. Each call takes approximately 0.25msec to complete. Alternatively, continuous generation mode can be used where a new number is generated approximately every 0.25msec. In either mode of operation an interrupt can be generated to indicate when the number is available, or a status bit can be polled.

The random bits are generated by sampling the state of the 32MHz clock every 32kHz system clock edge. As these clocks are asynchronous to each other, each sampled bit is unpredictable and hence random.

18 Sample FIFO

A 10 deep FIFO is provided to buffer data between the CPU and either the four-wire digital audio interface or the DAC/ ADC. It supports single channel input and output data, up to 16 bits wide. When used it can reduce the rate at which the processor has to generate/process data, and this may allow more efficient operation. Interrupts can be generated based on fill levels and also FIFO empty and full conditions. Normal configuration of the digital audio interface or the DAC/ ADC is still required when accessing the data via the FIFO.

When used with the DAC / ADC functions a timing signal is generated by the DAC/ ADC functions to control the transfer of data to and from the FIFO and the analogue peripherals. The transfers will occur at the sample rate configured within the DAC / ADC functions.

When the FIFO is linked to the four-wire digital audio interface, timer 2 must be used to generate an internal timing signal to control the flow of data across the interface. The timer does not require any external pins to be enabled. The timer should be set up to produce a PWM output with a rising edge generated every time a digital audio transfer is required. The transfer rate is typically configured to be the audio sample rate, e.g. 8kHz. If the transfer rate is too fast or slow data will be transferred correctly between the FIFO and the digital audio block.

all the data specified in the length field to the JN5148. The master must then deassert IP_SEL to show the transfer is complete.

The master may initiate a transfer to read data from the JN5148 by asserting the slave select pin, IP_SEL, and generating its status byte on IP_DI with RXRDY set. After receiving the status byte from the JN5148, it should check that the JN5148 has a buffer ready by reading the TXRDY bit of the received status byte. If the TXRDY bit is 0, indicating that the JN5148 does not have data to send, it must terminate the transfer by deasserting IP_SEL unless it is transmitting data to the JN5148. If the TXRDY bit is 1, indicating that the JN5148 can send data, then the master must generate a further 8 clocks on IP_CLK in order to receive the message length on IP_DO. The master must continue clocking the interface until sufficient clocks have been generated to receive all the data specified in the length field from the JN5148. The master should then deassert IP_SEL to show the transfer is complete.

Data can be sent in both directions at once and the master must ensure both transfers have completed before deasserting IP_SEL.

20.3 Comparators

The JN5148 contains two analogue comparators COMP1 and COMP2 that are designed to have true rail-to-rail inputs and operate over the full voltage range of the analogue supply VDD1. The hysteresis level (common to both comparators) can be set to a nominal value of 0mV, 10mV, 20mV or 40mV. In addition, the source of the negative input signal for each comparator (COMP1M and COMP2M) can be set to the internal voltage reference, the output of DAC1 or DAC2 (COMP1 or COMP2 respectively) or the appropriate external pin. The comparator outputs are routed to internal registers and can be polled, or can be used to generate interrupts. The comparators can be disabled to reduce power consumption.

The comparators have a low power mode where the response time of the comparator is slower than normal and is specified in section 22.3.10. This mode may be used during non-sleep operation however it is particularly useful in sleep mode to wake up the JN5148 from sleep where low current consumption is important. The wakeup action and the configuration for which edge of the comparator output will be active are controlled through software. In sleep mode the negative input signal source, must be configured to be driven from the external pins.

21 Power Management and Sleep Modes

21.1 Operating Modes

Three operating modes are provided in the JN5148 that enable the system power consumption to be controlled carefully to maximise battery life.

- Active Processing Mode
- Sleep Mode
- Deep Sleep Mode

The variation in power consumption of the three modes is a result of having a series of power domains within the chip that may be controllably powered on or off.

21.1.1 Power Domains

The JN5148 has the following power domains:

- VDD Supply Domain: supplies the wake-up timers and controller, DIO blocks, Comparators, 32kHz RC and crystal oscillators. This domain is driven from the external supply (battery) and is always powered. The wake-up timers and controller, and the 32kHz RC and crystal oscillators may be powered on or off in sleep mode through software control.
- Digital Logic Domain: supplies the digital peripherals, CPU, ROM, Baseband controller, Modem and Encryption processor. It is powered off during sleep mode.
- Analogue Domain: supplies the ADC, DACs and the temperature sensor. It is powered off during sleep mode and may be powered on or off in active processing mode through software control.
- RAM Domain: supplies the RAM during sleep mode to retain the memory contents. It may be powered on or off for sleep mode through software control.
- Radio Domain: supplies the radio interface. It is powered during transmit and receive and controlled by the baseband processor. It is powered off during sleep mode.

The current consumption figures for the different modes of operation of the device is given in section 22.2.2.

21.2 Active Processing Mode

Active processing mode in the JN5148 is where all of the application processing takes place. By default, the CPU will execute at the selected clock speed executing application firmware. All of the peripherals are available to the application, as are options to actively enable or disable them to control power consumption; see specific peripheral sections for details.

Whilst in Active processing mode there is the option to doze the CPU but keep the rest of the chip active; this is particularly useful for radio transmit and receive operations, where the CPU operation is not required therefore saving power.

21.2.1 CPU Doze

Whilst in doze mode, CPU operation is stopped but the chip remains powered and the digital peripherals continue to run. Doze mode is entered through software and is terminated by any interrupt request. Once the interrupt service routine has been executed, normal program execution resumes. Doze mode uses more power than sleep and deep sleep modes but requires less time to restart and can therefore be used as a low power alternative to an idle loop.

Whilst in CPU doze the current associated with the CPU is not consumed, therefore the basic device current is reduced as shown in the figures in section 22.2.2.1.

21.3 Sleep Mode

The JN5148 enters sleep mode through software control. In this mode most of the internal chip functions are shutdown to save power, however the state of DIO pins are retained, including the output values and pull-up enables,

22.2.2 DC Current Consumption

VDD = 2.0 to 3.6V, -40 to +85º C

22.2.2.1 Active Processing

Mode:	Min	Typ	Max	Unit	Notes
CPU processing 32,16,8 or 4MHz		1600 + 280/MHz		µA	SPI, GPIOs enabled. When in CPU doze the current related to CPU speed is not consumed.
Radio transmit		15.0		mA	CPU in software doze – radio transmitting
Radio receive		17.5		mA	CPU in software doze – radio in receive mode
The following current figures should be added to those above if the feature is being used					
ADC		655		µA	Temperature sensor and battery measurements require ADC
DAC		215 / 235		µA	One / both
Comparator		73 / 0.8		µA	Normal / low-power
UART		90		µA	For each UART
Timer		30		µA	For each Timer
2-wire serial interface		70		µA	

22.2.2.2 Sleep Mode

Mode:	Min	Typ	Max	Unit	Notes
Sleep mode with I/O wakeup		0.12		µA	Waiting on I/O event
Sleep mode with I/O and RC Oscillator timer wakeup – measured at 25ºC		1.25		µA	As above, but also waiting on timer event. If both wakeup timers are enabled then add another 0.05µA
32kHz crystal oscillator		1.5		µA	As alternative sleep timer
The following current figures should be added to those above if the feature is being used					
RAM retention– measured at 25ºC		2.2		µA	For full 128kB retained
Comparator (low-power mode)		0.8		µA	Reduced response time

22.2.2.3 Deep Sleep Mode

Mode:	Min	Typ	Max	Unit	Notes
Deep sleep mode– measured at 25ºC		100		nA	Waiting on chip RESET or I/O event

Parameter	Symbol	Min	Max	Unit
Clock period	t_{ck}	125.0	-	ns
Data setup time	t_{si}	15	-	ns
Data hold time	t_{hi}	15		ns
Data invalid period	t_{vo}	-	40	ns
Select set-up period	t_{sss}	15	-	ns
Select hold period	t_{ssh}	15	-	ns
Select asserted to output data driven	t_{lz}		20	ns
Select negated to data output tri-stated	t_{hz}		20	ns

22.3.4 Two-wire Serial Interface

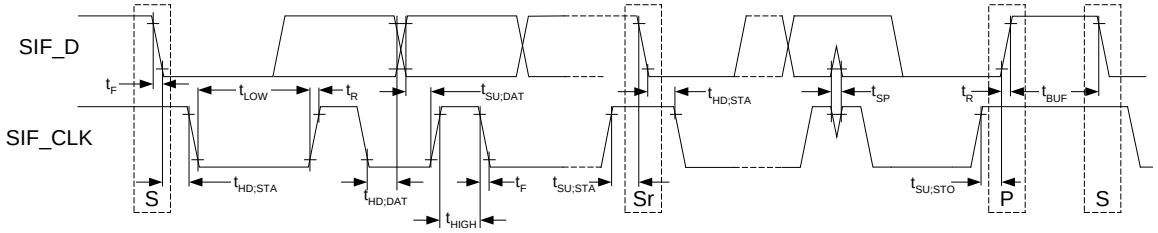
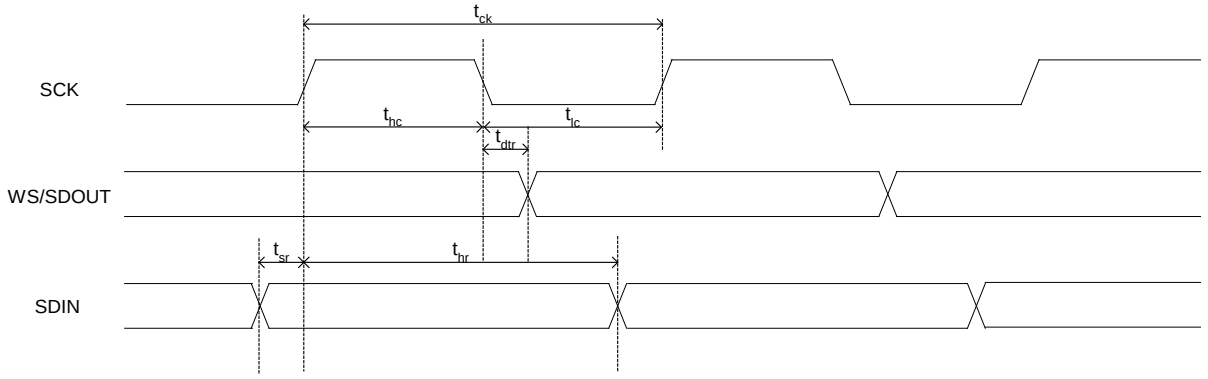


Figure 50: Two-wire Serial Interface Timing

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SIF_CLK clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4	-	0.6	-	µs
LOW period of the SIF_CLK clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SIF_CLK clock	t_{HIGH}	4	-	0.6	-	µs
Set-up time for repeated START condition	$t_{SU:STA}$	4.7	-	0.6	-	µs
Data setup time SIF_D	$t_{SU:DAT}$	0.25	-	0.1	-	µs
Rise Time SIF_D and SIF_CLK	t_R	-	1000	20+0.1Cb	300	ns
Fall Time SIF_D and SIF_CLK	t_F	-	300	20+0.1Cb	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Pulse width of spikes that will be suppressed by input filters (Note 1)	t_{SP}	-	60	-	60	ns
Capacitive load for each bus line	C_b	-	400	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nl}	0.1VDD	-	0.1VDD	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nh}	0.2VDD	-	0.2VDD	-	V

Note 1: This figure indicates the pulse width that is guaranteed to be suppressed. Pulse with widths up to 125nsec may alos get suppressed.

22.3.5 Four-Wire Digital Audio Interface



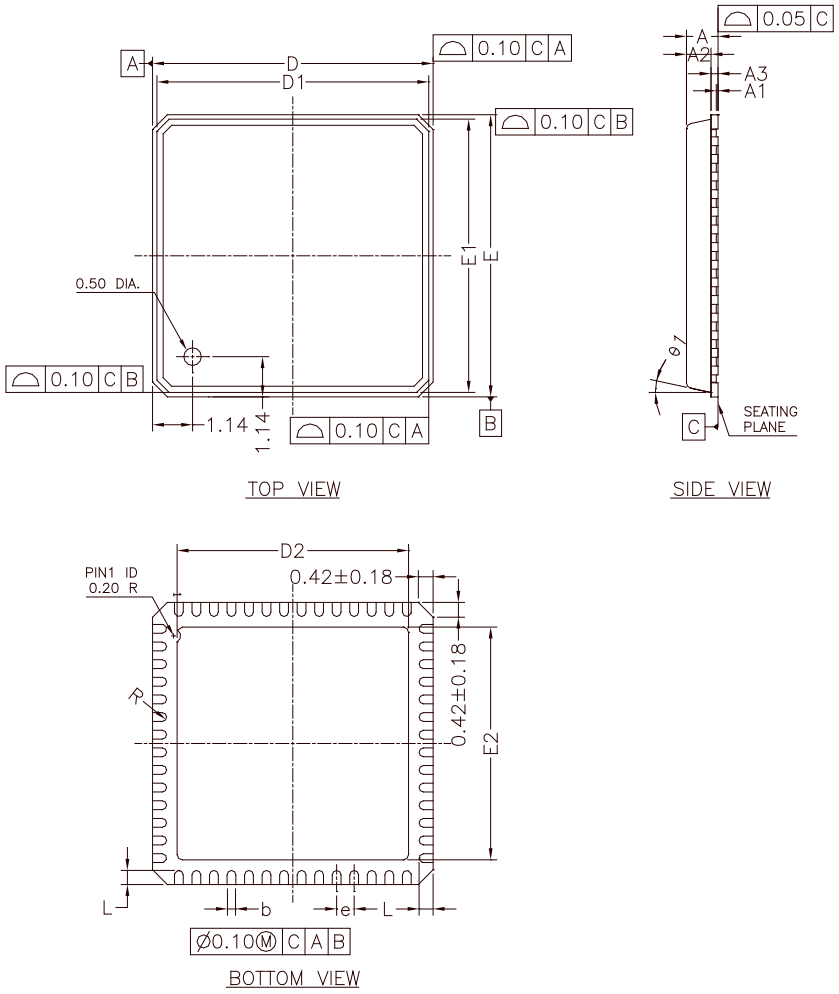
Parameter	Symbol	Maximum Frequency (8MHz)		Generic		Unit
		Min	Max	Min	Max	
DAI_SCK clock period	t_{ck}	125	-	125	-	ns
LOW period of the DAI_SCK clock	t_{lc}	43	-	$0.35t_{ck}$	-	ns
HIGH period of the DAI_SCK clock	t_{hc}	43	-	$0.35t_{ck}$	-	ns
Transmit delay time	t_{dtr}	-	50	-	$0.4t_{ck}$	ns
Receive set-up time	t_{sr}	25	-	$0.2t_{ck}$	-	ns
Receive hold time	t_{hr}	0	-	0	-	ns

22.3.6 Wakeup and Boot Load Timings

Parameter	Min	Typ	Max	Unit	Notes
Time for crystal to stabilise ready for Boot Load		0.84		ms	Reached oscillator amplitude threshold
Time for crystal to stabilise ready for radio activity		1.0		ms	
Wake up from Deep Sleep or from Sleep (memory not held)		0.84 + 0.5* program size in kBytes		ms	Assumes SPI clock to external Flash is 16MHz
Wake up from Sleep (memory held)		0.84		ms	
Wake up from CPU Doze mode		0.2		µs	
Wake up from Sleep using 24MHz RC oscillator (memory held)		0.29		ms	

Appendix A Mechanical and Ordering Information

A.1 56-pin QFN Package Drawing



Controlling Dimension: mm

Symbol	millimetres		
	Min.	Nom.	Max.
A	------	------	0.9
A1	0.00	0.01	0.05
A2	------	0.65	0.7
A3		0.20 Ref.	
b	0.2	0.25	0.3
D		8.00 bsc	
D1		7.75 bsc	
D2	6.20	6.40	6.60
E		8.00 bsc	
E1		7.75 bsc	
E2	6.20	6.40	6.60
L	0.30	0.40	0.50
e		0.50 bsc	
υ1	0°	------	12°
R	0.09	------	------
Tolerances of Form and Position			
aaa		0.10	
bbb		0.10	
ccc		0.05	

Figure 51: 56-pin QFN Package Drawings

A.2 PCB Decal

The following PCB decal is recommended; all dimensions are in millimetres (mm).

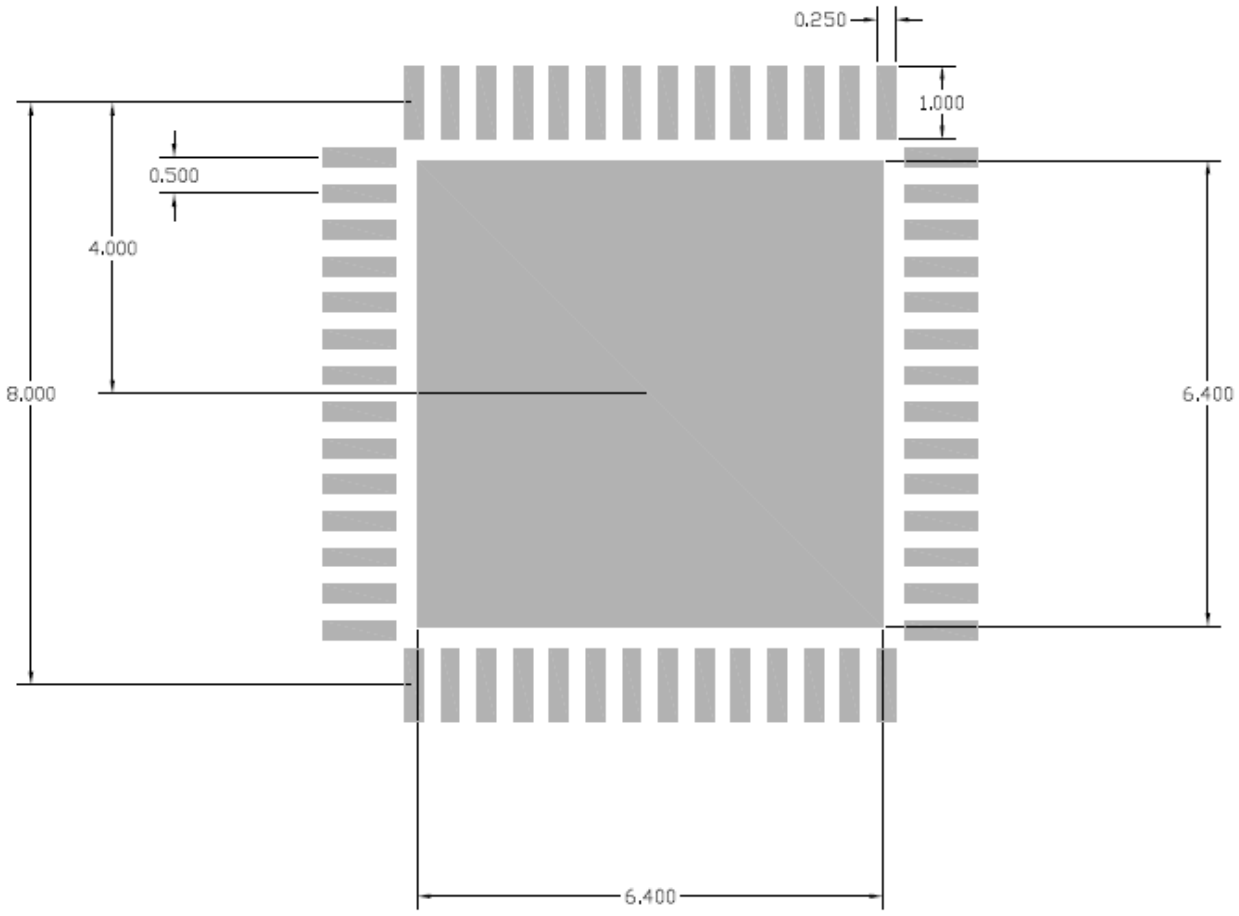


Figure 52: PCB Decal

The PCB schematic and layout rules detailed in Appendix B.4 must be followed. Failure to do so will likely result in the JN5148 failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.

A.3 Ordering Information

The standard qualification for the JN5148 is Industrial temperature range: -40ºC to +85ºC, packaged in a 56-pin QFN package.

Ordering Code Format:

JN5148/XXX

XXX: ROM Variant

001 Supports all available networking stacks

Ordering Codes:

Part Number	Ordering Code	Description
JN5148-001	JN5148/001	JN5148 microcontroller

The chip is available in three different reel quantities:

- 500 on 180mm reel
- 1000 on 180mm reel
- 2500 on 330mm reel

Where this Data Sheet is denoted as “Advanced” or “Preliminary”, devices will be either Engineering Samples or Prototypes. Devices of this status are marked with an Rx suffix after the ROM identifier to identify the revision of silicon during these product phases - for example JN5148-001**R1**-T.

The Standard Supply Multiple (SSM) for Engineering Samples or Prototypes is 50 units with a maximum of 250 units. If the quantity of Engineering Samples or Prototypes ordered is less than a reel quantity, then these will be shipped in tape form only, with no reel and will not be dry packaged in a moisture sensitive environment.

The SSM for Production status devices is one reel, all reels are dry packaged in a moisture sensitive bag see A.5.3.

A.5.2 Reel Information: 180mm Reel

Surface Resistivity	Between $10e^{9}$ – $10e^{11}$ Ohms Square
Material	High Impact Polystyrene, environmentally friendly, recyclable

All dimensions and tolerances are fully compliant with EIA-481-B and are specified in millimetres.

6 window design with one window on each side blanked to allow adequate labelling space.

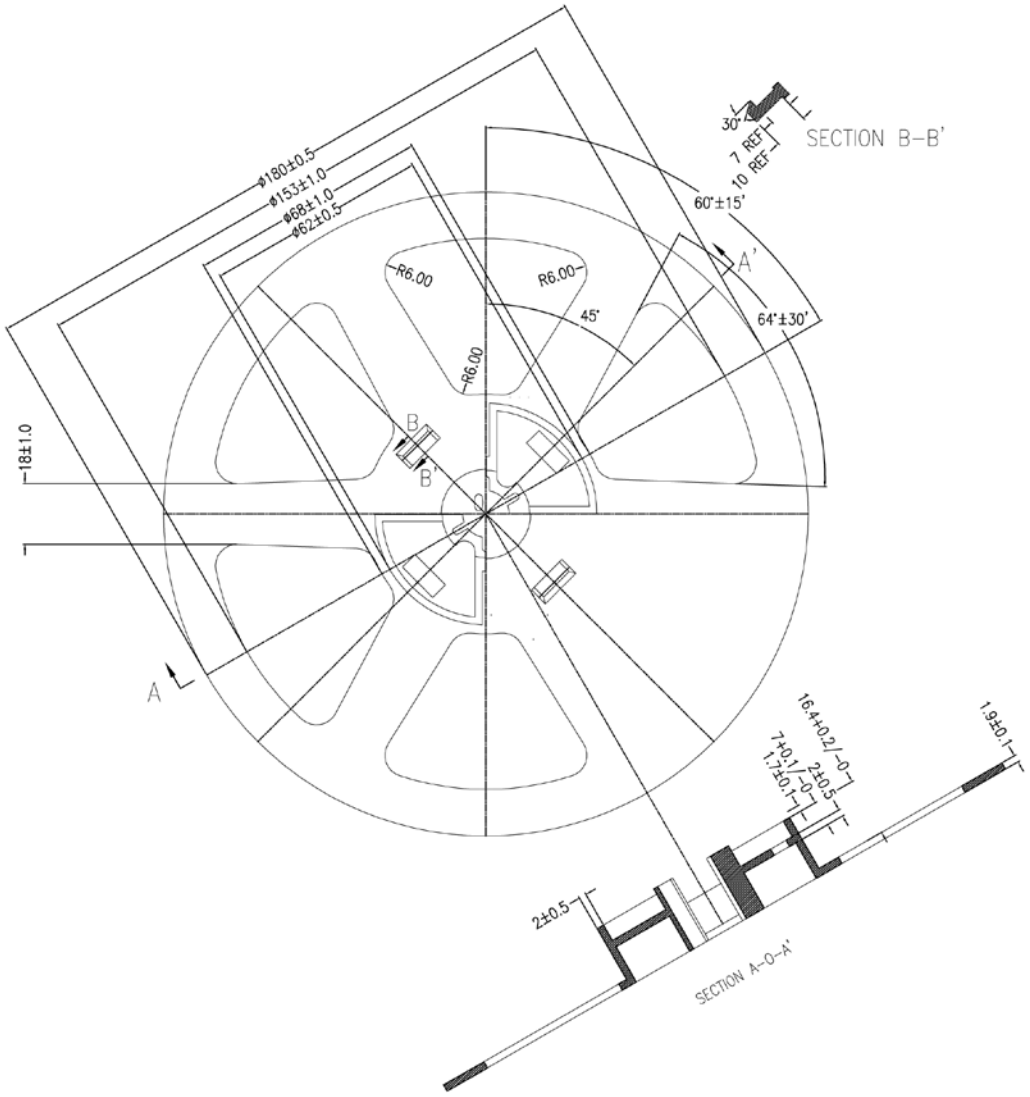


Figure 56: 180mm Reel Dimensions

Component Designator	Value/Type	Function	PCB Layout Constraints
C13	10uF	Power source decoupling	
C14	100nF	Analogue Power decoupling	Adjacent to U1 pin 13
C16	100nF	Digital power decoupling	Adjacent to U1 pin 49
C15	100nF	VB Synth decoupling	Less than 5mm from U1 pin 10
C18	47pF	VB Synth decoupling	Less than 5mm from U1 pin 10
C2	10nF	VB VCO decoupling	Less than 5mm from U1 pin 12
C24	47pF	VB VCO decoupling	Less than 5mm from U1 pin 12
C3	100nF	VB RF decoupling	Less than 5mm from U1 pin 16 and U1 pin 18
C12	47pF	VB RF decoupling	Less than 5mm from U1 pin 16 and U1 pin 18
C8	100nF	VB A decoupling	Less than 5mm from U1 pin 27
C9	47pF	VB A decoupling	Less than 5mm from U1 pin 27
C6	100nF	VB RAM decoupling	Less than 5mm from U1 pin 35
C7	100nF	VB Dig decoupling	Less than 5mm from U1 pin 40
R1	43k	I Bias Resistor	Less than 5mm from U1 pin 14
C20	100nF	Vref decoupling	Less than 5mm from U1 pin 15
U2	4Mbit	Serial Flash Memory (Numonyx M25P40)	
Y1	32MHz	Crystal (AEL X32M000000S025) (CL = 9pF, Max ESR 40R)	
C10	15pF +/-5% COG	Crystal Load Capacitor	Adjacent to pin 8 and Y1 pin 1
C11	15pF +/-5% COG	Crystal Load Capacitor	Adjacent to pin 9 and Y1 pin 3
R2			Not fitted
C1	47pF	AC Coupling Phycomp 2238-869-15479	Must be copied directly from the reference design.
L1	5.6nH	RF Matching Inductor MuRata LQP15MN5N6B02	
L2	2.7nH	Load Inductor MuRata LQP15MN2N7B02	

Table 8: JN5148 Printed Antenna Reference Module Components and PCB Layout Constraints

The paddle should be connected directly to ground. Any pads that requiring connection to ground should do so by connecting directly to the paddle.

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