Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	80KB (80K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3212a-40u6

2.8 Addressing modes

The addressing modes in UPSD321xx devices instruction set are as follows

1. Direct addressing
2. Indirect addressing
3. Register addressing
4. Register-specific addressing
5. Immediate constants addressing
6. Indexed addressing

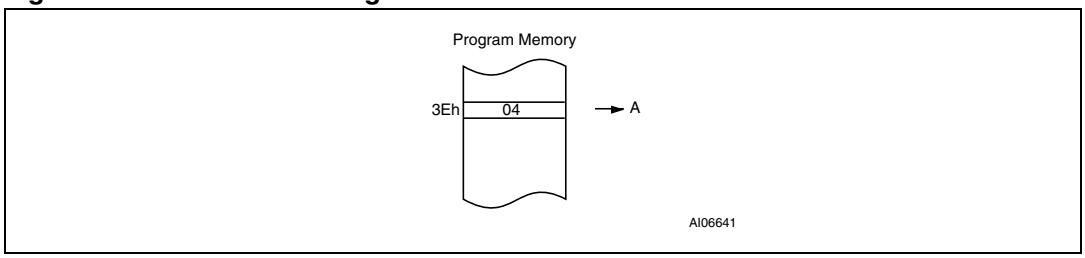
2.8.1 Direct addressing

In a direct addressing the operand is specified by an 8-bit address field in the instruction. Only internal Data RAM and SFRs (80~FFH RAM) can be directly addressed.

Example:

mov A, 3EH ; A <----- RAM[3E]

Figure 10. Direct addressing



2.8.2 Indirect addressing

In indirect addressing the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed. The address register for 8-bit addresses can be R0 or R1 of the selected register bank, or the Stack Pointer. The address register for 16-bit addresses can only be the 16-bit “data pointer” register, DPTR.

Example:

mov @R1, #40 H ;[R1] <-----40H

Figure 11. Indirect addressing

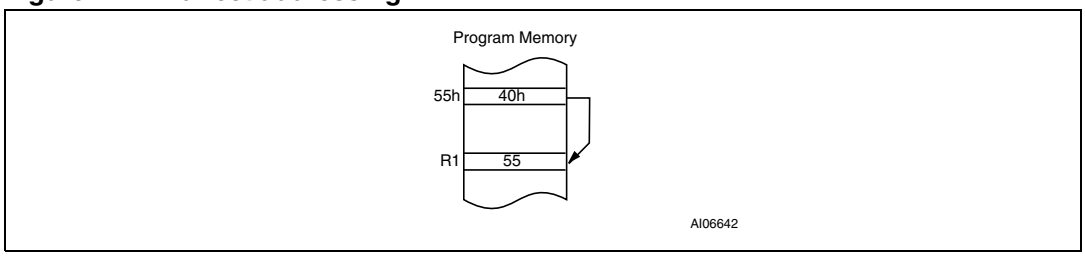


Table 8. Shifting a BCD number 2 digits to the right (using direct XCHs: 9 bytes)

		2A	2B	2C	2D	2E	ACC
CLR	A	00	12	34	56	78	00
XCH	A,2Bh	00	00	34	56	78	12
XCH	A,2Ch	00	00	12	56	78	34
XCH	A,2Dh	00	00	12	34	78	56
XCH	A,2Eh	00	00	12	34	56	78

Table 9. Shifting a BCD number one digit to the right

			2A	2B	2C	2D	2E	ACC
	MOV	R1,#2Eh	00	12	34	56	78	xx
	MOV	R0,#2Dh	00	12	34	56	78	xx
	; loop for R1 = 2Eh							
LOOP:	MOV	A,@R1	00	12	34	56	78	78
	XCHD	A,@R0	00	12	34	58	78	76
	SWAP	A	00	12	34	58	78	67
	MOV	@R1,A	00	12	34	58	67	67
	DEC	R1	00	12	34	58	67	67
	DEC	R0	00	12	34	58	67	67
	CNJE	R1,#2Ah,LOOP	00	12	34	58	67	67
	; loop for R1 = 2Dh		00	12	38	45	67	45
	; loop for R1 = 2Ch		00	18	23	45	67	23
	; loop for R1 = 2Bh		08	01	23	45	67	01
	CLR	A	08	01	23	45	67	00
	XCH	A,2Ah	00	01	23	45	67	08

2.11.2 External RAM

Table 10 shows a list of the Data Transfer instructions that access external Data Memory. Only indirect addressing can be used. The choice is whether to use a one-byte address, @Ri, where Ri can be either R0 or R1 of the selected register bank, or a two-byte address, @DTPR.

Note: In all external Data RAM accesses, the Accumulator is always either the destination or source of the data.

Table 12. Boolean instructions

Mnemonic	Operation
ANL C,bit	C = A .AND. bit
ANL C,/bit	C = C .AND. .NOT. bit
ORL C,bit	C = A .OR. bit
ORL C,/bit	C = C .OR. .NOT. bit
MOV C,bit	C = bit
MOV bit,C	bit = C
CLR C	C = 0
CLR bit	bit = 0
SETB C	C = 1
SETB bit	bit = 1
CPL C	C = .NOT. C
CPL bit	bit = .NOT. bit
JC rel	Jump if C =1
JNC rel	Jump if C = 0
JB bit,rel	Jump if bit =1
JNB bit,rel	Jump if bit = 0
JBC bit,rel	Jump if bit = 1; CLR bit

2.13 Relative offset

The destination address for these jumps is specified to the assembler by a label or by an actual address in Program memory. However, the destination address assembles to a relative offset byte. This is a signed (two's complement) offset byte which is added to the PC in two's complement arithmetic if the jump is executed.

The range of the jump is therefore -128 to +127 Program Memory bytes relative to the first byte following the instruction.

2.14 Jump instructions

Table 13 shows the list of unconditional jump instructions. The table lists a single "JMP add" instruction, but in fact there are three SJMP, LJMP, and AJMP, which differ in the format of the destination address. JMP is a generic mnemonic which can be used if the programmer does not care which way the jump is en-coded.

The SJMP instruction encodes the destination address as a relative offset, as described above. The instruction is 2 bytes long, consisting of the opcode and the relative offset byte. The jump distance is limited to a range of -128 to +127 bytes relative to the instruction following the SJMP.

2.15 Machine cycles

A machine cycle consists of a sequence of six states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus, a machine cycle takes 12 oscillator periods or 1µs if the oscillator frequency is 12MHz. Refer to *Table 13: State sequence in UPSD321xx devices*.

Each state is divided into a Phase 1 half and a Phase 2 half. State Sequence in UPSD321xx devices shows that retrieve/execute sequences in states and phases for various kinds of instructions.

Normally two program retrievals are generated during each machine cycle, even if the instruction being executed does *not* require it. If the instruction being executed does not need more code bytes, the CPU simply ignores the extra retrieval, and the Program Counter is not incremented.

Execution of a one-cycle instruction (*Figure 13: State sequence in UPSD321xx devices*) begins during State 1 of the machine cycle, when the opcode is latched into the Instruction Register. A second retrieve occurs during S4 of the same machine cycle. Execution is complete at the end of State 6 of this machine cycle.

The MOVX instructions take two machine cycles to execute. No program retrieval is generated during the second cycle of a MOVX instruction. This is the only time program retrievals are skipped. The retrieve/execute sequence for MOVX instruction is shown in *Figure 13* (d).

Table 14. Conditional jump instructions

Mnemonic	Operation	Addressing modes			
		Dir.	Ind.	Reg.	Imm.
JZ rel	Jump if A = 0	Accumulator only			
JNZ rel	Jump if A ≠ 0	Accumulator only			
DJNZ <byte>,rel	Decrement and jump if not zero	X		X	
CJNE A,<byte>,rel	Jump if A ≠ <byte>	X			X
CJNE <byte>,#data,rel	Jump if <byte> ≠ #data		X	X	

Table 16. List of all SFRs (continued)

SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
A1	PWMCON	PWML	PWMP	PWME	CFG4	CFG3	CFG2	CFG1	CFG0	00	PWM Control Polarity
A2	PWM0									00	PWM0 Output Duty Cycle
A3	PWM1									00	PWM1 Output Duty Cycle
A4	PWM2									00	PWM2 Output Duty Cycle
A5	PWM3									00	PWM3 Output Duty Cycle
A6	WDRST									00	Watch Dog Reset
A7	IEA				ES2			EI^{2}C		00	Interrupt Enable (2nd)
A8	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0	00	Interrupt Enable
A9											
AA	PWM4P									00	PWM 4 Period
AB	PWM4W									00	PWM 4 Pulse Width
AE	WDKEY									00	Watch Dog Key Register
B0	P3									FF	Port 3
B1	PSCL0L									00	Prescaler 0 Low (8-bit)
B2	PSCL0H									00	Prescaler 0 High (8-bit)
B3	PSCL1L									00	Prescaler 1 Low (8-bit)
B4	PSCL1H									00	Prescaler 1 High (8-bit)
B7	IPA				PS2			PI2C		00	Interrupt Priority (2nd)
B8	IP			PT2	PS	PT1	PX1	PT0	PX0	00	Interrupt Priority
C0	P4									FF	New Port 4
C8	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00	Timer 2 Control

Table 16. List of all SFRs (continued)

SFR Addr	Reg Name	Bit Register Name								Reset Value	Comments
		7	6	5	4	3	2	1	0		
EF	UDR0	UDR0.7	UDR0.6	UDR0.5	UDR0.4	UDR0.3	UDR0.2	UDR0.1	UDR0.0	00	USB Endpt0 Data Recv
F0	B									00	B Register

Table 17. PSD module register address offset

CSIOP addr offset	Register name	Bit register name								Reset value	Comments
		7	6	5	4	3	2	1	0		
00	Data In (Port A)	Reads Port pins as input									
02	Control (Port A)	Configure pin between I/O or Address Out mode. Bit = 0 selects I/O								00	
04	Data Out (Port A)	Latched data for output to Port pins, I/O Output mode								00	
06	Direction (Port A)	Configures Port pin as input or output. Bit = 0 selects input								00	
08	Drive (Port A)	Configures Port pin between CMOS, Open Drain or Slew rate. Bit = 0 selects CMOS								00	
0A	Input Macrocell (Port A)	Reads latched value on Input Macrocells									
0C	Enable Out (Port A)	Reads the status of the output enable control to the Port pin driver. Bit = 0 indicates pin is in input mode.									
01	Data In (Port B)										
03	Control (Port B)									00	
05	Data Out (Port B)									00	
07	Direction (Port B)									00	
09	Drive (Port B)									00	
0B	Input Macrocell (Port B)										
0D	Enable Out (Port B)										
10	Data In (Port C)										
12	Data Out (Port C)									00	
14	Direction (Port C)									00	
16	Drive (Port C)									00	
18	Input Macrocell (Port C)										

Table 21. Description of the IEA bits

Bit	Symbol	Function
7	—	Not used
6	—	Not used
5	—	Not used
4	ES2	Enable 2nd USART Interrupt
3	—	Not used
2	—	Not used
1	EI2C	Enable I²C Interrupt
0	EUSB	Enable USB Interrupt

Table 22. Description of the IP bits

Bit	Symbol	Function
7	—	Reserved
6	—	Reserved
5	PT2	Timer 2 Interrupt priority level
4	PS	USART Interrupt priority level
3	PT1	Timer 1 Interrupt priority level
2	PX1	External Interrupt (Int1) priority level
1	PT0	Timer 0 Interrupt priority level
0	PX0	External Interrupt (Int0) priority level

Table 23. Description of the IPA bits

Bit	Symbol	Function
7	—	Not used
6	—	Not used
5	—	Not used
4	PS2	2nd USART Interrupt priority level
3	—	Not used
2	—	Not used
1	PI2C	I²C Interrupt priority level
0	PUSB	USB Interrupt priority level

7 I/O ports (MCU module)

The MCU module has five ports: Port 0, Port 1, Port 2, Port 3, and Port 4. (Refer to the PSD module section on I/O ports A,B,C and D). Ports P0 and P2 are dedicated for the external address and data bus and is not available in the 52-pin package devices.

Port 1- Port 3 are the same as in the standard 8032 microcontrollers, with the exception of the additional special peripheral functions. All ports are bi-directional. Pins of which the alternative function is not used may be used as normal bi-directional I/O.

The use of Port 1-Port 4 pins as alternative functions are carried out automatically by the UPSD321xx devices provided the associated SFR Bit is set HIGH.

The following SFR registers (*Table 29*, *Table 30*, and *Table 31*) are used to control the mapping of alternate functions onto the I/O port bits. Port 1 alternate functions are controlled using the P1SFS register, except for Timer 2 and the 2nd UART which are enabled by their configuration registers. P1.0 to P1.3 are default to GPIO after reset.

Port 3 pins 6 and 7 have been modified from the standard 8032. These pins that were used for READ and WRITE control signals are now GPIO or I^2C bus pins. The READ and WRITE pins are assigned to dedicated pins.

Port 3 (I^2C) and Port 4 alternate functions are controlled using the P3SFS and P4SFS Special Function Selection registers. After a reset, the I/O pins default to GPIO. The alternate function is enabled if the corresponding bit in the PXSFS register is set to '1.' Other Port 3 alternative functions (UART, Interrupt, and Timer/Counter) are enabled by their configuration register and do not require setting of the bits in P3SFS.

Table 28. I/O port functions

Port name	Main function	Alternate
Port 1	GPIO	Timer 2 - Bits 0,1 2nd UART - Bits 2,3 ADC - Bits 4..7
Port 3	GPIO	UART - Bits 0,1 Interrupt - Bits 2,3 Timers - Bits 4,5 I^2C - Bits 6,7
Port 4	GPIO	PWM - Bits 3..7
USB +/-	USB +/- Only	

Table 29. P1SFS (91h)

7	6	5	4	3	2	1	0
0=Port 1.7 1=ACH3	0=Port 1.6 1=ACH2	0=Port 1.5 1=ACH1	0=Port 1.4 1=ACH0	Bits are reserved		Bits are reserved	

Table 49. PWM SFR memory map (continued)

SFR addr	Reg name	Bit register name								Reset value	Comments
		7	6	5	4	3	2	1	0		
B2	PSCL0H									00	Prescaler 0 High (8-bit)
B3	PSCL1L									00	Prescaler 1 Low (8-bit)
B4	PSCL1H									00	Prescaler 1 High (8-bit)

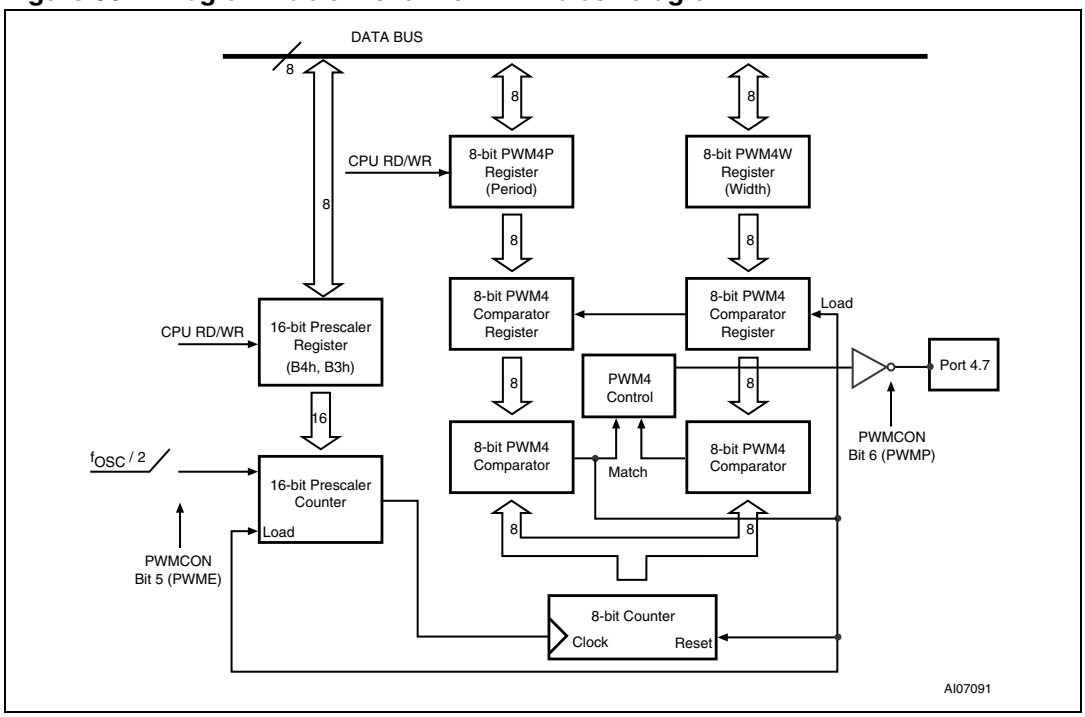
PWMCON register bit definition:

- PWML = PWM 0-3 polarity control
- PWMP = PWM 4 polarity control
- PWME = PWM enable (0 = disabled, 1= enabled)
- CFG3..CFG0 = PWM 0-3 Output (0 = Open Drain; 1 = Push-Pull)
- CFG4 = PWM 4 Output (0 = Open Drain; 1 = Push-Pull)

14.2 Programmable period 8-bit PWM

The PWM 4 channel can be programmed to provide a PWM output with variable pulse width and period. The PWM 4 has a 16-bit Prescaler, an 8-bit Counter, a Pulse Width Register, and a Period Register. The Pulse Width Register defines the PWM pulse width time, while the Period Register defines the period of the PWM. The input clock to the Prescaler is $f_{OSC}/2$. The PWM 4 channel is assigned to Port 4.7.

Figure 36. Programmable 4-channel PWM block diagram



15.1 Serial status register (SxSTA: S1STA, S2STA)

SxSTA is a “Read-only” register. The contents of this register may be used as a vector to a service routine. This optimized the response time of the software and consequently that of the I²C-bus. The status codes for all possible modes of the I²C-bus interface are given Table *Table 54*.

This flag is set, and an interrupt is generated, after any of the following events occur.

1. Own slave address has been received during AA = 1: ack_int
2. The general call address has been received while GC(SxADR.0) = 1 and AA = 1:
3. A data byte has been received or transmitted in Master mode (even if arbitration is lost): ack_int
4. A data byte has been received or transmitted as selected slave: ack_int
5. A stop condition is received as selected slave receiver or transmitter: stop_int

15.2 Data shift register (SxDAT: S1DAT, S2DAT)

SxDAT contains the serial data to be transmitted or data which has just been received. The MSB (Bit 7) is transmitted or received first; that is, data shifted from right to left.

Table 53. Serial status register (SxSTA)

7	6	5	4	3	2	1	0
GC	STOP	INTR	TX_MODE	BBUSY	BLOST	/ACK_REP	SLV

Table 54. Description of the SxSTA bits

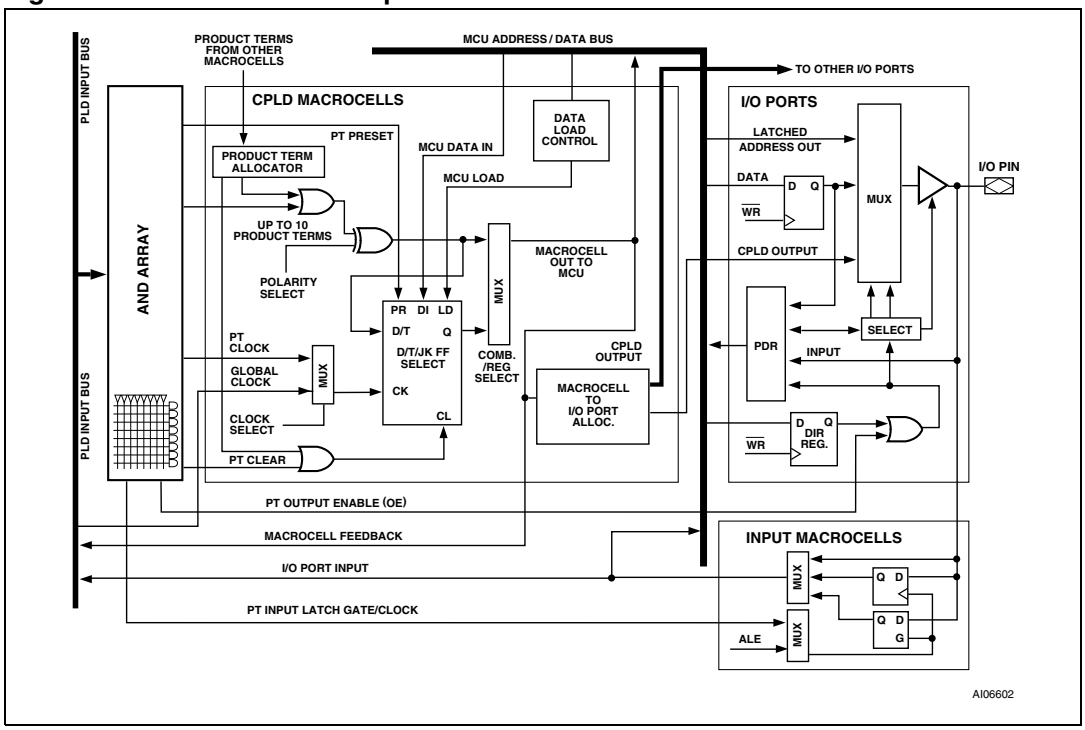
Bit	Symbol	Function
7	GC	General Call Flag
6	STOP	Stop Flag. This bit is set when a STOP condition is received
5	INTR(1,2)	Interrupt Flag. This bit is set when an I²C Interrupt condition is requested
4	TX_MODE	Transmission mode Flag. This bit is set when the I²C is a transmitter; otherwise this bit is reset
3	BBUSY	Bus Busy Flag. This bit is set when the bus is being used by another master; otherwise, this bit is reset
2	BLOST	Bus Lost Flag. This bit is set when the master loses the bus contention; otherwise this bit is reset
1	/ACK_REP	Acknowledge Response Flag. This bit is set when the receiver transmits the not acknowledge signal This bit is reset when the receiver transmits the acknowledge signal
0	SLV	Slave mode Flag. This bit is set when the I²C plays role in the Slave mode; otherwise this bit is reset

1. Interrupt Flag bit (INTR, SxSTA Bit 5) is cleared by Hardware as reading SxSTA register.
2. I²C interrupt flag (INTR) can occur in below case. (except DDC2B mode at SWENB=0)

The Input Macrocells (IMC) and Output Macrocells (OMC) are connected to the PSD module internal data bus and can be directly accessed by the MCU. This enables the MCU software to load data into the Output Macrocells (OMC) or read data from both the Input and Output Macrocells (IMC and OMC).

This feature allows efficient implementation of system logic and eliminates the need to connect the data bus to the AND Array as required in most standard PLD macrocell architectures.

Figure 54. Macrocell and I/O ports



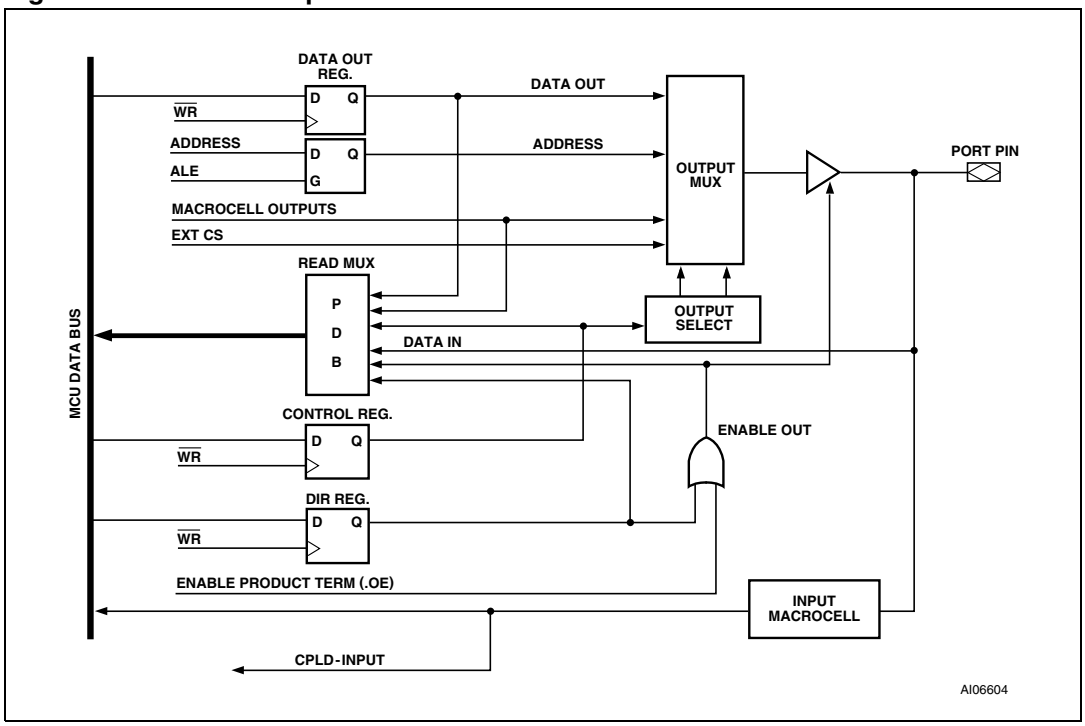
22.4 Output macrocell (OMC)

Eight of the Output Macrocells (OMC) are connected to Ports A and B pins and are named as McellAB0-McellAB7. The other eight macrocells are connected to Ports B and C pins and are named as McellBC0-McellBC7. If an McellAB output is not assigned to a specific pin in PSDsoft, the Macrocell Allocator block assigns it to either Port A or B. The same is true for a McellBC output on Port B or C. *Table 89* shows the macrocells and port assignment.

The Output Macrocell (OMC) architecture is shown in *Figure 55*. As shown in the figure, there are native product terms available from the AND Array, and borrowed product terms available (if unused) from other Output Macrocells (OMC). The polarity of the product term is controlled by the XOR gate. The Output Macrocell (OMC) can implement either sequential logic, using the flip-flop element, or combinatorial logic. The multiplexer selects between the sequential or combinatorial logic outputs. The multiplexer output can drive a port pin and has a feedback path to the AND Array inputs.

The flip-flop in the Output Macrocell (OMC) block can be configured as a D, T, JK, or SR type in PSDsoft. The flip-flop's clock, preset, and clear inputs may be driven from a product term of the AND Array. Alternatively, CLKIN (PD1) can be used for the clock input to the flip-

Figure 57. General I/O port architecture



The Port pin's tri-state output driver enable is controlled by a two input OR gate whose inputs come from the CPLD AND Array enable product term and the Direction Register. If the enable product term of any of the Array outputs are not defined and that port pin is not defined as a CPLD output in the PSDsoft, then the Direction Register has sole control of the buffer that drives the port pin.

The contents of these registers can be altered by the MCU. The Port Data Buffer (PDB) feedback path allows the MCU to check the contents of the registers.

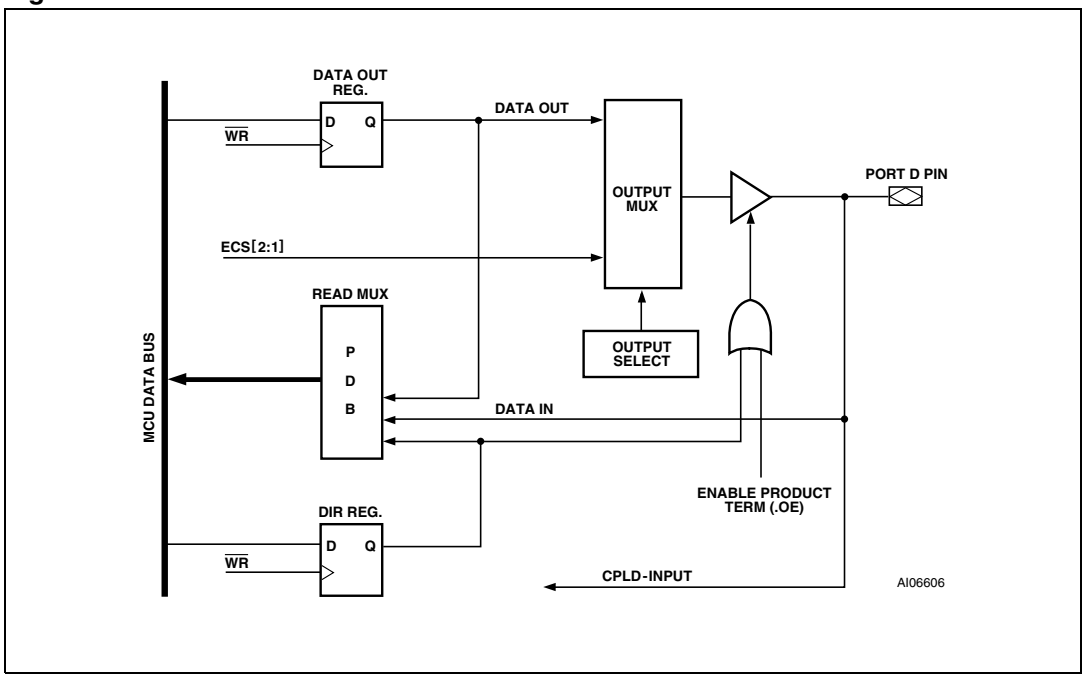
Ports A, B, and C have embedded Input Macrocells (IMC). The Input Macrocells (IMC) can be configured as latches, registers, or direct inputs to the PLDs. The latches and registers are clocked by Address Strobe (ALE) or a product term from the PLD AND Array. The outputs from the Input Macrocells (IMC) drive the PLD input bus and can be read by the MCU. See *Figure 56*.

23.2 Port operating modes

The I/O Ports have several modes of operation. Some modes can be defined using PSDsoft, some by the MCU writing to the Control Registers in CSIOP space, and some by both. The modes that can only be defined using PSDsoft must be programmed into the device and cannot be changed unless the device is reprogrammed. The modes that can be changed by the MCU can be done so dynamically at run-time. The PLD I/O, Data Port, Address Input, and Peripheral I/O modes are the only modes that must be defined before programming the device. All other modes can be changed by the MCU at run-time. See Application Note *AN1171* for more detail.

Table 90 summarizes which modes are available on each port. *Table 93* shows how and where the different modes are configured. Each of the port operating modes are described in the following sections.

Figure 61. Port D structure



23.13 External chip select

The CPLD also provides two External Chip Select (ECS1-ECS2) outputs on Port D pins that can be used to select external devices. Each External Chip Select (ECS1-ECS2) consists of one product term that can be configured active High or Low. The output enable of the pin is controlled by either the output enable product term or the Direction register. (See *Figure 62*.)

Table 120. External clock drive (with the 3 V MCU module)

Symbol	Parameter[1]	24 MHz oscillator		Variable oscillator 1/t_{CLCL} = 8 to 24 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	Oscillator period			41.7	125	ns
t_{WLWH}	High time			12	$t_{CLCL} - t_{CLCX}$	ns
t_{LLAX2}	Low time			12	$t_{CLCL} - t_{CLCX}$	ns
t_{RHDX}	Rise time				12	ns
t_{RHDX}	Fall time				12	ns

1. Conditions (in addition to those in *Table 111*, V_{CC} = 3.0 to 3.6 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF, for 5 V devices, and 50 pF for 3 V devices; C_L for other outputs is 80 pF, for 5 V devices, and 50 pF for 3 V devices)

Figure 70. External data memory Read cycle

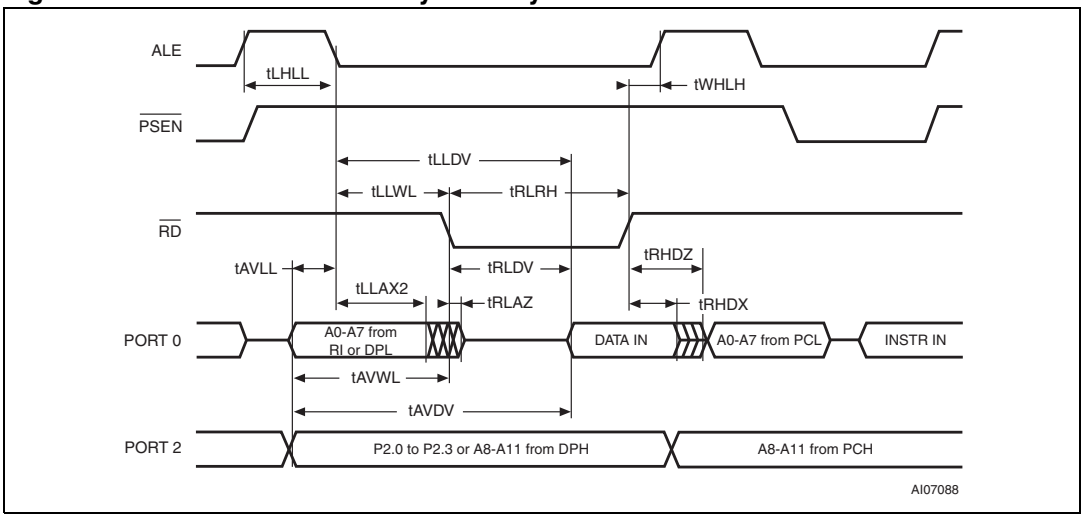


Figure 71. External data memory Write cycle

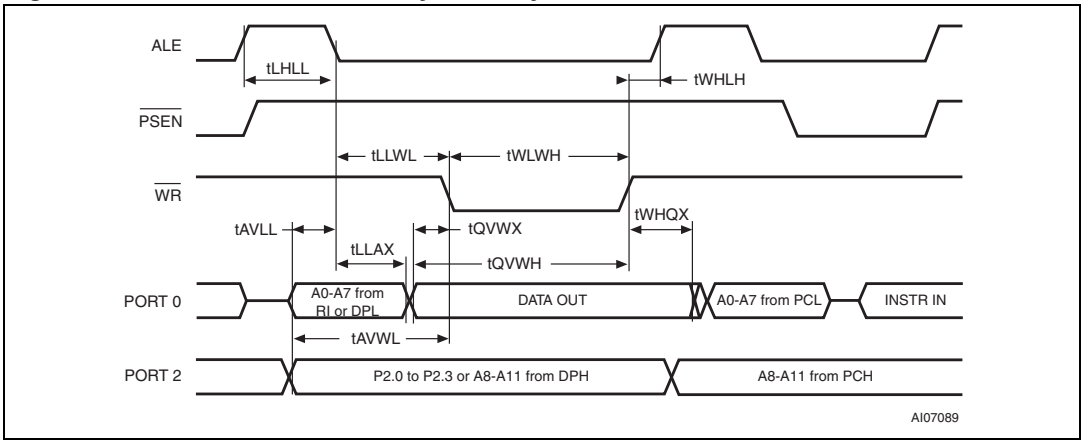


Table 122. External data memory AC characteristics (with the 3 V MCU module)

Symbol	Parameter[1]	24 MHz oscillator		Variable oscillator $1/t_{CLCL}$ = 8 to 24 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{RLRH}	$\overline{RD}$ pulse width	180		6 t_{CLCL} – 70		ns
t_{WLWH}	$\overline{WR}$ pulse width	180		6 t_{CLCL} – 70		ns
t_{LLAX2}	Address hold after ALE	56		2 t_{CLCL} – 27		ns
t_{RHDX}	$\overline{RD}$ to valid data in		118		5 t_{CLCL} – 90	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		63		2 t_{CLCL} – 20	ns
t_{LLDV}	ALE to valid data in		200		8 t_{CLCL} – 133	ns
t_{AVDV}	Address to valid data in		220		9 t_{CLCL} – 155	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	75	175	3 t_{CLCL} – 50	t_{CLCL} + 50	ns
t_{AVWL}	Address valid to $\overline{WR}$ or $\overline{RD}$	67		4 t_{CLCL} – 97		ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ High to ALE High	17	67	t_{CLCL} – 25	t_{CLCL} + 25	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5		t_{CLCL} – 37		ns
t_{QVWH}	Data set-up before $\overline{WR}$	170		7 t_{CLCL} – 122		ns
t_{WHQX}	Data hold after $\overline{WR}$	15		t_{CLCL} – 27		ns
t_{RLAZ}	Address float after $\overline{RD}$		0		0	ns

1. Conditions (in addition to those in *Table 111*, V_{CC} = 3.0 to 3.6 V): V_{SS} = 0 V; C_L for Port 0, ALE and PSEN output is 100 pF, for 5 V devices, and 50 pF for 3 V devices; C_L for other outputs is 80 pF, for 5 V devices, and 50 pF for 3 V devices)

Table 123. A/D analog specification

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
AV_{REF}	Analog power supply input voltage range		V_{SS}		V_{CC}	V
V_{AN}	Analog input voltage range		V_{SS} – 0.3		AV_{REF} + 0.3	V
I_{AVDD}	Current following between V_{CC} and V_{SS}				200	µA
CA_{IN}	Overall accuracy				±2	l.s.b.
N_{NLE}	Non-linearity error				±2	l.s.b.
N_{DNLE}	Differential non-linearity error				±2	l.s.b.
N_{ZOE}	Zero-offset error				±2	l.s.b.
N_{FSE}	Full scale error				±2	l.s.b.
N_{GE}	Gain error				±2	l.s.b.
t_{CONV}	Conversion time	at 8 MHz clock			20	µs

Table 140. ISC timing (5 V devices)

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{ISCCF}	Clock (TCK, PC1) frequency (except for PLD)	(Note 1)		20	MHz
t_{ISCCH}	Clock (TCK, PC1) high time (except for PLD)	(Note 1)	23		ns
t_{ISCCL}	Clock (TCK, PC1) low time (except for PLD)	(Note 1)	23		ns
t_{ISCCFP}	Clock (TCK, PC1) frequency (PLD only)	(Note 2)		2	MHz
t_{ISCCHP}	Clock (TCK, PC1) high time (PLD only)	(Note 2)	240		ns
t_{ISCCLP}	Clock (TCK, PC1) low time (PLD only)	(Note 2)	240		ns
t_{ISCPSU}	ISC port set-up time		7		ns
t_{ISCPH}	ISC port hold-up time		5		ns
t_{ISCPCO}	ISC port clock to output			21	ns
t_{ISCPZV}	ISC port high-impedance to valid output			21	ns
t_{ISCPVZ}	ISC port valid output to high-impedance			21	ns

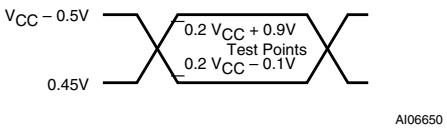
1. For non-PLD Programming, Erase or in ISC By-pass mode.
2. For Program or Erase PLD only.

Table 141. ISC timing (3 V devices)

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{ISCCF}	Clock (TCK, PC1) frequency (except for PLD)	(Note 1)		12	MHz
t_{ISCCH}	Clock (TCK, PC1) high time (except for PLD)	(Note 1)	40		ns
t_{ISCCL}	Clock (TCK, PC1) low time (except for PLD)	(Note 1)	40		ns
t_{ISCCFP}	Clock (TCK, PC1) frequency (PLD only)	(Note 2)		2	MHz
t_{ISCCHP}	Clock (TCK, PC1) high time (PLD only)	(Note 2)	240		ns
t_{ISCCLP}	Clock (TCK, PC1) low time (PLD only)	(Note 2)	240		ns
t_{ISCPSU}	ISC port set-up time		12		ns
t_{ISCPH}	ISC port hold-up time		5		ns
t_{ISCPCO}	ISC port clock to output			30	ns
t_{ISCPZV}	ISC port high-impedance to valid output			30	ns
t_{ISCPVZ}	ISC port valid output to high-impedance			30	ns

1. For non-PLD Programming, Erase or in ISC By-pass mode.
2. For Program or Erase PLD only.

Figure 81. MCU module AC measurement I/O waveform



1. AC inputs during testing are driven at V_{CC}–0.5 V for a logic '1,' and 0.45 V for a logic '0.'
2. Timing measurements are made at V_{IH}(min) for a logic '1,' and V_{IL}(max) for a logic '0'.

Figure 86. PSD module AC measurement load circuit

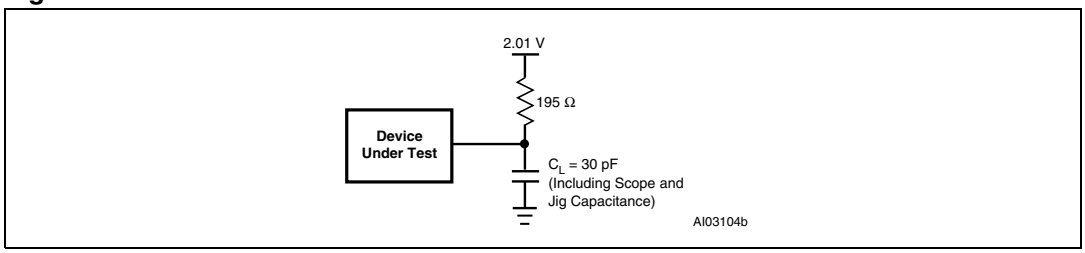
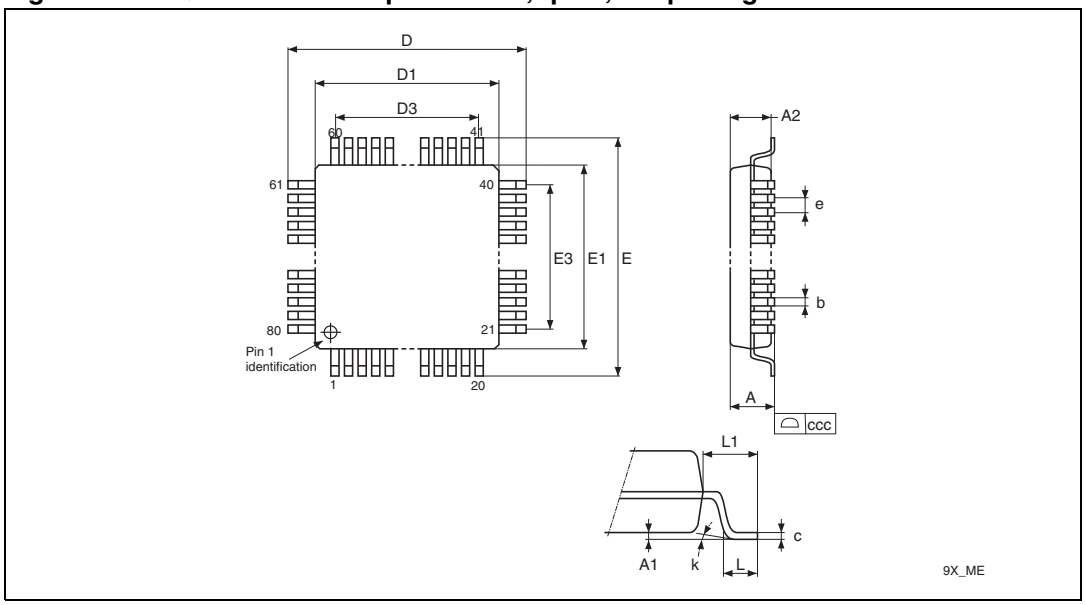


Table 142. Capacitance

Symbol	Parameter	Test conditions (1)	Typ.(2)	Max.	Unit
C_{IN}	Input capacitance (for input pins)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Output capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF

1. Sampled only, not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 88. LQFP80 – 80-lead plastic thin, quad, flat package outline



1. Drawing is not to scale.

Table 144. LQFP80 – 80-lead plastic thin, quad, flat package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.090	0.200		0.0035	0.0079
D	14.000			0.5512		
D1	12.000			0.4724		
D3	9.500			0.3740		
E	14.000			0.5512		
E1	12.000			0.4724		
E3	9.500			0.3740		
e	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k		0°	7°		0°	7°
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com