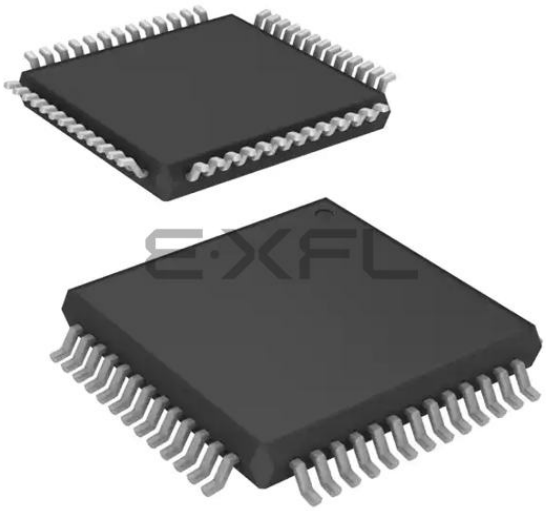

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8032
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	80KB (80K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/upsd3212c-40t6

Contents

Table 2. 80-pin package pin description (continued)

Port pin	Signal name	Pin no.	In/ out	Function	
				Basic	Alternate
P4.7	PWM4	18	I/O	General I/O port pin	Programmable 8-bit Pulse Width modulation output 4
	USB–	8	I/O	Pull-up resistor required (2 kΩ for 3 V devices, 7.5 kΩ for 5 V devices)	
	V_{REF}	70	O	Reference Voltage input for ADC	
	RD_	65	O	READ signal, external bus	
	WR_	62	O	WRITE signal, external bus	
	PSEN_	63	O	$\overline{PSEN}$ signal, external bus	
	ALE	4	O	Address Latch signal, external bus	
	RESET_	68	I	Active low $\overline{RESET}$ input	
	XTAL1	48	I	Oscillator input pin for system clock	
	XTAL2	49	O	Oscillator output pin for system clock	
PA0		35	I/O	General I/O port pin	PLD macrocell outputs PLD inputs Latched address out (A0-A7) Peripheral I/O mode
PA1		34	I/O	General I/O port pin	
PA2		32	I/O	General I/O port pin	
PA3		28	I/O	General I/O port pin	
PA4		26	I/O	General I/O port pin	
PA5		24	I/O	General I/O port pin	
PA6		22	I/O	General I/O port pin	
PA7		21	I/O	General I/O port pin	
PB0		80	I/O	General I/O port pin	PLD macrocell outputs PLD inputs Latched address out (A0-A7)
PB1		78	I/O	General I/O port pin	
PB2		76	I/O	General I/O port pin	
PB3		74	I/O	General I/O port pin	
PB4		73	I/O	General I/O port pin	
PB5		72	I/O	General I/O port pin	
PB6		67	I/O	General I/O port pin	
PB7		66	I/O	General I/O port pin	

2.8.3 Register addressing

The register banks, containing registers R0 through R7, can be accessed by certain instructions which carry a 3-bit register specification within the opcode of the instruction. Instructions that access the registers this way are code efficient, since this mode eliminates an address byte. When the instruction is executed, one of four banks is selected at execution time by the two bank select bits in the PSW.

Example:

```
mov PSW, #0001000B ; select Bank0
mov A, #30H
mov R1, A
```

2.8.4 Register-specific addressing

Some instructions are specific to a certain register. For example, some instructions always operate on the Accumulator, or Data Pointer, etc., so no address byte is needed to point it. The opcode itself does that.

2.8.5 Immediate constants addressing

The value of a constant can follow the opcode in Program memory.

Example:

```
mov A, #10H.
```

2.8.6 Indexed addressing

Only Program memory can be accessed with indexed addressing, and it can only be read. This addressing mode is intended for reading look-up tables in Program memory. A 16-bit base register (either DPTR or PC) points to the base of the table, and the Accumulator is set up with the table entry number. The address of the table entry in Program memory is formed by adding the Accumulator data to the base pointer.

Example:

```
movc A, @A+DPTR
```

Figure 12. Indexed addressing

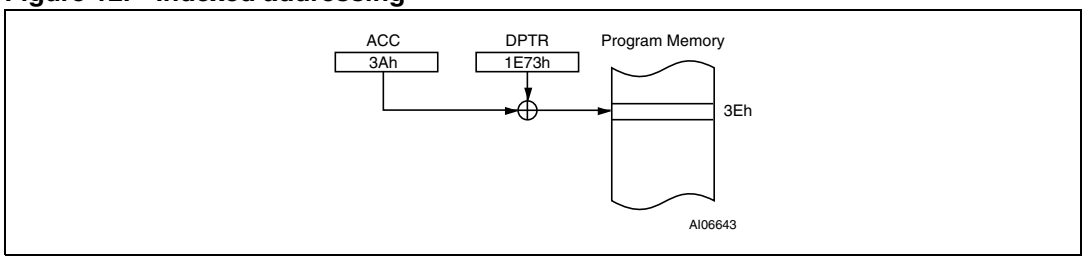


Table 12. Boolean instructions

Mnemonic	Operation
ANL C,bit	C = A .AND. bit
ANL C,/bit	C = C .AND. .NOT. bit
ORL C,bit	C = A .OR. bit
ORL C,/bit	C = C .OR. .NOT. bit
MOV C,bit	C = bit
MOV bit,C	bit = C
CLR C	C = 0
CLR bit	bit = 0
SETB C	C = 1
SETB bit	bit = 1
CPL C	C = .NOT. C
CPL bit	bit = .NOT. bit
JC rel	Jump if C =1
JNC rel	Jump if C = 0
JB bit,rel	Jump if bit =1
JNB bit,rel	Jump if bit = 0
JBC bit,rel	Jump if bit = 1; CLR bit

2.13 Relative offset

The destination address for these jumps is specified to the assembler by a label or by an actual address in Program memory. However, the destination address assembles to a relative offset byte. This is a signed (two's complement) offset byte which is added to the PC in two's complement arithmetic if the jump is executed.

The range of the jump is therefore -128 to +127 Program Memory bytes relative to the first byte following the instruction.

2.14 Jump instructions

Table 13 shows the list of unconditional jump instructions. The table lists a single "JMP add" instruction, but in fact there are three SJMP, LJMP, and AJMP, which differ in the format of the destination address. JMP is a generic mnemonic which can be used if the programmer does not care which way the jump is en-coded.

The SJMP instruction encodes the destination address as a relative offset, as described above. The instruction is 2 bytes long, consisting of the opcode and the relative offset byte. The jump distance is limited to a range of -128 to +127 bytes relative to the instruction following the SJMP.

11 Timer/counters (Timer 0, Timer 1 and Timer 2)

The UPSD321xx devices has three 16-bit Timer/Counter registers: Timer 0, Timer 1 and Timer 2. All of them can be configured to operate either as timers or event counters and are compatible with standard 8032 architecture.

In the “Timer” function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is 1/6 of the CPU clock frequency or 1/12 of the oscillator frequency (f_{OSC}).

In the “Counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 f_{OSC} clock periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the f_{OSC}. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full cycle. In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes from which to select.

11.1 Timer 0 and Timer 1

The “Timer” or “Counter” function is selected by control bits C/ T in the Special Function Register TMOD. These Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for Timers/ Counters. Mode 3 is different. The four operating modes are de-scribed in the following text.

Table 36. Control register (TCON)

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 37. Description of the TCON bits

Bit	Symbol	Function
7	TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine
6	TR1	Timer 1 run control bit. Set/cleared by software to turn Timer/Counter on or off
5	TF0	Timer 0 overflow flag. Set by hardier on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine
4	TR0	Timer 0 run control bit. Set/cleared by software to turn Timer/Counter on or off
3	IE1	Interrupt 1 Edge Flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed
2	IT1	Interrupt 1 Type Control Bit. Set/cleared by software to specify falling-edge/low-level triggered external interrupt

Figure 30. Serial port Mode 2 block diagram

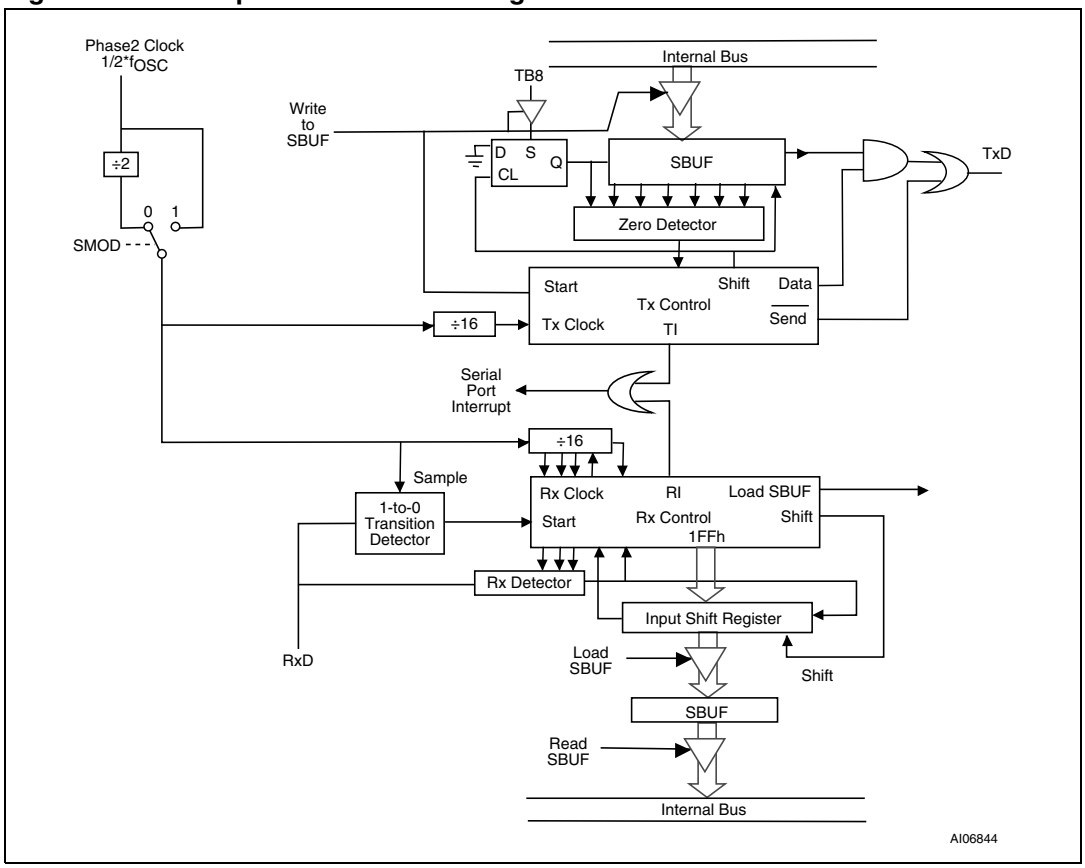
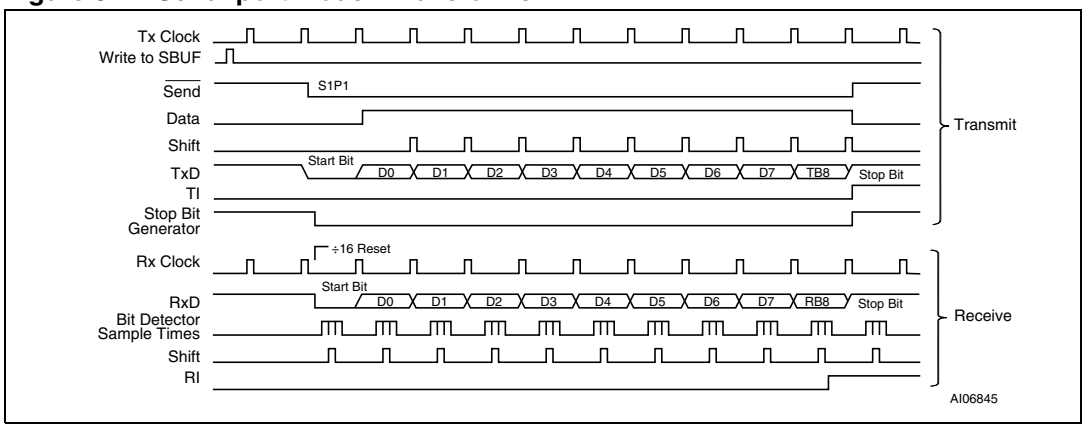


Figure 31. Serial port Mode 2 waveforms



13 Analog-to-digital convertor (ADC)

The analog to digital (A/D) converter allows conversion of an analog input to a corresponding 8-bit digital value. The A/D module has four analog inputs, which are multiplexed into one sample and hold. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog supply voltage is connected to AV_{REF} of ladder resistance of A/D module.

The A/D module has two registers which are the control register ACON and A/D result register ADAT. The register ACON, shown in *Table 47*, controls the operation of the A/D converter module. To use analog inputs, I/O is selected by P1SFS register. Also an 8-bit prescaler ASCL divides the main system clock input down to approximately 6MHz clock that is required for the ADC logic. Appropriate values need to be loaded into the prescaler based upon the main MCU clock frequency prior to use.

The processing of conversion starts when the Start bit ADST is set to '1.' After one cycle, it is cleared by hardware. The register ADAT contains the results of the A/D conversion. When conversion is completed, the result is loaded into the ADAT the A/D Conversion Status bit ADSF is set to '1.'

The block diagram of the A/D module is shown in Figure *Figure 34*. The A/D Status bit ADSF is set automatically when A/D conversion is completed, cleared when A/D conversion is in process.

The ASCL should be loaded with a value that results in a clock rate of approximately 6MHz for the ADC using the following formula:

ADC clock input = (f_{OSC} / 2) / (Prescaler register value +1)

Where f_{OSC} is the MCU clock input frequency.

The conversion time for the ADC can be calculated as follows:

ADC Conversion Time = 8 clock * 8bits * (ADC Clock) ~= 10.67usec (at 6MHz)

13.1 ADC interrupt

The ADSF Bit in the ACON register is set to '1' when the A/D conversion is complete. The status bit can be driven by the MCU, or it can be configured to generate a falling edge interrupt when the conversion is complete.

The ADSF Interrupt is enabled by setting the ADSFINT Bit in the PCON register. Once the bit is set, the external INT1 Interrupt is disabled and the ADSF Interrupt takes over as INT1. INT1 must be configured as if it is an edge interrupt input. The INP1 pin (p3.3) is available for general I/O functions, or Timer1 gate control.

Table 65. Description of the UISTA bits (continued)

Bit	Symbol	R/W	Function
4	TXD0F	R/W	Endpoint0 Data Transmit Flag. This bit is set after the data stored in Endpoint 0 transmit buffers has been sent and an ACK handshake packet from the host is received. Once the next set of data is ready in the transmit buffers, software must clear this flag. To enable the next data packet transmission, TX0E must also be set. If TXD0F Bit is not cleared, a NAK handshake will be returned in the next IN transactions. $\overline{\text{RESET}}$ clears this bit.
3	RXD0F	R/W	Endpoint0 Data Receive Flag. This bit is set after the USB module has received a data packet and responded with ACK handshake packet. Software must clear this flag after all of the received data has been read. Software must also set RX0E Bit to one to enable the next data packet reception. If RXD0F Bit is not cleared, a NAK handshake will be returned in the next OUT transaction. $\overline{\text{RESET}}$ clears this bit.
2	TXD1F	R/W	Endpoint1 / Endpoint2 Data Transmit Flag. This bit is shared by Endpoints 1 and Endpoints 2. It is set after the data stored in the shared Endpoint 1/ Endpoint 2 transmit buffer has been sent and an ACK handshake packet from the host is received. Once the next set of data is ready in the transmit buffers, software must clear this flag. To enable the next data packet transmission, TX1E must also be set. If TXD1F Bit is not cleared, a NAK handshake will be returned in the next IN transaction. $\overline{\text{RESET}}$ clears this bit.
1	EOPF	R/W	End of Packet Flag. This bit is set when a valid End of Packet sequence is detected on the D+ and D-line. Software must clear this flag. $\overline{\text{RESET}}$ clears this bit.
0	RESUMF	R/W	Resume Flag. This bit is set when USB bus activity is detected while the SUSPND Bit is set. Software must clear this flag. $\overline{\text{RESET}}$ clears this bit.

Table 66. USB Endpoint0 transmit control register (UCON0: 0EAh)

7	6	5	4	3	2	1	0
TSEQ0	STALL0	TX0E	RX0E	TP0SIZ3	TP0SIZ2	TP0SIZ1	TP0SIZ0

20 PSD module detailed operation

As shown in *Figure 14*, the PSD module consists of five major types of functional blocks:

- Memory blocks
- PLD blocks
- I/O Ports
- Power Management Unit (PMU)
- JTAG Interface

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable.

possibility of a byte being written on the first edge of WRITE Strobe ($\overline{WR}$, CNTL0). Any WRITE cycle initiation is locked when V_{CC} is below V_{LKO}.

21.5 Read

Under typical conditions, the MCU may read the primary Flash memory or the secondary Flash memory using READ operations just as it would a ROM or RAM device. Alternately, the MCU may use READ operations to obtain status information about a Program or Erase cycle that is currently in progress. Lastly, the MCU may use instructions to read special data from these memory blocks. The following sections describe these READ functions.

21.5.1 Read memory contents

Primary Flash memory and secondary Flash memory are placed in the READ mode after Power-up, chip reset, or a Reset Flash instruction (see *Table 82*). The MCU can read the memory contents of the primary Flash memory or the secondary Flash memory by using READ operations any time the READ operation is not part of an instruction.

21.5.2 Read memory sector protection status

The primary Flash memory Sector Protection Status is read with an instruction composed of 4 operations: 3 specific WRITE operations and a READ operation (see *Table 82*). During the READ operation, address Bits A6, A1, and A0 must be '0,' '1,' and '0,' respectively, while Sector Select (FS0-FS3 or CSBOOT0-CSBOOT1) designates the Flash memory sector whose protection has to be verified. The READ operation produces 01h if the Flash memory sector is protected, or 00h if the sector is not protected.

The sector protection status for all NVM blocks (primary Flash memory or secondary Flash memory) can also be read by the MCU accessing the Flash Protection registers in PSD I/O space. See *Section 21.8.1: Flash memory sector protect* for register definitions.

21.5.3 Reading the Erase/Program status bits

The Flash memory provides several status bits to be used by the MCU to confirm the completion of an Erase or Program cycle of Flash memory. These status bits minimize the time that the MCU spends performing these tasks and are defined in *Table 83*. The status bits can be read as many times as needed.

For Flash memory, the MCU can perform a READ operation to obtain these status bits while an Erase or Program instruction is being executed by the embedded algorithm. See *Section 21.6: Programming Flash memory*, for details.

21.5.4 Data polling flag (DQ7)

When erasing or programming in Flash memory, the Data Polling flag bit (DQ7) outputs the complement of the bit being entered for programming/writing on the DQ7 Bit. Once the

Program instruction or the WRITE operation is completed, the true logic value is read on the Data Polling flag bit (DQ7) (in a READ operation).

- Data Polling is effective after the fourth WRITE pulse (for a Program instruction) or after the sixth WRITE pulse (for an Erase instruction). It must be performed at the address being programmed or at an address within the Flash memory sector being erased.
- During an Erase cycle, the Data Polling flag bit (DQ7) outputs a '0.' After completion of the cycle, the Data Polling flag bit (DQ7) outputs the last bit programmed (it is a '1' after erasing).
- If the byte to be programmed is in a protected Flash memory sector, the instruction is ignored.
- If all the Flash memory sectors to be erased are protected, the Data Polling flag bit (DQ7) is reset to '0' for about 100µs, and then returns to the previous addressed byte. No erasure is performed.

21.5.5 Toggle flag (DQ6)

The Flash memory offers another way for determining when the Program cycle is completed. During the internal WRITE operation and when either the FS0-FS3 or CSBOOT0-CSBOOT1 is true, the Toggle flag bit (DQ6) toggles from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory.

When the internal cycle is complete, the toggling stops and the data READ on the Data Bus D0-D7 is the addressed memory byte. The device is now accessible for a new READ or WRITE operation. The cycle is finished when two successive Reads yield the same output data.

- The Toggle flag bit (DQ6) is effective after the fourth WRITE pulse (for a Program instruction) or after the sixth WRITE pulse (for an Erase instruction).
- If the byte to be programmed belongs to a protected Flash memory sector, the instruction is ignored.
- If all the Flash memory sectors selected for erasure are protected, the Toggle flag bit (DQ6) toggles to '0' for about 100µs and then returns to the previous addressed byte.

21.5.6 Error flag (DQ5)

During a normal Program or Erase cycle, the Error flag bit (DQ5) is to '0.' This bit is set to '1' when there is a failure during Flash memory Byte Program, Sector Erase, or Bulk Erase cycle.

In the case of Flash memory programming, the Error flag bit (DQ5) indicates the attempt to program a Flash memory bit from the programmed state, '0', to the erased state, '1,' which is not valid. The Error flag bit (DQ5) may also indicate a Time-out condition while attempting to program a byte.

In case of an error in a Flash memory Sector Erase or Byte Program cycle, the Flash memory sector in which the error occurred or to which the programmed byte belongs must no longer be used. Other Flash memory sectors may still be used. The Error Flag bit (DQ5) is reset after a Reset Flash instruction.

21.5.7 Erase time-out flag (DQ3)

The Erase Time-out Flag bit (DQ3) reflects the time-out period allowed between two consecutive Sector Erase instructions. The Erase Time-out Flag bit (DQ3) is reset to '0' after

a Sector Erase cycle for a time period of 100µs + 20% unless an additional Sector Erase instruction is decoded. After this time period, or when the additional Sector Erase instruction is decoded, the Erase Time-out Flag bit (DQ3) is set to ‘1’.

Table 83. Status bit

Functional Block	FS0-FS3/ CSBOOT0-CSBOOT1	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Flash Memory	V_{IH}	Data Polling	Toggle Flag	Error Flag	X	Erase Time-out	X	X	X

1. X = Not guaranteed value, can be read either '1' or '0.'
2. DQ7-DQ0 represent the Data Bus bits, D7-D0.
3. FS0-FS3 and CSBOOT0-CSBOOT1 are active High.

21.6 Programming Flash memory

Flash memory must be erased prior to being programmed. A byte of Flash memory is erased to all '1's (FFh), and is programmed by setting selected bits to '0'. The MCU may erase Flash memory all at once or by-sector, but not byte-by-byte. However, the MCU may program Flash memory byte-by-byte.

The primary and secondary Flash memories require the MCU to send an instruction to program a byte or to erase sectors (see *Table 82*).

Once the MCU issues a Flash memory Program or Erase instruction, it must check for the status bits for completion. The embedded algorithms that are invoked support several means to provide status to the MCU. Status may be checked using any of three methods: Data Polling, Data Toggle, or Ready/$\overline{\text{Busy}}$ (PC3).

21.6.1 Data Polling

Polling on the Data Polling Flag bit (DQ7) is a method of checking whether a Program or Erase cycle is in progress or has completed. *Figure 47* shows the Data Polling algorithm.

When the MCU issues a Program instruction, the embedded algorithm begins. The MCU then reads the location of the byte to be programmed in Flash memory to check status. The Data Polling Flag bit (DQ7) of this location becomes the complement of b7 of the original data byte to be programmed. The MCU continues to poll this location, comparing the Data Polling Flag bit (DQ7) and monitoring the Error Flag bit (DQ5). When the Data Polling Flag bit (DQ7) matches b7 of the original data, and the Error Flag bit (DQ5) remains '0,' the embedded algorithm is complete. If the Error Flag bit (DQ5) is '1,' the MCU should test the Data Polling Flag bit (DQ7) again since the Data Polling Flag bit (DQ7) may have changed simultaneously with the Error Flag bit (DQ5) (see *Figure 47*).

The Error Flag bit (DQ5) is set if either an internal time-out occurred while the embedded algorithm attempted to program the byte or if the MCU attempted to program a '1' to a bit that was not erased (not erased is logic '0').

It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed, to compare the byte that was written to the Flash memory with the byte that was intended to be written.

The Reset Flash instruction puts the Flash memory back into normal READ mode. If an Error condition has occurred (and the device has set the Error Flag bit (DQ5) to '1' the Flash memory is put back into normal READ mode within a few milliseconds of the Reset Flash instruction having been issued. The Reset Flash instruction is ignored when it is issued during a Program or Bulk Erase cycle of the Flash memory. The Reset Flash instruction aborts any on-going Sector Erase cycle, and returns the Flash memory to the normal READ mode within a few milliseconds.

21.9 SRAM

The SRAM is enabled when SRAM Select (RS0) from the DPLD is High. SRAM Select (RS0) can contain up to two product terms, allowing flexible memory mapping.

21.10 Sector Select and SRAM Select

Sector Select (FS0-FS3, CSBOOT0-CSBOOT1) and SRAM Select (RS0) are all outputs of the DPLD. They are setup by writing equations for them in PSDsoft Express. The following rules apply to the equations for these signals:

1. Primary Flash memory and secondary Flash memory Sector Select signals must *not* be larger than the physical sector size.
2. Any primary Flash memory sector must *not* be mapped in the same memory space as another Flash memory sector.
3. A secondary Flash memory sector must *not* be mapped in the same memory space as another secondary Flash memory sector.
4. SRAM, I/O, and Peripheral I/O spaces must *not* overlap.
5. A secondary Flash memory sector *may* overlap a primary Flash memory sector. In case of overlap, priority is given to the secondary Flash memory sector.
6. SRAM, I/O, and Peripheral I/O spaces *may* overlap any other memory sector. Priority is given to the SRAM, I/O, or Peripheral I/O.

21.10.1 Example

FS0 is valid when the address is in the range of 8000h to BFFFh, CSBOOT0 is valid from 8000h to 9FFFh, and RS0 is valid from 8000h to 87FFh. Any address in the range of RS0 always accesses the SRAM. Any address in the range of CSBOOT0 greater than 87FFh (and less than 9FFFh) automatically addresses secondary Flash memory segment 0. Any address greater than 9FFFh accesses the primary Flash memory segment 0. You can see that half of the primary Flash memory segment 0 and one-fourth of secondary Flash memory segment 0 cannot be accessed in this example.

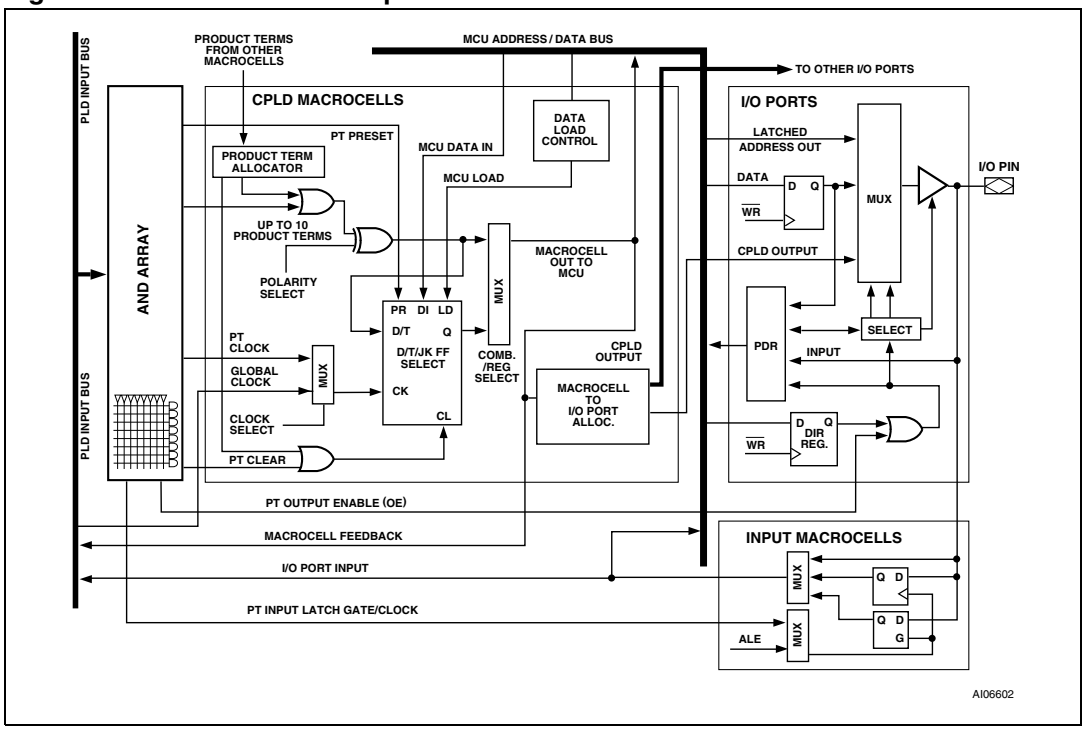
Note: An equation that defined FS1 to anywhere in the range of 8000h to BFFFh would not be valid.

Figure 49 shows the priority levels for all memory components. Any component on a higher level can overlap and has priority over any component on a lower level. Components on the same level must *not* overlap. Level one has the highest priority and level 3 has the lowest.

The Input Macrocells (IMC) and Output Macrocells (OMC) are connected to the PSD module internal data bus and can be directly accessed by the MCU. This enables the MCU software to load data into the Output Macrocells (OMC) or read data from both the Input and Output Macrocells (IMC and OMC).

This feature allows efficient implementation of system logic and eliminates the need to connect the data bus to the AND Array as required in most standard PLD macrocell architectures.

Figure 54. Macrocell and I/O ports



22.4 Output macrocell (OMC)

Eight of the Output Macrocells (OMC) are connected to Ports A and B pins and are named as McellAB0-McellAB7. The other eight macrocells are connected to Ports B and C pins and are named as McellBC0-McellBC7. If an McellAB output is not assigned to a specific pin in PSDsoft, the Macrocell Allocator block assigns it to either Port A or B. The same is true for a McellBC output on Port B or C. *Table 89* shows the macrocells and port assignment.

The Output Macrocell (OMC) architecture is shown in *Figure 55*. As shown in the figure, there are native product terms available from the AND Array, and borrowed product terms available (if unused) from other Output Macrocells (OMC). The polarity of the product term is controlled by the XOR gate. The Output Macrocell (OMC) can implement either sequential logic, using the flip-flop element, or combinatorial logic. The multiplexer selects between the sequential or combinatorial logic outputs. The multiplexer output can drive a port pin and has a feedback path to the AND Array inputs.

The flip-flop in the Output Macrocell (OMC) block can be configured as a D, T, JK, or SR type in PSDsoft. The flip-flop's clock, preset, and clear inputs may be driven from a product term of the AND Array. Alternatively, CLKIN (PD1) can be used for the clock input to the flip-

are not set, writing to the macrocell loads data to the macrocell flip-flops. See *Section 22: PLDs*.

23.9.4 OMC mask register

Each OMC Mask Register Bit corresponds to an Output Macrocell (OMC) flip-flop. When the OMC Mask Register Bit is set to a '1,' loading data into the Output Macrocell (OMC) flip-flop is blocked. The default value is '0' or unblocked.

23.9.5 Input macrocells (IMC)

The Input Macrocells (IMC) can be used to latch or store external inputs. The outputs of the Input Macrocells (IMC) are routed to the PLD input bus, and can be read by the MCU. See *Section 22: PLDs*.

23.9.6 Enable out

The Enable Out register can be read by the MCU. It contains the output enable values for a given port. A '1' indicates the driver is in output mode. A '0' indicates the driver is in tri-state and the pin is in input mode.

Table 97. Drive register pin assignment

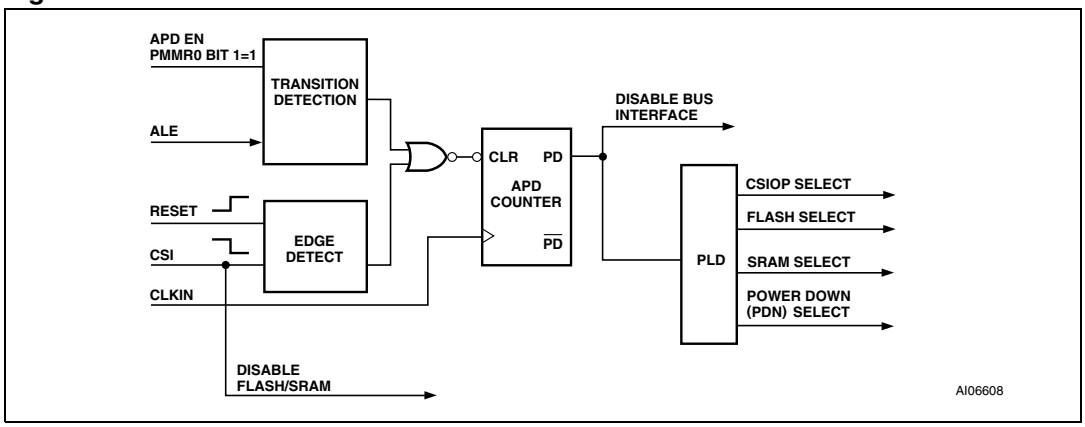
Drive Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port B	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port C	Open Drain	NA(1)	NA(1)	Open Drain	Open Drain	Open Drain	NA(1)	NA(1)
Port D	NA(1)	NA(1)	NA(1)	NA(1)	NA(1)	Slew Rate	Slew Rate	NA(1)

1. NA = Not Applicable.

Table 98. Port data registers

Register Name	Port	MCU Access
Data In	A,B,C,D	READ – input on pin
Data Out	A,B,C,D	WRITE/READ
Output Macrocell	A,B,C	READ – outputs of macrocells WRITE – loading macrocells flip-flop
Mask Macrocell	A,B,C	WRITE/READ – prevents loading into a given macrocell
Input Macrocell	A,B,C	READ – outputs of the Input Macrocells
Enable Out	A,B,C	READ – the output enable control of the port driver

Figure 63. APD unit



The PSD module has a Turbo Bit in PMMR0. This bit can be set to turn the Turbo mode off (the default is with Turbo mode turned on). While Turbo mode is off, the PLDs can achieve standby current when no PLD inputs are changing (zero DC current). Even when inputs do change, significant power can be saved at lower frequencies (AC current), compared to when Turbo mode is on. When the Turbo mode is on, there is a significant DC current component and the AC component is higher.

Automatic Power-down (APD) Unit and Power-down mode

The APD Unit, shown in *Figure 63*, puts the PSD module into Power-down mode by monitoring the activity of Address Strobe (ALE). If the APD Unit is enabled, as soon as activity on Address Strobe (ALE) stops, a four-bit counter starts counting. If Address Strobe (ALE/AS, PD0) remains inactive for fifteen clock periods of CLKIN (PD1), Power-down (PDN) goes High, and the PSD module enters Power-down mode, as discussed next.

Power-down mode

By default, if you enable the APD Unit, Power-down mode is automatically enabled. The device enters Power-down mode if Address Strobe (ALE) remains inactive for fifteen periods of CLKIN (PD1).

The following should be kept in mind when the PSD module is in Power-down mode:

- If Address Strobe (ALE) starts pulsing again, the PSD module returns to normal Operating mode. The PSD module also returns to normal Operating mode if either PSD Chip Select Input ($\overline{\text{CSI}}$, PD2) is Low or the $\overline{\text{RESET}}$ input is High.
- The MCU address/data bus is blocked from all memory and PLDs.
- Various signals can be blocked (prior to Power-down mode) from entering the PLDs by setting the appropriate bits in the PMMR registers. The blocked signals include MCU control signals and the common CLKIN (PD1).

Note: Blocking CLKIN (PD1) from the PLDs does not block CLKIN (PD1) from the APD Unit.

- All memories enter Standby mode and are drawing standby current. However, the PLD and I/O ports blocks do *not* go into Standby mode because you don't want to have to wait for the logic and I/O to "wake-up" before their outputs can change. See *Table 99* for Power-down mode effects on PSD module ports.
- Typical standby current is of the order of microamperes. These standby current values assume that there are no transitions on any PLD input.

Table 105. PSD module example, typ. power calculation at V_{CC} = 5.0 V (Turbo mode off) (continued)

Conditions			
Calculation (using typical values)			
I_{CC} total	= I_{CC}(MCUactive) x %MCUactive + I_{CC}(PSDactive) x %PSDactive + I_{PD}(pwrdown) x %pwrdown		
	I_{CC}(MCUactive)	= 20mA	
	I_{PD}(pwrdown)	= 250µA	
	I_{CC}(PSDactive)	= I_{CC}(ac) + I_{CC}(dc)	
		= %flash x 2.5mA/MHz x Freq ALE	
			+ %SRAM x 1.5mA/MHz x Freq ALE
			+ % PLD x (from graph using Freq PLD)
		= 0.8 x 2.5mA/MHz x 2MHz + 0.15 x 1.5mA/MHz x 2MHz + 24mA	
		= (4 + 0.45 + 24) mA	
		= 28.45mA	
I_{CC} total	= 20mA x 40% + 28.45mA x 40% + 250µA x 60%		
		= 8mA + 11.38mA + 150µA	
		= 19.53mA	
This is the operating power with no Flash memory Erase or Program cycles in progress. Calculation is based on all I/O pins being disconnected and I_{OUT} = 0mA.			

Table 115. DC characteristics (5 V devices)

Symbol	Parameter	Test conditions (in addition to those in *Table 110*)	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage (Ports 1, 2, 3, 4[Bits 7,6,5,4,3,1,0], XTAL1, $\overline{RESET}$)	4.5 V < V_{CC} < 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IH1}	Input high voltage (Ports A, B, C, D, 4[Bit 2], USB+, USB–)	4.5 V < V_{CC} < 5.5 V	2.0		V_{CC} + 0.5	V
V_{IL}	Input low voltage (Ports 1, 2, 3, 4[Bits 7,6,5,4,3,1,0], XTAL1, $\overline{RESET}$)	4.5 V < V_{CC} < 5.5 V	V_{SS}– 0.5		0.3 V_{CC}	V
V_{IL1}	Input low voltage (Ports A, B, C, D, 4[Bit 2])	4.5 V < V_{CC} < 5.5 V	–0.5		0.8	V
	Input low voltage (USB+, USB–)	4.5 V < V_{CC} < 5.5 V	V_{SS}– 0.5		0.8	V
V_{OL}	Output low voltage (Ports A,B,C,D)	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.25	0.45	V
V_{OL1}	Output low voltage (Ports 1,2,3,4, $\overline{WR}$, $\overline{RD}$)	I_{OL} = 1.6 mA			0.45	V
V_{OL2}	Output low voltage (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA			0.45	V
V_{OH}	Output high voltage (Ports A,B,C,D)	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9		V
V_{OH2}	Output high voltage (Port 0 in ext. Bus mode, ALE, PSEN)	I_{OH} = –800 µA	2.4			V
		I_{OH} = –80 µA	4.05			V
V_{LVR}	Low Voltage $\overline{RESET}$	0.1 V hysteresis	3.75	4.0	4.25	V
V_{OP}	XTAL open bias voltage (XTAL1, XTAL2)	I_{OL} = 3.2 mA	2.0		3.0	V
V_{LKO}	V_{CC}(min) for Flash Erase and Program		2.5		4.2	V
I_{IL}	Logic '0' input current (Ports 1,2,3,4)	V_{IN} = 0.45 V (0 V for Port 4[pin 2])	–10		–50	µA
I_{TL}	Logic 1-to-0 transition current (Ports 1,2,3,4)	V_{IN} = 3.5 V (2.5 V for Port 4[pin 2])	–65		–650	µA
I_{RST}	Reset pin pull-up current ($\overline{RESET}$)	V_{IN} = V_{SS}	–10		–55	µA

Table 116. DC characteristics (3 V devices)

Symbol	Parameter	Test conditions (in addition to those in *Table 111*)	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage (Ports 1, 2, 3, 4[Bits 7,6,5,4,3,1,0], A, B, C, D, XTAL1, $\overline{RESET}$)	3.0 V < V_{CC} < 3.6 V	0.7V_{CC}		V_{CC} + 0.5	V
V_{IH1}	Input high voltage (Port 4[Bit 2])	3.0 V < V_{CC} < 3.6 V	2.0		V_{CC} + 0.5	V
V_{IL}	Input high voltage (Ports 1, 2, 3, 4[Bits 7,6,5,4,3,1,0], XTAL1, $\overline{RESET}$)	3.0 V < V_{CC} < 3.6 V	V_{SS}– 0.5		0.3 V_{CC}	V
V_{IL1}	Input low voltage (Ports A, B, C, D)	3.0 V < V_{CC} < 3.6 V	–0.5		0.8	V
	Input low voltage (Port 4[Bit 2])	3.0 V < V_{CC} < 3.6 V	V_{SS}– 0.5		0.8	V
V_{OL}	Output low voltage (Ports A,B,C,D)	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1	V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.45	V
V_{OL1}	Output low voltage (Ports 1,2,3,4, $\overline{WR}$, $\overline{RD}$)	I_{OL} = 1.6 mA			0.45	V
		I_{OL} = 100 µA			0.3	V
V_{OL2}	Output low voltage (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA			0.45	V
		I_{OL} = 200 µA			0.3	V
V_{OH}	Output high voltage (Ports A,B,C,D)	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99		V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6		V
V_{OH2}	Output high voltage (Port 0 in ext. Bus mode, ALE, $\overline{PSEN}$)	I_{OH} = –800 µA	2.0			V
		I_{OH} = –80 µA	2.7			V
V_{LVR}	Low voltage reset	0.1 V hysteresis	2.3	2.5	2.7	V
V_{OP}	XTAL open bias voltage (XTAL1, XTAL2)	I_{OL} = 3.2 mA	1.0		2.0	V
V_{LKO}	V_{CC}(min) for Flash Erase and Program		1.5		2.2	V
I_{IL}	Logic '0' input current (Ports 1,2,3,4)	V_{IN} = 0.45 V (0 V for Port 4[pin 2])	–1		–50	µA
I_{TL}	Logic 1-to-0 transition current (Ports 1,2,3,4)	V_{IN} = 3.5 V (2.5 V for Port 4[pin 2])	–25		–250	µA
I_{RST}	Reset pin pull-up current ($\overline{RESET}$)	V_{IN} = V_{SS}	–10		–55	µA
I_{FR}	XTAL feedback resistor current (XTAL1)	XTAL1 = V_{CC} XTAL2 = V_{SS}	–20		–50	µA
I_{LI}	Input leakage current	V_{SS} < V_{IN} < V_{CC}	–1		1	µA
I_{LO}	Output leakage current	0.45 < V_{OUT} < V_{CC}	–10		10	µA

Figure 72. Input to output disable / enable

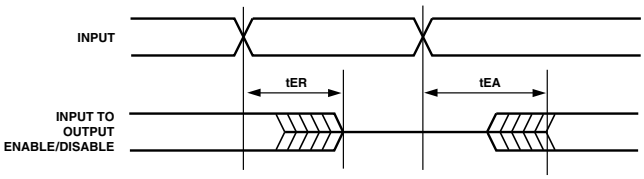


Table 124. CPLD combinatorial timing (5 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT aloc	Turbo off	Slew rate(1)	Unit
t_{PD}(2)	CPLD input pin/feedback to CPLD combinatorial output			20	+ 2	+ 10	– 2	ns
t_{EA}	CPLD input to CPLD output enable			21		+ 10	– 2	ns
t_{ER}	CPLD input to CPLD output disable			21		+ 10	– 2	ns
t_{ARP}	CPLD register clear or preset delay			21		+ 10	– 2	ns
t_{ARPW}	CPLD register clear or preset pulse width		10			+ 10		ns
t_{ARD}	CPLD array delay	Any macrocell		11	+ 2			ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount
2. t_{PD} for MCU address and control signals refers to delay from pins on Port 0, Port 2, $\overline{RD}$ $\overline{WR}$, $\overline{PSEN}$ and ALE to CPLD combinatorial output (80-pin package only)

Table 125. CPLD combinatorial timing (3 V devices)

Symbol	Parameter	Conditions	Min.	Max.	PT aloc	Turbo off	Slew rate(1)	Unit
t_{PD}(2)	CPLD input pin/feedback to CPLD combinatorial output			40	+ 4	+ 20	– 6	ns
t_{EA}	CPLD input to CPLD output enable			43		+ 20	– 6	ns
t_{ER}	CPLD input to CPLD output disable			43		+ 20	– 6	ns
t_{ARP}	CPLD register clear or preset delay			40		+ 20	– 6	ns
t_{ARPW}	CPLD register clear or preset pulse width		25			+ 20		ns
t_{ARD}	CPLD array delay	Any macrocell		25	+ 4			ns

1. Fast Slew Rate output available on PA3-PA0, PB3-PB0, and PD2-PD1. Decrement times by given amount
2. t_{PD} for MCU address and control signals refers to delay from pins on Port 0, Port 2, $\overline{RD}$ $\overline{WR}$, $\overline{PSEN}$ and ALE to CPLD combinatorial output (80-pin package only)