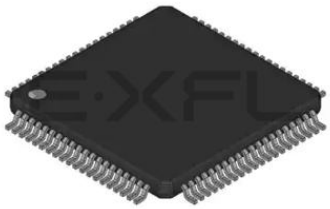
Infineon Technologies - XC2387C136F100LABKXUMA1 Datasheet



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Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	1.088MB (1.088M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	90K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2387c136f100labkxuma1

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XC238xC Data Sheet
Revision History: V1.3 2011-07

Previous Versions:
V1.2, 2010-09
V1.1, 2010-02 Preliminary

Page	Subjects (major changes since last revision)
11	Clarified available Flash and SRAM memory allocation.
76	USIC “QSPI” protocol shortcut removed due to ambiguity (interpreted as Queued SPI or Quad SPI).
106	Relaxed the conditions for short-term deviation of internal clock source frequency Δf_{INT}.
106	Added startup time from power-on t_{SPO}
109	Removed the 128MHz conditions for N_{WSFLE}
116	Added the minimum PLL free running frequency. Reduced the min/max bandwidth.
136	Added notes on required pad settings for FlexRay operation. Added note on FlexRay operation frequency.
136	Corrected parameter name f(oscdd) to f(osc) in FleyRay timing table.
144	Thermal resistance values updated.

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Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
9	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU62_CCPOS1A	I	St/B	**CCU62 Position Input 1**
	TMS_C	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
10	P8.2	O0 / I	St/B	**Bit 2 of Port 8, General Purpose Input/Output**
	CCU60_CC62	O1	St/B	**CCU60 Channel 2 Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	U1C1_DOUT	O3	St/B	**USIC1 Channel 1 Shift Data output**
	CCU60_CC62INB	I	St/B	**CCU60 Channel 2 Input**
11	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	CCU62_CTRAPA	I	St/B	**CCU62 Emergency Trap Input**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
69	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_SELO 0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_SELO 1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_CC19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	A19	OH	St/B	**External Bus Interface Address Line 19**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	RxDC0D	I	St/B	**CAN Node 0 Receive Data Input**
	ESR2_6	I	St/B	**ESR2 Trigger Input 6**
70	P4.4	O0 / I	St/B	**Bit 4 of Port 4, General Purpose Input/Output**
	U3C0_SELO 2	O1	St/B	**USIC3 Channel 0 Select/Control 2 Output**
	CC2_CC28	O3 / I	St/B	**CAPCOM2 CC28IO Capture Inp./ Compare Out.**
	$\overline{CS4}$	OH	St/B	**External Bus Interface Chip Select 4 Output**
	CLKIN2	I	St/B	**Clock Signal Input 2**
	U3C0_DX2C	I	St/B	**USIC3 Channel 0 Shift Control Input**
71	P4.3	O0 / I	St/B	**Bit 3 of Port 4, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CC2_CC27	O3 / I	St/B	**CAPCOM2 CC27IO Capture Inp./ Compare Out.**
	$\overline{CS3}$	OH	St/B	**External Bus Interface Chip Select 3 Output**
	RxDC2A	I	St/B	**CAN Node 2 Receive Data Input**
	T2EUDA	I	St/B	**GPT12E Timer T2 External Up/Down Control Input**
	CCU62_CCP OS2B	I	St/B	**CCU62 Position Input 2**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P0.1	O0 / I	St/B	**Bit 1 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_CC61	O3	St/B	**CCU61 Channel 1 Output**
	A1	OH	St/B	**External Bus Interface Address Line 1**
	U1C0_DX0B	I	St/B	**USIC1 Channel 0 Shift Data Input**
	CCU61_CC61INA	I	St/B	**CCU61 Channel 1 Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
80	P2.8	O0 / I	DP/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_SCLKOUT	O1	DP/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	DP/B	**Programmable Clock Signal Output** [1]
	CC2_CC21	O3 / I	DP/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	A21	OH	DP/B	**External Bus Interface Address Line 21**
	U0C1_DX1D	I	DP/B	**USIC0 Channel 1 Shift Clock Input**
81	P4.7	O0 / I	St/B	**Bit 7 of Port 4, General Purpose Input/Output**
	CC2_CC31	O3 / I	St/B	**CAPCOM2 CC31IO Capture Inp./ Compare Out.**
	T4EUDA	I	St/B	**GPT12E Timer T4 External Up/Down Control Input**
	CCU61_CCPOS2A	I	St/B	**CCU61 Position Input 2**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
84	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_CC60	O2	St/B	**CCU60 Channel 0 Output**
	AD0	OH / IH	St/B	**External Bus Interface Address/Data Line 0**
	CCU60_CC60INA	I	St/B	**CCU60 Channel 0 Input**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
85	P3.0	O0 / I	St/B	**Bit 0 of Port 3, General Purpose Input/Output**
	U2C0_DOUT	O1	St/B	**USIC2 Channel 0 Shift Data Output**
	ESR1_1	I	St/B	**ESR1 Trigger Input 1**
	U2C0_DX0A	I	St/B	**USIC2 Channel 0 Shift Data Input**
	U2C0_DX1A	I	St/B	**USIC2 Channel 0 Shift Clock Input**
86	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	AD1	OH / IH	St/B	**External Bus Interface Address/Data Line 1**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
104	P3.6	O0 / I	St/B	**Bit 6 of Port 3, General Purpose Input/Output**
	U2C1_DOUT	O1	St/B	**USIC2 Channel 1 Shift Data Output**
	U0C0_SELO 6	O3	St/B	**USIC0 Channel 0 Select/Control 6 Output**
	U2C1_DX0A	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX1B	I	St/B	**USIC2 Channel 1 Shift Clock Input**
105	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_COU T63	O2	St/B	**CCU60 Channel 3 Output**
	AD7	OH / IH	St/B	**External Bus Interface Address/Data Line 7**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_CCP OS0A	I	St/B	**CCU60 Position Input 0**
	T4INB	I	St/B	**GPT12E Timer T4 Count/Gate Input**
106	P0.7	O0 / I	St/B	**Bit 7 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	U1C0_SELO 3	O2	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	A7	OH	St/B	**External Bus Interface Address Line 7**
	U1C1_DX0B	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_CTR APB	I	St/B	**CCU61 Emergency Trap Input**
107	P3.7	O0 / I	St/B	**Bit 7 of Port 3, General Purpose Input/Output**
	U2C1_DOUT	O1	St/B	**USIC2 Channel 1 Shift Data Output**
	U2C0_SELO 3	O2	St/B	**USIC2 Channel 0 Select/Control 3 Output**
	U0C0_SELO 7	O3	St/B	**USIC0 Channel 0 Select/Control 7 Output**
	U2C1_DX0B	I	St/B	**USIC2 Channel 1 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
138	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XC238xC completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
139	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	**CAN Node 0 Receive Data Input**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**
140	$\overline{\text{ESR2}}$	O0 / I	St/B	**External Service Request 2** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC1E	I	St/B	**CAN Node 1 Receive Data Input**
	CCU60_CTRAPC	I	St/B	**CCU60 Emergency Trap Input**
	CCU61_CTRAPC	I	St/B	**CCU61 Emergency Trap Input**
	CCU62_CTRAPC	I	St/B	**CCU62 Emergency Trap Input**
	CCU63_CTRAPC	I	St/B	**CCU63 Emergency Trap Input**
	U1C1_DX0D	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2C	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX0E	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX2B	I	St/B	**USIC2 Channel 1 Shift Control Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
20	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.*
2, 36, 38, 72, 74, 108, 110, 144	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.*
1, 37, 73, 109	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground.* *For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.*

1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

Up to 24 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC2000 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 8**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

The on-chip Flash memory stores code, constant data, and control data. The 1,600 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 6 modules of 256 Kbytes. Each module is organized in 4-Kbyte sectors.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

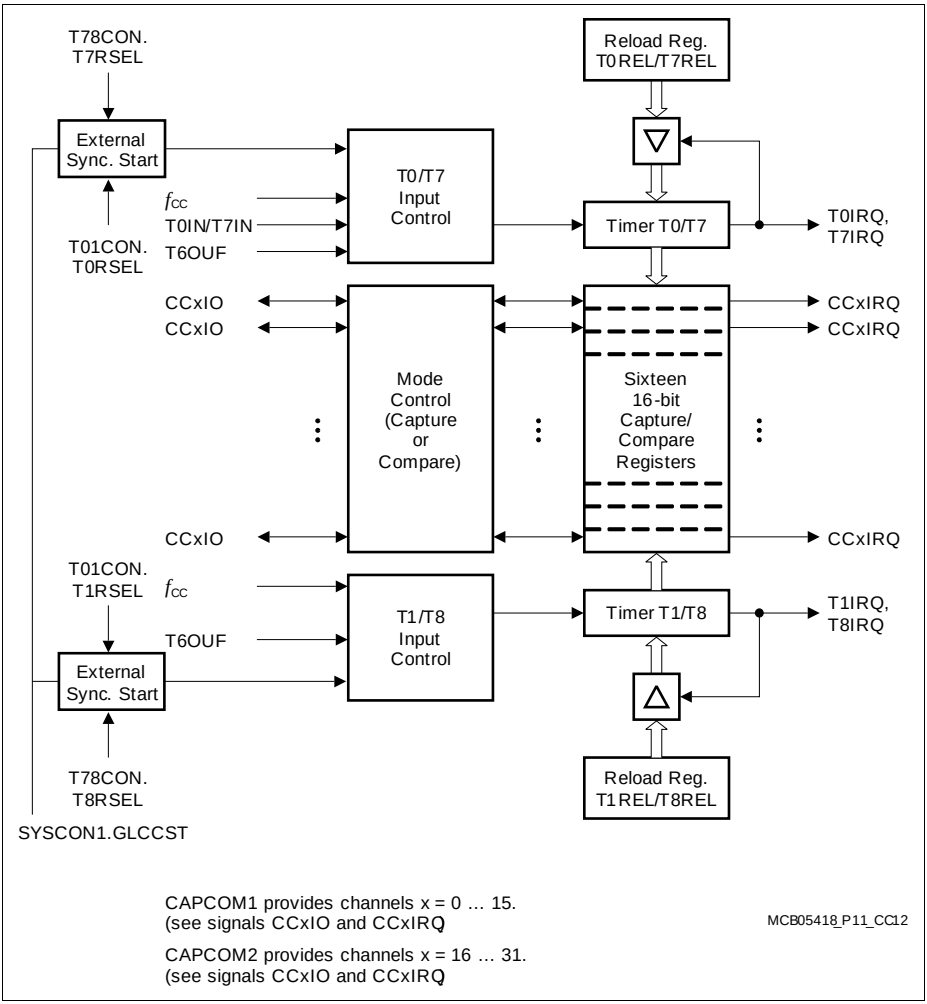

Figure 6 CAPCOM Unit Block Diagram

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - module capability: maximum baud rate = f_{SYS} / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - module capability: maximum baud rate = f_{SYS} / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
  - module capability: maximum baud rate = f_{SYS} / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - module capability: maximum baud rate = f_{SYS} / 2

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

Clock control, address decoding, and service request control are managed outside the E-Ray module kernel.

FlexRay™ Module Features

For communication on a FlexRay™ network, individual Message Buffers with up to 254 data bytes are configurable. The message storage consists of a single-ported Message RAM that holds up to 128 Message Buffers. All functions concerning the handling of messages are implemented in the Message Handler. Those functions are the acceptance filtering, the transfer of messages between the two FlexRay™ Channel Protocol Controllers and the Message RAM, maintaining the transmission schedule as well as providing message status information.

The register set of the E-Ray IP-module can be accessed directly by an external Host via the module's Host interface. These registers are used to control/configure/monitor the FlexRay™ Channel Protocol Controllers, Message Handler, Global Time Unit, System Universal Control, Frame and Symbol Processing, Network Management, Service Request Control, and to access the Message RAM via Input / Output Buffer.

The E-Ray IP-module supports the following features:

- Conformance with FlexRay™ protocol specification V2.1
- Data rates of up to 10 Mbit/s on each channel
- Up to 128 Message Buffers configurable
- 8 Kbytes of Message RAM for storage of e.g. 128 Message Buffers with max. 48 bytes data field or up to 30 Message Buffers with 254 bytes Data Sections
- Configuration of Message Buffers with different payload lengths possible
- One configurable receive FIFO
- Each Message Buffer can be configured as receive buffer, as transmit buffer or as part of the receive FIFO
- Host access to Message Buffers via Input and Output Buffer.
  Input Buffer: Holds message to be transferred to the Message RAM
  Output Buffer: Holds message read from the Message RAM
- Filtering for slot counter, cycle counter, and channel
- Maskable module service requests
- Network Management supported
- Four service request lines
- Automatic delayed read access to Output Command Request Register (OBCR) if a data transfer from Message RAM to Output Shadow Buffer (initiated by a previous write access to the OBCR) is ongoing.
- Automatic delayed read access to Input Command Request Register (IBCR) if a data transfer from Input Shadow Buffer to Message RAM to (initiated by a previous write access to the IBCR) is ongoing.
- Four Input Buffers for building up transmission Frames in parallel.
- Flag indicating which Input Buffer is currently accessible by the host.

4.6 Flash Memory Parameters

The XC238xC is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XC238xC's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 25 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	7[1)]		$N_{FL\_RD} \leq 1$
		–	–	1[2)]		$N_{FL\_RD} > 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycles	$t_{RET} \geq$ 20 years
Flash wait states[3)]	$N_{WSFLASH}$ SR	1	–	–		$f_{SYS} \leq$ 8 MHz
		2	–	–		$f_{SYS} \leq$ 13 MHz
		3	–	–		$f_{SYS} \leq$ 17 MHz
		4	–	–		$f_{SYS} >$ 17 MHz
Flash wait state extension[4)]	N_{WSFLE} SR	0	–	–		$f_{SYS} \leq$ 80 MHz
		1	–	–		$f_{SYS} >$ 80 MHz
Erase time per sector/page	t_{ER} CC	–	7[5)]	8.0	ms	
Programming time per page	t_{PR} CC	–	3[5)]	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	years	$N_{ER} \leq$ 1.000 cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycles	

Table 25 Flash Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase cycles	N_{ER} SR	–	–	15.000	cycles	$t_{RET} \geq$ 5 years; Valid for up to 64 user selected sectors (data storage)
		–	–	1.000	cycles	$t_{RET} \geq$ 20 years

1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.
2) Flash module 6 can be erased/programmed while code is executed and/or data is read from any other Flash module.
3) Value of IMB_IMBCTRL.WSFLASH.
4) Value of IMB_IMBCTRL.WSFLE.
5) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC238xC Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.7.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.
Please refer to the Programmer's Guide.

4.7.3 External Clock Input Parameters

These parameters specify the external clock generation for the XC238xC. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2
- By supplying an **external clock signal**
  - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 or CLKIN2 (IO voltage domain)

If connected to CLKIN1 or CLKIN2, the input signal must reach the defined input levels V_{IL} and V_{IH}. If connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Note: Operating Conditions apply.

Table 28 External Clock Input Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC} SR	4	–	40	MHz	Input= Clock Signal
		4	–	20	MHz	Input= Crystal or Ceramic Resonator
XTAL1 input current absolute value	$\|I_{IL}\|$ CC	–	–	20	µA	
Input clock high time	t_1 SR	6	–	–	ns	
Input clock low time	t_2 SR	6	–	–	ns	
Input clock rise time	t_3 SR	–	8	8	ns	
Input clock fall time	t_4 SR	–	8	8	ns	
Input voltage amplitude on XTAL1[1)]	V_{AX1} SR	0.3 x V_{DDIM}	–	–	V	f_{OSC}≥ 4 MHz; f_{OSC}< 16 MHz
		0.4 x V_{DDIM}	–	–	V	f_{OSC}≥ 16 MHz; f_{OSC}< 25 MHz
		0.5 x V_{DDIM}	–	–	V	f_{OSC}≥ 25 MHz; f_{OSC}≤ 40 MHz
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDIM}	–	1.7	V	[2)]

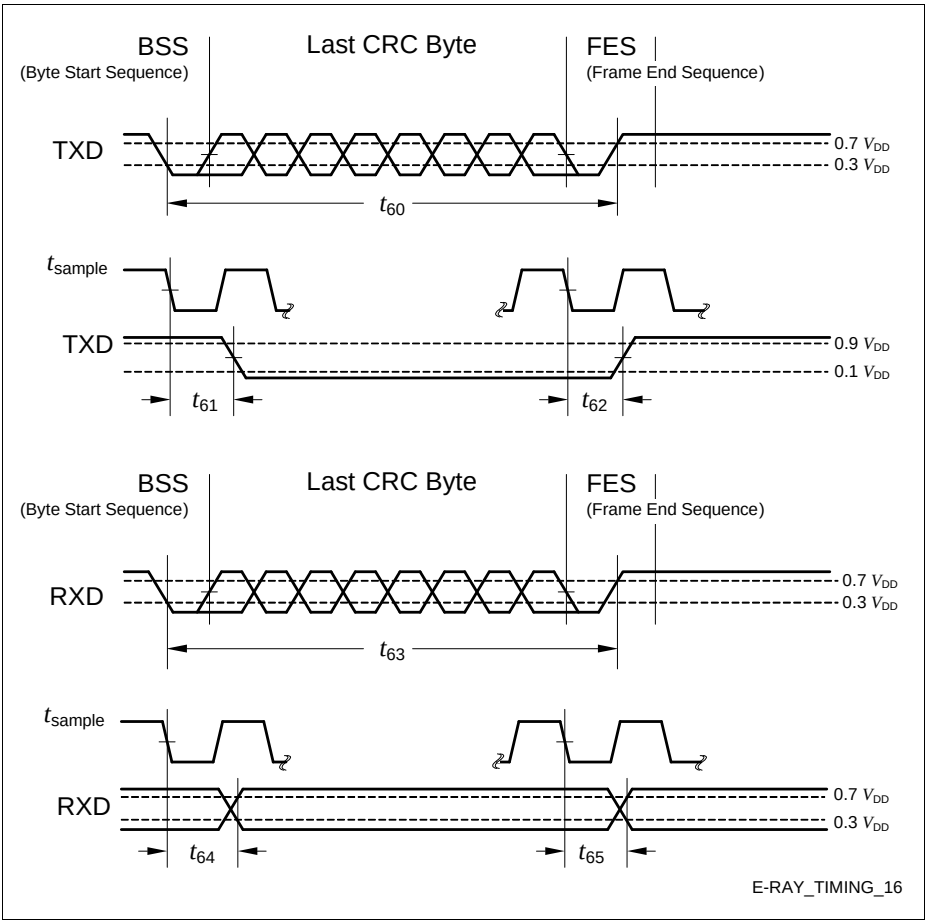

Figure 28 FlexRay Timing

Table 41 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 41 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1)]	t_{11} SR	25	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time[1)]	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	3	–	–	ns	pad_type= high speed [2)]
		6	–	–	ns	pad_type= stan dard
DAP1 hold after DAP0 rising edge	t_{17} SR	4	–	–	ns	pad_type= high speed [2)]
		6	–	–	ns	pad_type= stan dard
DAP1 valid per DAP0 clock period[3)]	t_{19} CC	19	21	–	ns	pad_type= high speed [2)]
		12	17	–	ns	pad_type= stan dard

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) Available high speed pins can be found in the pin definitions table in chapter 2.

3) The Host has to find a suitable sampling point by analyzing the sync telegram response.

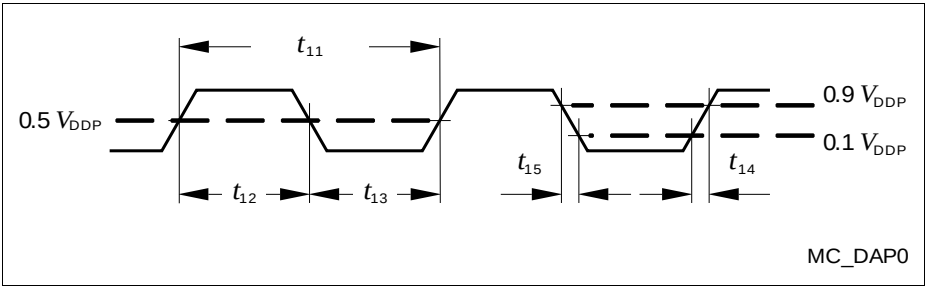

Figure 29 Test Clock Timing (DAP0)

5 Package and Reliability

The XC2000 Family devices use the package type PG-LQFP (Plastic Green - Low Profile Quad Flat Package). The following specifications must be regarded to ensure proper integration of the XC238xC in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 44 Package Parameters (PG-LQFP-144-13)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	Ex × Ey	–	8.0 × 8.0	mm	–
Power Dissipation	P_{DISS}	–	< 1	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	39	K/W	2-layer, no vias[1)]
			33	K/W	4-layer, unsoldered[2)]
			24	K/W	4-layer, no vias, soldered[3)]
			19	K/W	4-layer, vias, soldered[4)]

1) Device mounted on a 2-layer JEDEC board (JESD 51-3) without thermal vias; exposed pad soldered or not soldered.

2) Device mounted on a 4-layer JEDEC board (JESD 51-7) with or without thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (JESD 51-7) without thermal vias; exposed pad soldered.

4) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.
Board layout examples are given in an application note.

Package Compatibility Considerations

The XC238xC is a member of the XC2000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Pad (if present) may vary.