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Understanding <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Details

E·XFl

Product Status	Active
Туре	Floating Point
Interface	DAI, SPI
Clock Rate	150MHz
Non-Volatile Memory	ROM (384kB)
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21261skstz150

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elements, but each processing element operates on different data. This architecture is efficient at executing math intensive audio algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single precision floating-point, 40-bit extended precision floatingpoint, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2126x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2126x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on Page 1). With the ADSP-2126x's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2126x includes an on-chip instruction cache that enables three-bus operation to fetch an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The ADSP-2126x's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-2126x contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the ADSP-2126x can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-2126x adds the following architectural features to the SIMD SHARC family core:

Dual-Ported On-Chip Memory

The ADSP-21262 and ADSP-21266 contain two megabits of internal SRAM and four megabits of internal mask-programmable ROM. The ADSP-21261 contain one megabit of internal SRAM and three megabits of internal mask-programmable ROM. Each block can be configured for different combinations of code and data storage (see memory maps, Table 4 and Table 5). Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory, in combination with three separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

The ADSP-2126x is available with a variety of multichannel surround sound decoders, preprogrammed in ROM memory. Table 3 shows the configuration of decoder algorithms.

Table 3.	Multichannel Surround Sound Decoder Algorithms
in On-Cl	hip ROM

Algorithms	B ROM	C ROM	D ROM
РСМ	Yes	Yes	Yes
AC-3	Yes	Yes	Yes
DTS 96/24	v2.2	v2.3	v2.3
AAC (LC)	Yes	Yes	Coefficients only
WMAPRO 7.1 96 KHz	No	No	Yes
MPEG2 BC 2ch	Yes	Yes	No
Noise	Yes	Yes	Yes
DPL2x/EX	DPL2	Yes	Yes
Neo:6/ES (v2.5046)	Yes	Yes	Yes

Table 5. Internal Memory Space (ADSP-21262/ADSP-21266)

IOP Registers 0x0000 0000–0003 FFFF				
Long Word (64 Bits)	Extended Precision Normal or Instruction Word (48 Bits)	Normal Word (32 Bits)	Short Word (16 Bits)	
Block 0 SRAM	Block 0 SRAM	Block 0 SRAM	Block 0 SRAM	
0x0004 0000–0x0004 3FFF	0x0008 0000–0x0008 5555	0x0008 0000–0x0008 7FFF	0x0010 0000–0x0010 FFFF	
Reserved	Reserved	Reserved	Reserved	
0x0004 4000–0x0005 7FFF		0x0008 8000–0x000A FFFF	0x0011 0000–0x0015 FFFF	
Block 0 ROM	Block 0 ROM	Block 0 ROM	Block 0 ROM	
0x0005 8000–0x0005 FFFF	0x000A 0000–0x000A AAAA	0x000B 0000–0x000B FFFF	0x0016 0000–0x0017 FFFF	
Block 1 SRAM	Block 1 SRAM	Block 1 SRAM	Block 1 SRAM	
0x0006 0000–0x0006 3FFF	0x000C 0000–0x000C 5555	0x000C 0000–0x000C 7FFF	0x0018 0000–0x0018 FFFF	
Reserved	Reserved	Reserved	Reserved	
0x0006 4000-0x0007 7FFF		0x000C 8000–0x000E FFFF	0x0019 0000–0x001D FFFF	
Block 1 ROM	Block 1 ROM	Block 1 ROM	Block 1 ROM	
0x0007 8000–0x0007 FFFF	0x000E 0000–0x000E AAAA	0x000F 0000–0x000F FFFF	0x001E 0000–0x001F FFFF	

Digital Application Interface (DAI)

The Digital application interface provides the ability to connect various peripherals to any of the SHARC DSP's DAI pins (DAI_P20-1).

Connections are made using the signal routing unit (SRU, shown in the block diagram on Page 1).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes six serial ports, two precision clock generators (PCGs), an input data port (IDP), six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2126x core, configurable as either eight channels of I²S or serial data, or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the ADSP-2126x's serial ports.

For complete information on using the DAI, see the *ADSP-2126x SHARC DSP Peripherals Manual*.

Serial Ports

The ADSP-2126x features six full duplex synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as the Analog Devices AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has its own dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

The serial ports operate at up to one-quarter of the DSP core clock rate, providing each with a maximum data rate of 50M bits/sec for a 200 MHz core and 37.5M bits/sec for a 150 MHz core. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I²S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle, two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample-pair and I²S protocols (I²S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs) with two data pins, allowing four left-justified sample-pair or I²S channels (using two stereo devices) per serial port with a maximum of up to 24 audio channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I²S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ -law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

TARGET BOARD JTAG EMULATOR CONNECTOR

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2126x processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore[®] Embedded Studio and/or VisualDSP++[®]), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse[™] framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite[®] evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders[®], which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of Cross-Core Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set

breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2126x architecture and functionality. For detailed information on the ADSP-2126x family core architecture and instruction set, refer to the ADSP-2126x SHARC DSP Core Manual and the ADSP-21160 SHARC DSP Instruction Set Reference.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab[™] site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

The ADSP-2126x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for TRST). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following: DAI_Px, SPICLK, MISO, MOSI, EMU, TMS, TRST, TDI and AD15-0 (NOTE: These pins have internal pull-up resistors.)

The following symbols appear in the Type column of Table 6: A = asynchronous, G = ground, I = input, O = output, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, and T = three-state.

Table 6. Pin Descriptions

		State During and	
Pin	Туре	After Reset	Function
AD15-0	I/O/T	Rev. 0.1 silicon— AD15–0 pins are driven low both during and after reset. Rev. 0.2 silicon— AD15–0 pins are three-stated and pulled high both	Parallel Port Address/Data. The parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 k Ω internal pull-up resistor. See Address Data Modes on Page 13 for details of the AD pin operation. For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, A23–8; ALE is used in conjunction with an external latch to retain the values of the A23–8. For 16-bit mode: ALE is automatically asserted whenever a change occurs in the address
		during and after reset.	bits, A15–0; ALE is used in conjunction with an external latch to retain the values of the A15–0. To use these pins as flags (FLAG15–0), set (= 1) Bit 20 of the SYSCTL register and disable the parallel port. See Table 7 on Page 13 for a list of how the AD15–0 pins map to the flag pins. When configured in the IDP_PDAP_CTL register, the IDP Channel 0 can use these pins for parallel input data.
RD	0	Output only, driven high ¹	Parallel Port Read Enable. RD is asserted low whenever the DSP reads 8-bit or 16-bit data from an external memory device. When AD15–0 are flags, this pin remains deasserted.
WR	0	Output only, driven high ¹	Parallel Port Write Enable. \overline{WR} is asserted low whenever the DSP writes 8-bit or 16-bit data to an external memory device. When AD15–0 are flags, this pin remains deasserted.
ALE	0	Output only, driven Iow ¹	Parallel Port Address Latch Enable. ALE is asserted whenever the DSP drives a new address on the parallel port address pin. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15–0 are flags, this pin remains deasserted.
FLAG3-0	I/O/A	Three-state	Flag Pins. Each FLAG pin is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals. These pins can be used as an SPI interface slave select output during SPI mastering. These pins are also multiplexed with the IRQx and the TIMEXP signals. In SPI master boot mode, FLAG0 is the slave select pin that must be connected to an SPI EPROM. FLAG0 is configured as a slave select during SPI master boot. When Bit 16 is set (= 1) in the SYSCTL register, FLAG0 is configured as IRQ0. When Bit 17 is set (= 1) in the SYSCTL register, FLAG1 is configured as IRQ1. When Bit 18 is set (= 1) in the SYSCTL register, FLAG2 is configured as IRQ2. When Bit 19 is set (= 1) in the SYSCTL register, FLAG3 is configured as TIMEXP, which indicates that the system timer has expired.
DAI_P20-1	I/O/T	Three-state with programmable pull-up	Digital Application Interface Pins . These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the SRU can be routed to any of these pins. The SRU provides the connection from the serial ports, input data port, precision clock generators, and timers to the DAI_P20-1 pins. These pins have internal 22.5 k Ω pull-up resistors which are enabled on reset. These pull-ups can be disabled in the DAI_PIN_PULLUP register.

Table 6. Pin Descriptions (Continued)

		State During and	
Pin	Туре	After Reset	Function
SPICLK	1/0	Three-state with pull-up enabled, driven high in SPI- master boot mode	Serial Peripheral Interface Clock Signal. Driven by the master, this signal controls the rate at which data is transferred. The master can transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (HIGH). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 22.5 k Ω internal pull-up resistor. If SPI master boot mode is selected, MOSI and SPICLK pins are driven during reset. These pins are not three-stated during reset in SPI master boot mode.
SPIDS	1	Input only	Serial Peripheral Interface Slave Device Select. An active low signal used to select the DSP as an SPI slave device. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode, the DSP's SPIDS signal can be driven by a slave device to signal to the DSP (as SPI master) that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single master, multiple-slave configuration where flag pins are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For ADSP-2126x to ADSP-2126x SPI interaction, any of the master ADSP-2126x's flag pins can be used to drive the SPIDS signal on the ADSP-2126x SPI slave device.
MOSI	I/O (O/D)	Three-state with pull-up enabled, driven low in SPI- master boot mode	SPI Master Out Slave In . If the ADSP-2126x is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the ADSP-2126x is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an ADSP-2126x SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has a 22.5 k Ω internal pull-up resistor. If SPI master boot mode is selected, MOSI and SPICLK pins are driven during reset. These pins are not three-stated during reset in SPI master boot mode.
MISO	I/O (O/D)	Three-state with pull-up enabled	SPI Master In Slave Out . If the ADSP-2126x is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the ADSP-2126x is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an ADSP-2126x SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has a 22.5 k Ω internal pull-up resistor. MISO can be configured as O/D by setting the OPD bit in the SPICTL register. Note: Only one slave is allowed to transmit data at any given time. To enable broadcast transmission to multiple SPI slaves, the DSP's MISO pin can be disabled by setting (= 1) Bit 5 (DMISO) of the SPICTL register.
BOOT_CFG1-0	1	Input only	Boot Configuration Select . Selects the boot mode for the DSP. The BOOT_CFG pins must be valid before reset is asserted. See Table 8 on Page 13 for a description of the boot modes.
CLKIN		Input only	Local Clock In . Used in conjunction with XTAL. CLKIN is the ADSP-2126x clock input. It configures the ADSP-2126x to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-2126x to use the external clock source such as an external clock oscillator. The core is clocked either by the PLL output or this clock input depending on the CLK_CFG1–0 pin settings. CLKIN should not be halted, changed, or operated below the specified frequency.
XIAL	0	Output only ²	Crystal Oscillator Terminal . Used in conjunction with CLKIN to drive an external crystal.

ADDRESS DATA PINS AS FLAGS

To use these pins as flags (FLAG15–0), set (= 1) Bit 20 of the SYSCTL register and disable the parallel port.

Table 7. AD15-0 to FLAG Pin Mapping

AD Pin	Flag Pin	AD Pin	Flag Pin
AD0	FLAG8	AD8	FLAG0
AD1	FLAG9	AD9	FLAG1
AD2	FLAG10	AD10	FLAG2
AD3	FLAG11	AD11	FLAG3
AD4	FLAG12	AD12	FLAG4
AD5	FLAG13	AD13	FLAG5
AD6	FLAG14	AD14	FLAG6
AD7	FLAG15	AD15	FLAG7

Boot Modes

Table 8. Boot Mode Selection

BOOT_CFG1-0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port Boot via EPROM
11	Reserved

CORE INSTRUCTION RATE TO CLKIN RATIO MODES

Table 9. Core Instruction Rate/CLKIN Ratio Selection

CLK_CFG1-0	Core to CLKIN Ratio
00	3:1
01	16:1
10	8:1
11	Reserved

ADDRESS DATA MODES

Table 10 shows the functionality of the AD pins for 8-bit and 16-bit transfers to the parallel port. For 8-bit data transfers, ALE latches address bits A23–A8 when asserted, followed by address bits A7–A0 and data bits D7–D0 when deasserted. For 16-bit data transfers, ALE latches address bits A15–A0 when asserted, followed by data bits D15–D0 when deasserted.

Table 10.	Address/Data	Mode	Selection
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EP Data Mode	ALE	AD7–0 Function	AD15-8 Function
8-bit	Asserted	A15–8	A23–16
8-bit	Deasserted	D7–0	A7–0
16-bit	Asserted	A7–0	A15–8
16-bit	Deasserted	D7–0	D15–8

PRODUCT SPECIFICATIONS

OPERATING CONDITIONS

Parameter ¹	Description	Min	Max	Unit
V _{DDINT}	Internal (Core) Supply Voltage	1.14	1.26	V
A _{VDD}	Analog (PLL) Supply Voltage	1.14	1.26	V
V _{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
V _{IH}	High Level Input Voltage ² @ V _{DDEXT} = Max	2.0	$V_{DDEXT} + 0.5$	V
V _{IL}	Low Level Input Voltage ² @ V _{DDEXT} = Min	-0.5	+0.8	V
V _{IH_CLKIN}	High Level Input Voltage ³ @ V _{DDEXT} = Max	1.74	$V_{DDEXT} + 0.5$	V
V _{IL_CLKIN}	Low Level Input Voltage @ V _{DDEXT} = Min	-0.5	+1.19	V
T _{AMB} K Grade	Ambient Operating Temperature ^{4, 5}	0	+70	°C
T _{AMB} B Grade	Ambient Operating Temperature ^{4, 5}	-40	+85	°C

¹Specifications subject to change without notice.

²Applies to input and bidirectional pins: AD15–0, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, SPIDS, BOOT_CFGx, CLK_CFGx, RESET, TCK, TMS, TDI, TRST. ³Applies to input pin CLKIN.

⁴See Thermal Characteristics on Page 38 for information on thermal specifications.

⁵ See Engineer-to-Engineer Note (No. EE-216) for further information.

ELECTRICAL CHARACTERISTICS

Parameter ¹	Description	Test Conditions	Min	Max	Unit
V _{OH}	High Level Output Voltage ²	@ $V_{DDEXT} = Min, I_{OH} = -1.0 \text{ mA}^3$	2.4		V
V _{OL}	Low Level Output Voltage ²	@ $V_{DDEXT} = Min$, $I_{OL} = 1.0 \text{ mA}^3$		0.4	V
I _{IH}	High Level Input Current ^{4, 5}	$@V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max$		10	μΑ
I _{IL}	Low Level Input Current ⁴	@ $V_{DDEXT} = Max, V_{IN} = 0 V$		10	μA
I _{ILPU}	Low Level Input Current Pull-Up ⁵	@ $V_{DDEXT} = Max, V_{IN} = 0 V$		200	μΑ
I _{OZH}	Three-State Leakage Current ^{6, 7, 8}	$@V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max$		10	μΑ
I _{OZL}	Three-State Leakage Current ⁶	@ $V_{DDEXT} = Max, V_{IN} = 0 V$		10	μA
I _{OZLPU}	Three-State Leakage Current Pull-Up ⁷	@ $V_{DDEXT} = Max, V_{IN} = 0 V$		200	μΑ
I _{DD-INTYP}	Supply Current (Internal) ^{9, 10, 11}	$t_{CCLK} = 5.0 \text{ ns}, V_{DDINT} = 1.2 \text{ V}, T_{AMB} = +25^{\circ}\text{C}$		500	mA
I _{AVDD}	Supply Current (Analog) ¹¹	$A_{VDD} = Max$		10	mA
C _{IN}	Input Capacitance ^{12, 13}	$f_{IN} = 1 \text{ MHz}, T_{CASE} = 25^{\circ}\text{C}, V_{IN} = 1.2 \text{ V}$		4.7	pF

¹Specifications subject to change without notice.

²Applies to output and bidirectional pins: AD15-0, RD, WR, ALE, FLAG3-0, DAI_Px, SPICLK, MOSI, MISO, EMU, TDO, CLKOUT, XTAL.

³See Output Drive Currents on Page 37 for typical drive current capabilities.

⁴Applies to input pins: <u>SPIDS</u>, BOOT_CFGx, CLK_CFGx, TCK, <u>RESET</u>, CLKIN.

⁵ Applies to input pins with 22.5 k Ω internal pull-ups: TRST, TMS, TDI.

⁶Applies to three-statable pins: FLAG3–0.

 7 Applies to three-statable pins with 22.5 k Ω pull-ups: AD15–0, DAI_Px, SPICLK, MISO, MOSI.

⁸Applies to open-drain output pins: <u>EMU</u>, MISO, MOSI.

⁹Typical internal current data reflects nominal operating conditions.

¹⁰See Engineer-to-Engineer Note (EE-216) for further information.

¹¹Characterized, but not tested.

¹²Applies to all signal pins.

¹³Guaranteed, but not tested.

Power-Up Sequencing

The timing requirements for DSP startup are given in Table 15 and Figure 5. Note that during power-up, a leakage current of approximately 200 μ A may be observed on the RESET pin. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 15. Power-Up Sequencing (DSP Startup)

Parameter		Min	Мах	Unit
Timing Requirer	ments			
t _{RSTVDD}	RESET Low Before V _{DDINT} /V _{DDEXT} On	0		ns
t _{IVDDEVDD}	V _{DDINT} On Before V _{DDEXT}	-50	+200	ms
t _{CLKVDD}	CLKIN Valid After V _{DDINT} /V _{DDEXT} Valid ¹	0	200	ms
t _{CLKRST}	CLKIN Valid Before RESET Deasserted	10 ²		μs
t _{PLLRST}	PLL Control Setup Before RESET Deasserted	20 ³		μs
Switching Chard	acteristics			
tCONTRCT	DSP Core Reset Deasserted After RESET Deasserted	$4096 \times t_{cv}^{4, 5}$		

¹Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

² Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to the crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

³Based on CLKIN cycles.

⁴ Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for RESET to be held low in order to properly initialize and propagate default states at all I/O pins.

⁵The 4096 cycle count depends on t_{SRST} specification in Table 17. If setup time is not met, one additional CLKIN cycle can be added to the core reset time, resulting in 4097 cycles maximum.



Figure 5. Power-Up Sequencing

Clock Input

See Table 16 and Figure 6.

Table 16. Clock Input

			150 MHz ¹		200 MHz ²	
Paramet	er	Min	Max	Min	Max	Unit
Timing Re	equirements					
t _{CK}	CLKIN Period	20 ³	160 ⁴	15 ³	160 ⁴	ns
t _{CKL}	CLKIN Width Low	7.5 ³	80 ⁴	6 ³	80 ⁴	ns
t _{CKH}	CLKIN Width High	7.5 ³	80 ⁴	6 ³	80 ⁴	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3	ns
f _{vco} ⁵	VCO Frequency	200	800	200	800	MHz
t _{CCLK}	CCLK Period ⁶	6.66	10	5	10	ns

¹Applies to all 150 MHz models. See Ordering Guide on Page 45.

² Applies to all 200 MHz models. See Ordering Guide on Page 45.

³ Applies only for CLK_CFG1-0 = 00 and default values for PLL control bits in PMCTL.

⁴Applies only for CLK_CFG1-0 = 01 and default values for PLL control bits in PMCTL.

⁵See Figure 4 on Page 16 for VCO diagram.

⁶Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.





Clock Signals

The ADSP-2126x can use an external clock or a crystal. See CLKIN pin description. The programmer can configure the ADSP-2126x to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode. Note that the 200 MHz clock rate is achieved using a 12.5 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN).



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. CRYSTAL SELECTION MUST COMPLY WITH CLKCFG1-0 = 10 OR = 01.

Figure 7. 150 MHz or 200 MHz Operation with a 12.5 MHz Fundamental Mode Crystal

Timer WDTH_CAP Timing

The timing specification in Table 21 and Figure 12 applies to Timer in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DAI_P20-1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20-1 pins.

Table 21. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requiren	nents			
t _{PWI}	Timer Pulse Width	$2 \times t_{CCLK}$	$2(2^{31}-1) \times t_{CCLK}$	ns



Figure 12. Timer Width Capture Timing

DAI Pin-to-Pin Direct Routing

See Table 22 and Figure 13 for direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 22. DAI Pin-to-Pin Routing

Parameter		Min	Мах	Unit
Timing Requirer	nents			
t _{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	10	ns



Figure 13. DAI Pin-to-Pin Direct Routing

Memory Read—Parallel Port

The specifications in Table 25, Table 26, Figure 16, and Figure 17 are for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-2126x is accessing external memory space.

Table 25. 8-Bit Memory Read Cycle

Parameter		Min	Мах	Unit
Timing Requ	lirements			
t _{DRS}	Address/Data 7–0 Setup Before RD High	3.3		ns
t _{DRH}	Address/Data 7–0 Hold After RD High	0		ns
t _{DAD}	Address 15–8 to Data Valid		$D+0.5\times t_{\text{CCLK}}-3.5$	ns
Switching Cl	haracteristics			
t _{ALEW}	ALE Pulse Width	$2 \times t_{CCLK} - 2$		ns
t _{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 0.5$		ns
t _{ADAS} ¹	Address/Data 15-0 Setup Before ALE Deasserted	$2.5 imes t_{CCLK} - 2.0$		ns
t _{adah} 1	Address/Data 15-0 Hold After ALE Deasserted	$0.5 imes t_{CCLK} - 0.8$		ns
t _{ALEHZ} 1	ALE Deasserted to Address/Data7–0 in High-Z	$0.5 imes t_{CCLK} - 0.8$	$0.5 imes t_{CCLK} + 2.0$	ns
t _{RW}	RD Pulse Width	D – 2		ns
t _{ADRH}	Address/Data 15–8 Hold After RD High	$0.5 \times t_{CCLK} - 1 + H$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) \times $t_{\mbox{\tiny CCLK}}$

 $H = t_{CCLK}$ (if a hold cycle is specified, else H = 0)

¹On reset, ALE is an active high cycle. However, it can be reconfigured by software to be active low.



Figure 16. 8-Bit Memory Read Cycle

Memory Write—Parallel Port

Use the specifications in Table 27, Table 28, Figure 18, and Figure 19 for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-2126x is accessing external memory space.

Table 27. 8-Bit Memory Write Cycle

Parameter		Min	Max	Unit
Switching Chara	cteristics			
t _{ALEW}	ALE Pulse Width	$2 \times t_{CCLK} - 2$		ns
t _{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 0.5$		ns
t _{ADAS} ¹	Address/Data 15-0 Setup Before ALE Deasserted	$2.5 imes t_{CCLK} - 2.0$		ns
t _{ADAH} 1	Address/Data 15–0 Hold After ALE Deasserted	$0.5 imes t_{CCLK} - 0.8$		ns
t _{ww}	WR Pulse Width	D – 2		ns
t _{ADWL}	Address/Data 15–8 to WR Low	$0.5 imes t_{CCLK} - 1.5$		ns
t _{ADWH}	Address/Data 15–8 Hold After WR High	$0.5 imes t_{CCLK} - 1 + H$		ns
t _{ALEHZ}	ALE Deasserted to Address/Data 15-0 in High-Z	$0.5 imes t_{CCLK} - 0.8$	$0.5 imes t_{CCLK} + 2.0$	ns
t _{DWS}	Address/Data 7–0 Setup Before WR High	D		ns
t _{DWH}	Address/Data 7–0 Hold After WR High	$0.5 \times t_{CCLK} - 1.5 + H$		ns
t _{DAWH}	Address/Data to WR High	D		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) \times $t_{\mbox{\tiny CCLK}}$

 $H = t_{CCLK}$ (if a hold cycle is specified, else H = 0)

¹On reset, ALE is an active high cycle. However, it can be reconfigured by software to be active low.



Figure 18. 8-Bit Memory Write Cycle

Serial Ports

To determine whether communication is possible between two devices at a given clock speed, the specifications in Table 29, Table 30, Table 31, Table 32, Figure 20, Figure 21, and Figure 22 must be confirmed: 1) frame sync delay and frame sync setup and hold; 2) data delay and data setup and hold; and 3) SCLK width. Serial port signals (SCLK, FS, DxA,/DxB) are routed to the DAI_P20-1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20-1 pins.

Table 29. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirem	ents (Contraction of the contraction of the contrac			
t _{sfse}	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode) ¹	2.5		ns
t _{HFSE}	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode) ¹	2.5		ns
t _{SDRE}	Receive Data Setup Before Receive SCLK ¹	2.5		ns
t _{HDRE}	Receive Data Hold After SCLK ¹	2.5		ns
t _{sclkw}	SCLK Width	7		ns
t _{SCLK}	SCLK Period	20		ns
Switching Chara	cteristics			
t _{DFSE}	FS Delay After SCLK (Internally Generated FS in Either Transmit or Receive Mode) ²		7	ns
t _{HOFSE}	FS Hold After SCLK (Internally Generated FS in Either Transmit or Receive Mode) ²	2		ns
t _{DDTE}	Transmit Data Delay After Transmit SCLK ²		7	ns
t _{HDTE}	Transmit Data Hold After Transmit SCLK ²	2		ns

¹Referenced to sample edge.

 $^2 \rm Referenced$ to drive edge.

Table 30. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Require	ments			
t _{SFSI}	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode) ¹	6		ns
t _{HFSI}	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode) ¹	1.5		ns
t _{sDRI}	Receive Data Setup Before SCLK ¹	6		ns
t _{HDRI}	Receive Data Hold After SCLK ¹	1.5		ns
Switching Char	acteristics			
t _{DFSI}	FS Delay After SCLK (Internally Generated FS in Transmit Mode) ²		3	ns
t _{HOFSI}	FS Hold After SCLK (Internally Generated FS in Transmit Mode) ²	-1.0		ns
t _{DFSI}	FS Delay After SCLK (Internally Generated FS in Receive Mode) ²		3	ns
t _{HOFSI}	FS Hold After SCLK (Internally Generated FS in Receive Mode) ²	-1.0		ns
t _{DDTI}	Transmit Data Delay After SCLK ²		3	ns
t _{HDTI}	Transmit Data Hold After SCLK ²	-1.0		ns
t _{sclkiw}	Transmit or Receive SCLK Width	0.5t _{SCLK} – 2	0.5t _{SCLK} + 2	ns

¹Referenced to the sample edge.

²Referenced to drive edge.



DATA TRANSMIT-INTERNAL CLOCK







Figure 20. Serial Ports

SPI Interface Protocol—Slave

Table 36. SPI Interface Protocol—Slave

Parameter		Min	Max	Unit
Timing Requirements				
t _{SPICLKS}	Serial Clock Cycle	$4 \times t_{CCLK}$		ns
t _{SPICHS}	Serial Clock High Period	$2 \times t_{CCLK} - 2$		ns
t _{SPICLS}	Serial Clock Low Period	$2 \times t_{CCLK} - 2$		ns
t _{SDSCO}	SPIDS Assertion to First SPICLK Edge CPHASE = 0 CPHASE = 1	$2 \times t_{CCLK} + 1$ $2 \times t_{CCLK} + 1$		ns
t _{HDS}	Last SPICLK Edge to \overline{SPIDS} Not Asserted CPHASE = 0	$2 \times t_{CCLK}$		ns
t _{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2		ns
t _{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t _{SDPPW}	$\overline{\text{SPIDS}}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{CCLK}$		ns
Switching Characteris	tics			
t _{DSOE}	SPIDS Assertion to Data Out Active	0	5	ns
t _{DSDHI}	SPIDS Deassertion to Data High Impedance	0	5	ns
t _{DDSPIDS}	SPICLK Edge to Data Out Valid (Data Out Delay Time)		7.5	ns
t _{HDSPIDS}	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{CCLK} - 2$		ns
t _{DSOV}	$\overline{\text{SPIDS}}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{\text{CCLK}} + 2$	ns



Figure 26. SPI Interface Protocol—Slave

OUTLINE DIMENSIONS

The ADSP-2126x is available in a 144-lead LQFP package and a 136-ball BGA package shown in Figure 35 and Figure 36.



COMPLIANT TO JEDEC STANDARDS MS-026-BFB

Figure 35. 144-Lead Low Profile Flat Package [LQFP] (ST-144) Dimensions shown in millimeters



Figure 36. 136-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-136-1) Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 42 is provided as an aide to PCB design. For industry-
standard design recommendations, refer to IPC-7351, Generic
Requirements for Surface-Mount Design and Land Pattern
Standard.

Table 42.	BGA	_ED Data	for Use	with	Surface	-Mount	Design
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Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
136-Ball CSP_BGA (BC-136-1)	Solder Mask Defined (SMD)	0.4 mm	0.53 mm

AUTOMOTIVE PRODUCTS

The ADSP-21261W and ADSP-21262W are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

ORDERING GUIDE

Analog Devices offers a wide variety of audio algorithms and combinations to run on the ADSP-21266 DSP. For a complete list, visit our website at www.analog.com/SHARC.

Model	Notes	Temperature Range ¹	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21261SKBCZ150	2	0°C to +70°C	150 MHz	1M bit	3M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21261SKSTZ150	2	0°C to +70°C	150 MHz	1M bit	3M bit	144-Lead LQFP	ST-144
ADSP-21262SBBC-150		–40°C to +85°C	150 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21262SBBCZ150	2	–40°C to +85°C	150 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21262SKBC-200		0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21262SKBCZ200	2	0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21262SKSTZ200	2	0°C to +70°C	200 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKSTZ-1B	2, 3	0°C to +70°C	150 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKSTZ-2B	2, 3	0°C to +70°C	200 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKBCZ-2B	2, 3	0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21266SKSTZ-1C	2, 4	0°C to +70°C	150 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKSTZ-2C	2, 4	0°C to +70°C	200 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKBCZ-2C	2, 4	0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21266SKSTZ-1D	2, 4	0°C to +70°C	150 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKSTZ-2D	2, 4	0°C to +70°C	200 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKBCZ-2D	2, 4	0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1

¹Referenced temperature is ambient temperature.

 $^{2}Z = RoHS$ Compliant Part.

³B at end of part number indicates Rev. 0.1 silicon. See Table 3 on Page 4 for multichannel surround sound decoder algorithms in on-chip B ROM.

⁴C and D at end of part number indicate Rev. 0.2 silicon. See Table 3 on Page 4 for multichannel surround sound decoder algorithms in on-chip C and D ROM.