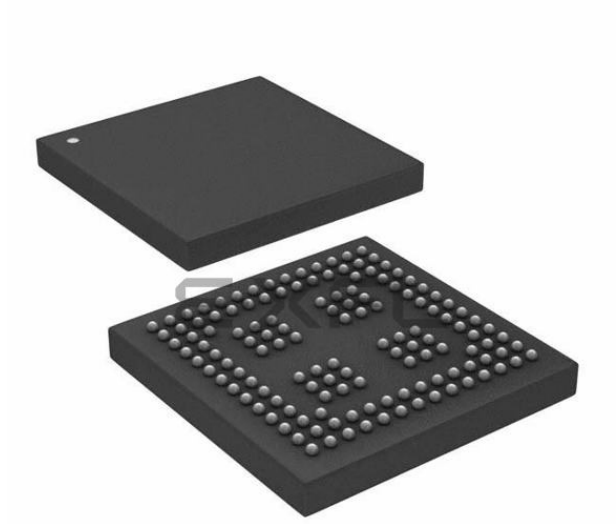

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	136-LFBGA, CSPBGA
Supplier Device Package	136-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21262skbc-200

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REVISION HISTORY

12/12—Rev. F to Rev. G

Corrected Long Word Memory Space in Table 4 in Memory and I/O Interface Features 4

Updated Development Tools 8

Added section, Related Signal Chains 9

Changed the package designator in Figure 36 from BC-136 to BC-136-1. This change in no way affects form, fit, or function. See Outline Dimensions 43

Updated Ordering Guide 45

elements, but each processing element operates on different data. This architecture is efficient at executing math intensive audio algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2126x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2126x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on Page 1). With the ADSP-2126x's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2126x includes an on-chip instruction cache that enables three-bus operation to fetch an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The ADSP-2126x's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-2126x contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the ADSP-2126x can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-2126x adds the following architectural features to the SIMD SHARC family core:

Dual-Ported On-Chip Memory

The ADSP-21262 and ADSP-21266 contain two megabits of internal SRAM and four megabits of internal mask-programmable ROM. The ADSP-21261 contain one megabit of internal SRAM and three megabits of internal mask-programmable ROM. Each block can be configured for different combinations of code and data storage (see memory maps, Table 4 and Table 5). Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory, in combination with three separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

The ADSP-2126x is available with a variety of multichannel surround sound decoders, preprogrammed in ROM memory. Table 3 shows the configuration of decoder algorithms.

Table 3. Multichannel Surround Sound Decoder Algorithms in On-Chip ROM

Algorithms	B ROM	C ROM	D ROM
PCM	Yes	Yes	Yes
AC-3	Yes	Yes	Yes
DTS 96/24	v2.2	v2.3	v2.3
AAC (LC)	Yes	Yes	Coefficients only
WMAPRO 7.1 96 KHz	No	No	Yes
MPEG2 BC 2ch	Yes	Yes	No
Noise	Yes	Yes	Yes
DPL2x/EX	DPL2	Yes	Yes
Neo:6/ES (v2.5046)	Yes	Yes	Yes

Serial Peripheral (Compatible) Interface

The serial peripheral interface is an industry-standard synchronous serial link, enabling the ADSP-2126x SPI-compatible port to communicate with other SPI-compatible devices. SPI is an interface consisting of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-2126x SPI-compatible peripheral implementation also features programmable baud rates at up to 50 MHz for a core clock of 200 MHz and up to 37.5 MHz for a core clock of 150 MHz, clock phases, and polarities. The ADSP-2126x SPI-compatible port uses open-drain drivers to support a multimaster configuration and to avoid data contention.

Parallel Port

The parallel port provides interfaces to SRAM and peripheral devices. The multiplexed address and data pins (AD15–0) can access 8-bit devices with up to 24 bits of address, or 16-bit devices with up to 16 bits of address. In either mode, 8- or 16-bit, the maximum data transfer rate is one-third the core clock speed. As an example, a clock rate of 200 MHz is equivalent to 66M byte/sec, and a clock rate of 150 MHz is equivalent to 50M byte/sec.

DMA transfers are used to move data to and from internal memory. Access to the core is also facilitated through the parallel port register read/write functions. The $\overline{RD}$, $\overline{WR}$, and ALE (address latch enable) pins are the control pins for the parallel port.

Timers

The ADSP-2126x has a total of four timers: a core timer able to generate periodic software interrupts, and three general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired output signal, and each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

ROM-Based Security

The ADSP-2126x has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the DSP does not boot-load any external code, executing exclusively from internal SRAM/ROM. Additionally, the DSP is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or test access port, will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

Program Booting

The internal memory of the ADSP-2126x boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins.

Phase-Locked Loop

The ADSP-2126x uses an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK_CFG1–0 pins are used to select ratios of 16:1, 8:1, and 3:1. After booting, numerous other ratios can be selected via software control. The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 2, 4, 8, and 16.

Power Supplies

The ADSP-2126x has separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the ADSP-2126x's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 2. (A recommended ferrite chip is the muRata BLM18AG102SN1D). To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 2 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

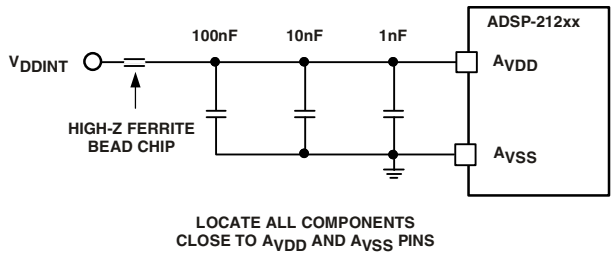


Figure 2. Analog Power Filter Circuit

PIN FUNCTION DESCRIPTIONS

The ADSP-2126x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

DAI_Px, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS,$\overline{\text{TRST}}$, TDI and AD15–0 (NOTE: These pins have internal pull-up resistors.)

The following symbols appear in the Type column of Table 6: A = asynchronous, G = ground, I = input, O = output, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, and T = three-state.

Table 6. Pin Descriptions

Pin	Type	State During and After Reset	Function
AD15–0	I/O/T	Rev. 0.1 silicon—AD15–0 pins are driven low both during and after reset. Rev. 0.2 silicon—AD15–0 pins are three-stated and pulled high both during and after reset.	**Parallel Port Address/Data.** The parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 kΩ internal pull-up resistor. See Address Data Modes on Page 13 for details of the AD pin operation. For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, A23–8; ALE is used in conjunction with an external latch to retain the values of the A23–8. For 16-bit mode: ALE is automatically asserted whenever a change occurs in the address bits, A15–0; ALE is used in conjunction with an external latch to retain the values of the A15–0. To use these pins as flags (FLAG15–0), set (= 1) Bit 20 of the SYSCTL register and disable the parallel port. See Table 7 on Page 13 for a list of how the AD15–0 pins map to the flag pins. When configured in the IDP_PDAP_CTL register, the IDP Channel 0 can use these pins for parallel input data.
$\overline{\text{RD}}$	O	Output only, driven high[1]	**Parallel Port Read Enable.** $\overline{\text{RD}}$ is asserted low whenever the DSP reads 8-bit or 16-bit data from an external memory device. When AD15–0 are flags, this pin remains deasserted.
$\overline{\text{WR}}$	O	Output only, driven high[1]	**Parallel Port Write Enable.** $\overline{\text{WR}}$ is asserted low whenever the DSP writes 8-bit or 16-bit data to an external memory device. When AD15–0 are flags, this pin remains deasserted.
ALE	O	Output only, driven low[1]	**Parallel Port Address Latch Enable.** ALE is asserted whenever the DSP drives a new address on the parallel port address pin. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15–0 are flags, this pin remains deasserted.
FLAG3–0	I/O/A	Three-state	**Flag Pins.** Each FLAG pin is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals. These pins can be used as an SPI interface slave select output during SPI mastering. These pins are also multiplexed with the $\overline{\text{IRQx}}$ and the TIMEXP signals. In SPI master boot mode, FLAG0 is the slave select pin that must be connected to an SPI EPROM. FLAG0 is configured as a slave select during SPI master boot. When Bit 16 is set (= 1) in the SYSCTL register, FLAG0 is configured as $\overline{\text{IRQ0}}$. When Bit 17 is set (= 1) in the SYSCTL register, FLAG1 is configured as $\overline{\text{IRQ1}}$. When Bit 18 is set (= 1) in the SYSCTL register, FLAG2 is configured as $\overline{\text{IRQ2}}$. When Bit 19 is set (= 1) in the SYSCTL register, FLAG3 is configured as TIMEXP, which indicates that the system timer has expired.
DAI_P20–1	I/O/T	Three-state with programmable pull-up	**Digital Application Interface Pins**. These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the SRU can be routed to any of these pins. The SRU provides the connection from the serial ports, input data port, precision clock generators, and timers to the DAI_P20–1 pins. These pins have internal 22.5 kΩ pull-up resistors which are enabled on reset. These pull-ups can be disabled in the DAI_PIN_PULLUP register.

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
CLK_CFG1–0	I	Input only	**Core/CLKIN Ratio Control**. These pins set the start up clock frequency. See Table 9 for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
$\overline{\text{RESETOUT}}$	O	Output only	**Reset Out**. Drives out the core reset signal to an external device.
$\overline{\text{RESET}}$	I/A	Input only	**Processor Reset**. Resets the ADSP-2126x to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Input only[3]	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2126x.
TMS	I/S	Three-state with pull-up enabled	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TDI	I/S	Three-state with pull-up enabled	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 22.5 kΩ internal pull-up resistor.
TDO	O	Three-state[4]	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Three-state with pull-up enabled	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2126x. $\overline{\text{TRST}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	Three-state with pull-up enabled	**Emulation Status**. Must be connected to the ADSP-2126x Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 kΩ internal pull-up resistor.
V_{DDINT}	P		**Core Power Supply**. Nominally +1.2 V dc and supplies the DSP's core processor (13 pins on the BGA package, 32 pins on the LQFP package).
V_{DDEXT}	P		**I/O Power Supply**. Nominally +3.3 V dc (6 pins on the BGA package, 10 pins on the LQFP package).
A_{VDD}	P		**Analog Power Supply**. Nominally +1.2 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 7.
A_{VSS}	G		**Analog Power Supply Return**.
GND	G		**Power Supply Return**. (54 pins on the BGA package, 39 pins on the LQFP package).

[1] $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE are continuously driven by the DSP and will not be three-stated.
[2] Output only is a three-state driver with its output path always enabled.
[3] Input only is a three-state driver, with both output path and pull-up disabled.
[4] Three-state is a three-state driver, with pull-up disabled.

Clock Input

See Table 16 and Figure 6.

Table 16. Clock Input

Parameter		150 MHz[1] Min	150 MHz[1] Max	200 MHz[2] Min	200 MHz[2] Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	20[3]	160[4]	15[3]	160[4]	ns
t_{CKL}	CLKIN Width Low	7.5[3]	80[4]	6[3]	80[4]	ns
t_{CKH}	CLKIN Width High	7.5[3]	80[4]	6[3]	80[4]	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3	ns
f_{VCO}[5]	VCO Frequency	200	800	200	800	MHz
t_{CCLK}	CCLK Period[6]	6.66	10	5	10	ns

[1] Applies to all 150 MHz models. See Ordering Guide on Page 45.
[2] Applies to all 200 MHz models. See Ordering Guide on Page 45.
[3] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[4] Applies only for CLK_CFG1–0 = 01 and default values for PLL control bits in PMCTL.
[5] See Figure 4 on Page 16 for VCO diagram.
[6] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

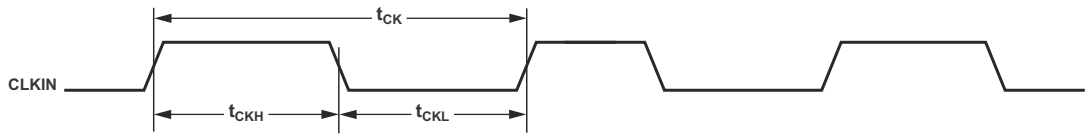
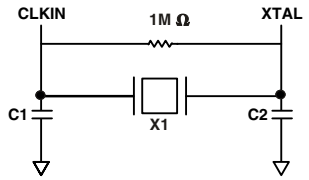


Figure 6. Clock Input

Clock Signals

The ADSP-2126x can use an external clock or a crystal. See CLKIN pin description. The programmer can configure the ADSP-2126x to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode. Note that the 200 MHz clock rate is achieved using a 12.5 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN).



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. CRYSTAL SELECTION MUST COMPLY WITH CLKCFG1-0 = 10 OR = 01.

Figure 7. 150 MHz or 200 MHz Operation with a 12.5 MHz Fundamental Mode Crystal

Reset

See Table 17 and Figure 8.

Table 17. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable VDD and CLKIN (not including start-up time of external clock oscillator).

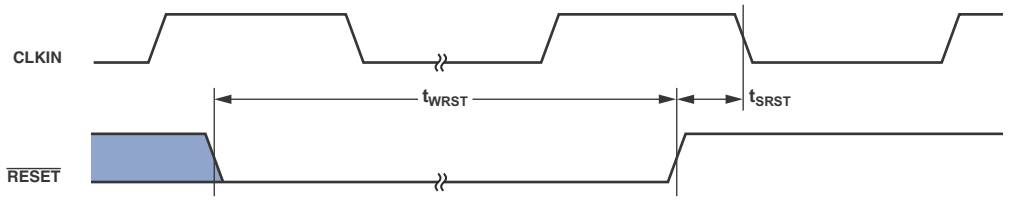


Figure 8. Reset

Interrupts

The timing specification in Table 18 and Figure 9 applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts. Also applies to DAI_P20–1 pins when configured as interrupts.

Table 18. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2\ t_{CCLK} + 2$		ns

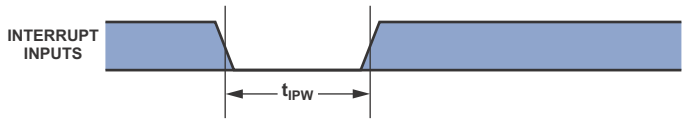


Figure 9. Interrupts

Core Timer

The timing specification in Table 19 and Figure 10 applies to FLAG3 when it is configured as the core timer (CTIMER).

Table 19. Core Timer

Parameter		Min	Max	Unit
Switching Characteristics				
t_{WCTIM}	CTIMER Pulse Width	$4 \times t_{CCLK} - 1$		ns

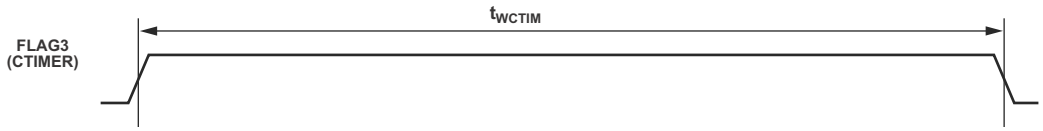


Figure 10. Core Timer

Timer PWM_OUT Cycle Timing

The timing specification in Table 20 and Figure 11 applies to Timer in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 20. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{CCLK} - 1$	$2(2^{31} - 1) \times t_{CCLK}$	ns

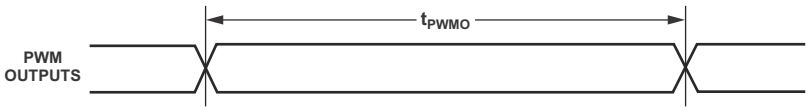


Figure 11. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The timing specification in Table 21 and Figure 12 applies to Timer in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 21. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PWI}	Timer Pulse Width	$2 \times t_{CCLK}$	$2(2^{31} - 1) \times t_{CCLK}$	ns

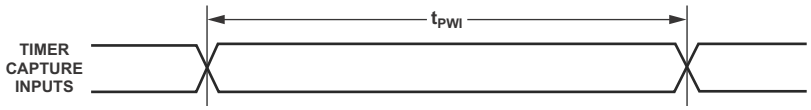


Figure 12. Timer Width Capture Timing

DAI Pin-to-Pin Direct Routing

See Table 22 and Figure 13 for direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 22. DAI Pin-to-Pin Routing

Parameter		Min	Max	Unit
Timing Requirements				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	10	ns

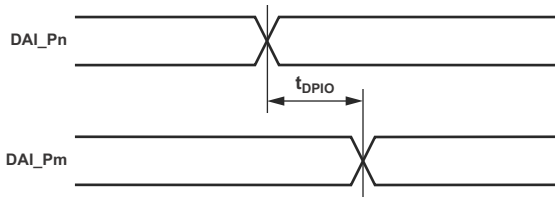


Figure 13. DAI Pin-to-Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

The timing in Table 23 and Figure 14 is valid only when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P07–DAI_P20).

Table 23. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Pulse Width	20		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	2		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	2		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock Falling Edge	2.5	10	ns
t_{DTRIG}	PCG Output Clock and Frame Sync Delay After PCG Trigger	$2.5 + 2.5 \times t_{PCGOW}$	$10 + 2.5 \times t_{PCGOW}$	ns
t_{PCGOW}	Output Clock Pulse Width	40		ns

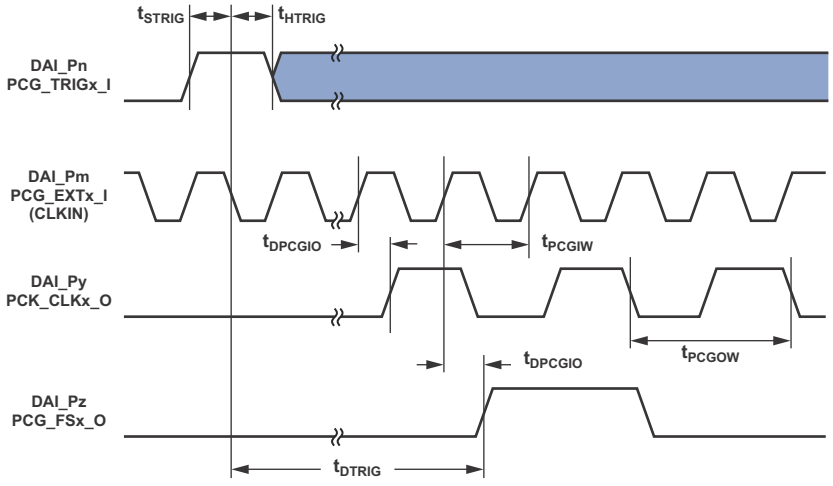


Figure 14. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications in Table 24 and Figure 15 apply to the FLAG3–0 and DAI_P20–1 pins, the parallel port, and the serial peripheral interface. See Table 6 on Page 10 for more information on flag use.

Table 24. Flags

Parameter		Min	Max	Unit
Timing Requirements				
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{CCLK} + 3$		ns
Switching Characteristics				
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{CCLK} - 1$		ns

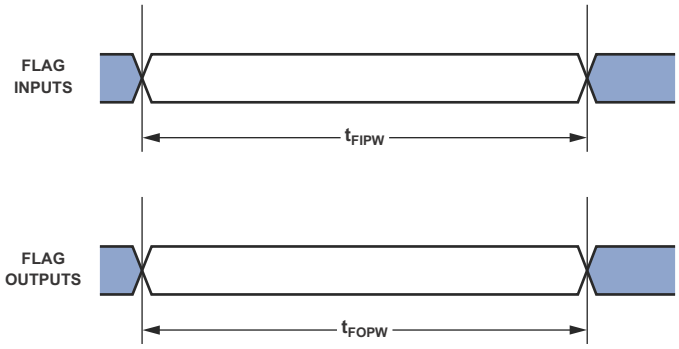


Figure 15. Flags

Memory Read—Parallel Port

The specifications in Table 25, Table 26, Figure 16, and Figure 17 are for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-2126x is accessing external memory space.

Table 25. 8-Bit Memory Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{DRS}	Address/Data 7–0 Setup Before $\overline{RD}$ High	3.3		ns
t_{DRH}	Address/Data 7–0 Hold After $\overline{RD}$ High	0		ns
t_{DAD}	Address 15–8 to Data Valid		$D + 0.5 \times t_{CCLK} - 3.5$	ns
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{CCLK} - 2$		ns
t_{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 0.5$		ns
t_{ADAS}[1]	Address/Data 15–0 Setup Before ALE Deasserted	$2.5 \times t_{CCLK} - 2.0$		ns
t_{ADAH}1	Address/Data 15–0 Hold After ALE Deasserted	$0.5 \times t_{CCLK} - 0.8$		ns
t_{ALEHZ}[1]	ALE Deasserted to Address/Data7–0 in High-Z	$0.5 \times t_{CCLK} - 0.8$	$0.5 \times t_{CCLK} + 2.0$	ns
t_{RW}	$\overline{RD}$ Pulse Width	D – 2		ns
t_{ADRH}	Address/Data 15–8 Hold After $\overline{RD}$ High	$0.5 \times t_{CCLK} - 1 + H$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{CCLK}
H = t_{CCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be reconfigured by software to be active low.

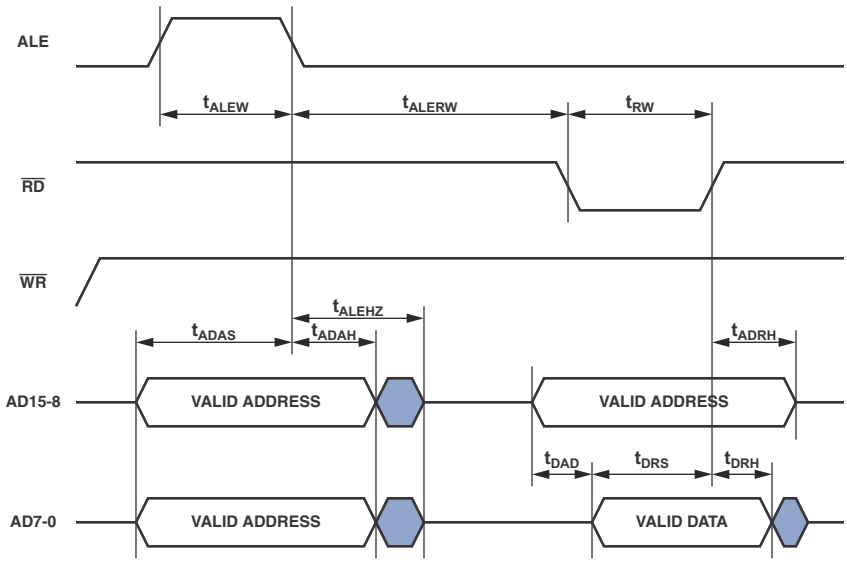


Figure 16. 8-Bit Memory Read Cycle

Table 28. 16-Bit Memory Write Cycle

Parameter		Min	Max	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{CCLK} - 2$		ns
t_{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 0.5$		ns
t_{ADAS}[1]	Address/Data 15–0 Setup Before ALE Deasserted	$2.5 \times t_{CCLK} - 2.0$		ns
t_{ADAH}[1]	Address/Data 15–0 Hold After ALE Deasserted	$0.5 \times t_{CCLK} - 0.8$		ns
t_{WW}	$\overline{WR}$ Pulse Width	D – 2		ns
t_{ALEHZ}[1]	ALE Deasserted to Address/Data 15–0 in High-Z	$0.5 \times t_{CCLK} - 0.8$	$0.5 \times t_{CCLK} + 2.0$	ns
t_{DWS}	Address/Data 15–0 Setup Before $\overline{WR}$ High	D		ns
t_{DWH}	Address/Data 15–0 Hold After $\overline{WR}$ High	$0.5 \times t_{CCLK} - 1.5 + H$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{CCLK}
H = t_{CCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be reconfigured by software to be active low.

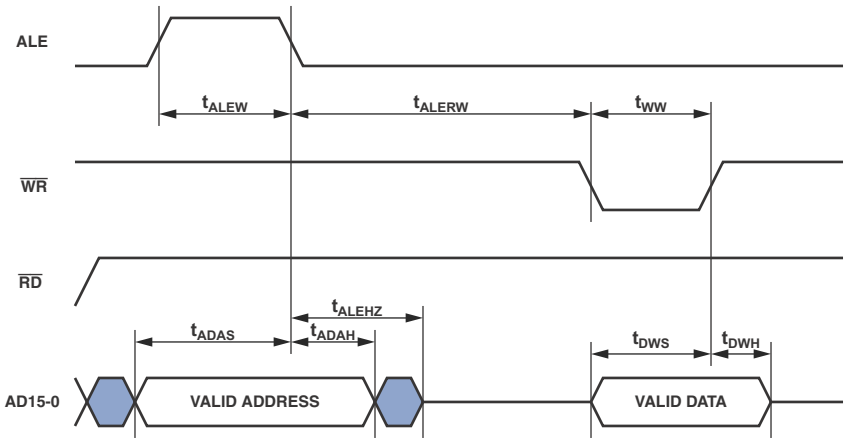


Figure 19. 16-Bit Memory Write Cycle

Table 32. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		7	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair mode as well as DSP serial mode, and MCE = 1, MFD = 0.

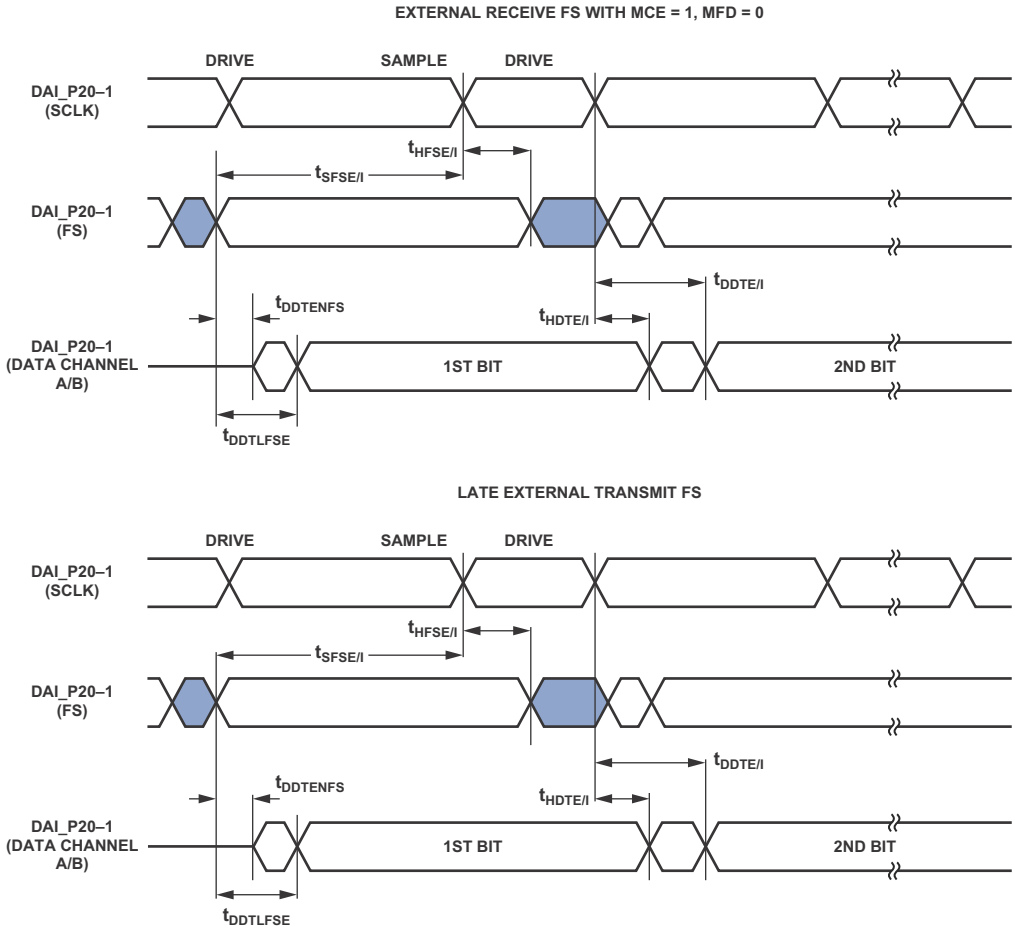


Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 33 and Figure 23. IDP Signals (SCLK, FS, SDATA) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 33. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}	FS Setup Before SCLK Rising Edge[1]	2.5		ns
t_{SIHFS}	FS Hold After SCLK Rising Edge[1]	2.5		ns
t_{SISD}	SDATA Setup Before SCLK Rising Edge[1]	2.5		ns
t_{SIHD}	SDATA Hold After SCLK Rising Edge[1]	2.5		ns
$t_{IDPCLKW}$	Clock Width	7		ns
t_{IDPCLK}	Clock Period	20		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via the precision clock generators (PCG) or SPORTs. PCG input can be either CLKIN or any of the DAI pins.

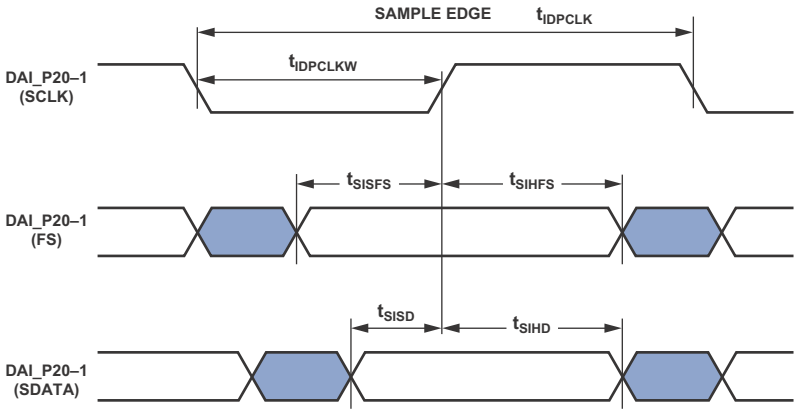


Figure 23. Input Data Port (IDP)

JTAG Test Access Port and Emulation

Table 37. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	8		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		10	ns

[1] System Inputs = AD15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, $\overline{\text{BOOT\_CFG1–0}}$, MISO, MOSI, SPICLK, DAI_Px, FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, AD15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, CLKOUT, $\overline{\text{EMU}}$, ALE.

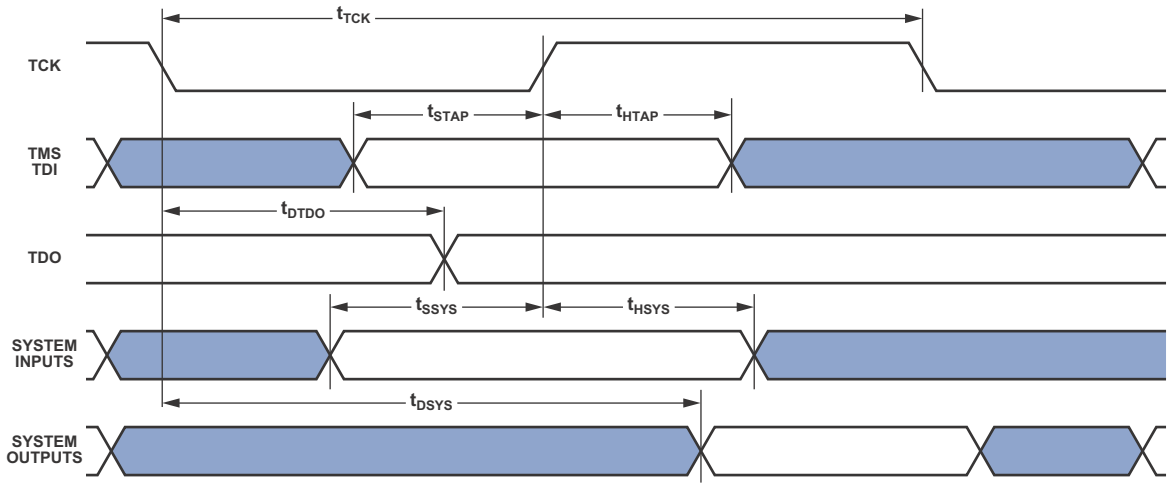


Figure 27. JTAG Test Access Port and Emulation

136-BALL BGA PIN CONFIGURATIONS

Table 41 shows the ADSP-2126x's pin names and their default function after reset (in parentheses). Figure 34 on Page 42 shows the BGA package pin assignments.

Table 41. 136-Ball BGA Pin Assignments

Pin Name	BGA Pin No.	Pin Name	BGA Pin No.	Pin Name	BGA Pin No.	Pin Name	BGA Pin No.
CLK_CFG0	A01	CLK_CFG1	B01	BOOT_CFG1	C01	V_{DDINT}	D01
XTAL	A02	GND	B02	BOOT_CFG0	C02	GND	D02
TMS	A03	V_{DDEXT}	B03	GND	C03	GND	D04
TCK	A04	CLKIN	B04	GND	C12	GND	D05
TDI	A05	$\overline{TRST}$	B05	GND	C13	GND	D06
$\overline{RESETOUT}$	A06	A_{VSS}	B06	V_{DDINT}	C14	GND	D09
TDO	A07	A_{VDD}	B07			GND	D10
$\overline{EMU}$	A08	V_{DDEXT}	B08			GND	D11
MOSI	A09	SPICLK	B09			GND	D13
MISO	A10	$\overline{RESET}$	B10			V_{DDINT}	D14
$\overline{SPIDS}$	A11	V_{DDINT}	B11				
V_{DDINT}	A12	GND	B12				
GND	A13	GND	B13				
GND	A14	GND	B14				
V_{DDINT}	E01	FLAG1	F01	AD7	G01	AD6	H01
GND	E02	FLAG0	F02	V_{DDINT}	G02	V_{DDEXT}	H02
GND	E04	GND	F04	V_{DDEXT}	G13	DAI_P18 (SD5B)	H13
GND	E05	GND	F05	DAI_P19 (SCLK45)	G14	DAI_P17 (SD5A)	H14
GND	E06	GND	F06				
GND	E09	GND	F09				
GND	E10	GND	F10				
GND	E11	GND	F11				
GND	E13	FLAG2	F13				
FLAG3	E14	DAI_P20 (SFS45)	F14				

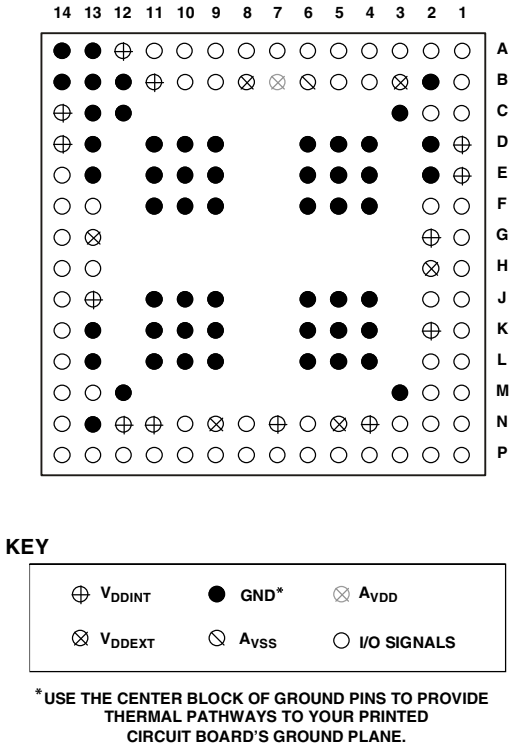
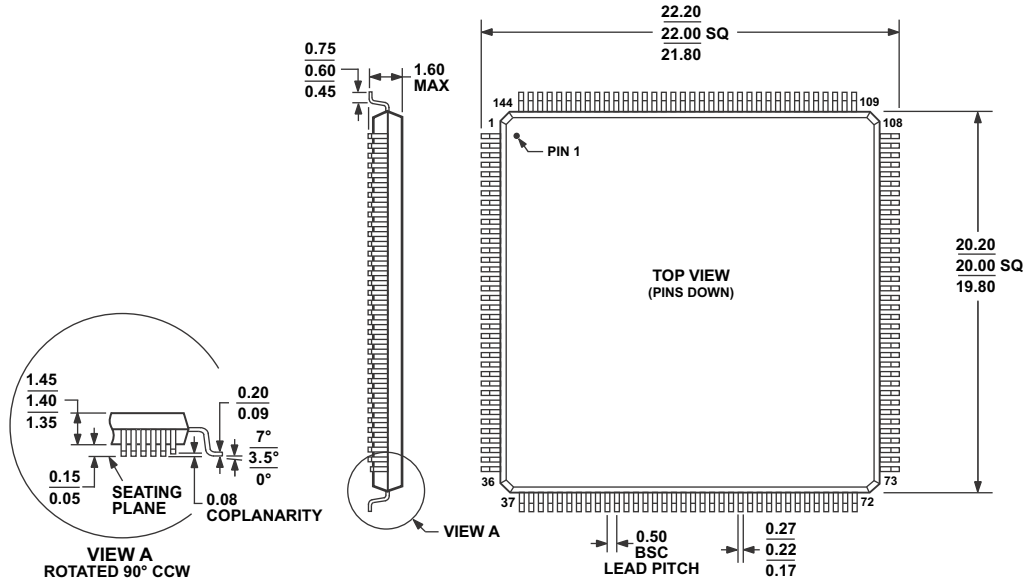


Figure 34. 136-Ball BGA Pin Assignments (Bottom View, Summary)

OUTLINE DIMENSIONS

The ADSP-2126x is available in a 144-lead LQFP package and a 136-ball BGA package shown in Figure 35 and Figure 36.



COMPLIANT TO JEDEC STANDARDS MS-026-BFB

Figure 35. 144-Lead Low Profile Flat Package [LQFP]
(ST-144)
Dimensions shown in millimeters