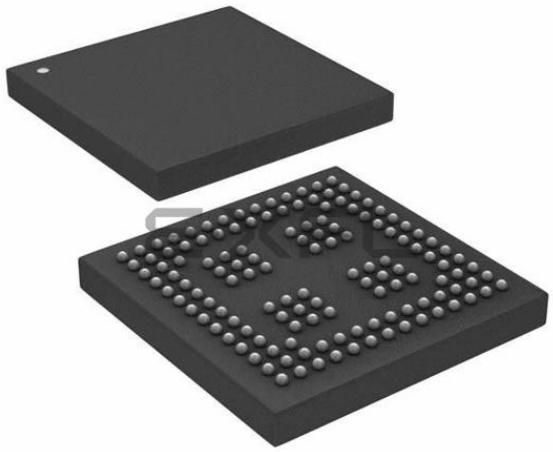

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	136-LFBGA, CSPBGA
Supplier Device Package	136-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21262skbcz200

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REVISION HISTORY

12/12—Rev. F to Rev. G

Corrected Long Word Memory Space in Table 4 in Memory and I/O Interface Features 4

Updated Development Tools 8

Added section, Related Signal Chains 9

Changed the package designator in Figure 36 from BC-136 to BC-136-1. This change in no way affects form, fit, or function. See Outline Dimensions 43

Updated Ordering Guide 45

GENERAL DESCRIPTION

The ADSP-21261/ADSP-21262/ADSP-21266 SHARC® DSPs are members of the SIMD SHARC family of DSPs featuring Analog Devices, Inc., Super Harvard Architecture. The ADSP-2126x is source code compatible with the ADSP-21160 and ADSP-21161 DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. Like other SHARC DSPs, the ADSP-2126x are 32-bit/40-bit floating-point processors optimized for high performance audio applications with dual-ported on-chip SRAM, mask-programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital application interface.

Table 1 shows performance benchmarks for the processors running at 200 MHz. Table 2 shows the features of the individual product offerings.

Table 1. Processor Benchmarks (at 200 MHz)

Benchmark Algorithm	Speed (at 200 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	61.3 µs
FIR Filter (per tap)[1]	3.3 ns
IIR Filter (per biquad)[1]	13.3 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	30 ns
[4×4] × [4×1]	53.3 ns
Divide (y/x)	20 ns
Inverse Square Root	30 ns

[1] Assumes two files in multichannel SIMD mode.

As shown in the functional block diagram in Figure 1 on Page 1, the ADSP-2126x uses two computational units to deliver a 5 to 10 times performance increase over previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-2126x DSPs achieve an instruction cycle time of 5 ns at 200 MHz or 6.6 ns at 150 MHz. With its SIMD computational hardware, the ADSP-2126x can perform 1200 MFLOPS running at 200 MHz, or 900 MFLOPS running at 150 MHz.

Table 2. ADSP-2126x SHARC Processor Features

Feature	ADSP-21261	ADSP-21262	ADSP-21266
RAM	1M bit	2M bit	2M bit
ROM	3M bit	4M bit	4M bit
Audio Decoders in ROM[1]	No	No	Yes
DMA Channels	18	22	22
SPORTs	4	6	6
Package	136-ball BGA 144-lead LQFP	136-ball BGA 144-lead LQFP	136-ball BGA 144-lead LQFP

[1] For information on available audio decoding algorithms, see Table 3 on Page 4.

The ADSP-2126x continues the SHARC family's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include 2M bit dual-ported SRAM memory, 4M bit dual-ported ROM, an I/O processor that supports 22 DMA channels, six serial ports, an SPI interface, external parallel bus, and digital application interface.

The block diagram of the ADSP-2126x on Page 1 illustrates the following architectural features:

- Two processing elements, each containing an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Three programmable interval timers with PWM generation, PWM capture/pulse width measurement, and external event counter capabilities
- On-chip dual-ported SRAM (up to 2M bit)
- On-chip dual-ported, mask-programmable ROM (up to 4M bit)
- JTAG test access port
- 8- or 16-bit parallel port that supports interfaces to off-chip memory peripherals
- DMA controller
- Six full-duplex serial ports (four on the ADSP-21261)
- SPI-compatible interface
- Digital application interface that includes two precision clock generators (PCG), an input data port (IDP), six serial ports, eight serial interfaces, a 20-bit synchronous parallel input port, 10 interrupts, six flag outputs, six flag inputs, three programmable timers, and a flexible signal routing unit (SRU)

FAMILY CORE ARCHITECTURE

The ADSP-2126x is code compatible at the assembly level with the ADSP-2136x and ADSP-2116x, and with the first generation ADSP-2106x SHARC DSPs. The ADSP-2126x shares architectural features with the ADSP-2136x and ADSP-2116x SIMD SHARC family of DSPs, as detailed in the following sections.

SIMD Computational Engine

The ADSP-2126x contain two computational processing elements that operate as a single-instruction multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY can be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing

Table 5. Internal Memory Space (ADSP-21262/ADSP-21266)

IOP Registers 0x0000 0000–0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 SRAM 0x0004 0000–0x0004 3FFF	Block 0 SRAM 0x0008 0000–0x0008 5555	Block 0 SRAM 0x0008 0000–0x0008 7FFF	Block 0 SRAM 0x0010 0000–0x0010 FFFF
Reserved 0x0004 4000–0x0005 7FFF	Reserved	Reserved 0x0008 8000–0x000A FFFF	Reserved 0x0011 0000–0x0015 FFFF
Block 0 ROM 0x0005 8000–0x0005 FFFF	Block 0 ROM 0x000A 0000–0x000A AAAA	Block 0 ROM 0x000B 0000–0x000B FFFF	Block 0 ROM 0x0016 0000–0x0017 FFFF
Block 1 SRAM 0x0006 0000–0x0006 3FFF	Block 1 SRAM 0x000C 0000–0x000C 5555	Block 1 SRAM 0x000C 0000–0x000C 7FFF	Block 1 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0007 7FFF	Reserved	Reserved 0x000C 8000–0x000E FFFF	Reserved 0x0019 0000–0x001D FFFF
Block 1 ROM 0x0007 8000–0x0007 FFFF	Block 1 ROM 0x000E 0000–0x000E AAAA	Block 1 ROM 0x000F 0000–0x000F FFFF	Block 1 ROM 0x001E 0000–0x001F FFFF

Digital Application Interface (DAI)

The Digital application interface provides the ability to connect various peripherals to any of the SHARC DSP's DAI pins (DAI_P20–1).

Connections are made using the signal routing unit (SRU, shown in the block diagram on Page 1).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes six serial ports, two precision clock generators (PCGs), an input data port (IDP), six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2126x core, configurable as either eight channels of I^2S or serial data, or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the ADSP-2126x's serial ports.

For complete information on using the DAI, see the *ADSP-2126x SHARC DSP Peripherals Manual*.

Serial Ports

The ADSP-2126x features six full duplex synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as the Analog Devices AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has its own dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

The serial ports operate at up to one-quarter of the DSP core clock rate, providing each with a maximum data rate of 50M bits/sec for a 200 MHz core and 37.5M bits/sec for a 150 MHz core. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle, two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample-pair and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs) with two data pins, allowing four left-justified sample-pair or I^2S channels (using two stereo devices) per serial port with a maximum of up to 24 audio channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

PIN FUNCTION DESCRIPTIONS

The ADSP-2126x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

DAI_Px, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS,$\overline{\text{TRST}}$, TDI and AD15–0 (NOTE: These pins have internal pull-up resistors.)

The following symbols appear in the Type column of Table 6: A = asynchronous, G = ground, I = input, O = output, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, and T = three-state.

Table 6. Pin Descriptions

Pin	Type	State During and After Reset	Function
AD15–0	I/O/T	Rev. 0.1 silicon—AD15–0 pins are driven low both during and after reset. Rev. 0.2 silicon—AD15–0 pins are three-stated and pulled high both during and after reset.	**Parallel Port Address/Data.** The parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 kΩ internal pull-up resistor. See Address Data Modes on Page 13 for details of the AD pin operation. For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, A23–8; ALE is used in conjunction with an external latch to retain the values of the A23–8. For 16-bit mode: ALE is automatically asserted whenever a change occurs in the address bits, A15–0; ALE is used in conjunction with an external latch to retain the values of the A15–0. To use these pins as flags (FLAG15–0), set (= 1) Bit 20 of the SYSCTL register and disable the parallel port. See Table 7 on Page 13 for a list of how the AD15–0 pins map to the flag pins. When configured in the IDP_PDAP_CTL register, the IDP Channel 0 can use these pins for parallel input data.
$\overline{\text{RD}}$	O	Output only, driven high[1]	**Parallel Port Read Enable.** $\overline{\text{RD}}$ is asserted low whenever the DSP reads 8-bit or 16-bit data from an external memory device. When AD15–0 are flags, this pin remains deasserted.
$\overline{\text{WR}}$	O	Output only, driven high[1]	**Parallel Port Write Enable.** $\overline{\text{WR}}$ is asserted low whenever the DSP writes 8-bit or 16-bit data to an external memory device. When AD15–0 are flags, this pin remains deasserted.
ALE	O	Output only, driven low[1]	**Parallel Port Address Latch Enable.** ALE is asserted whenever the DSP drives a new address on the parallel port address pin. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15–0 are flags, this pin remains deasserted.
FLAG3–0	I/O/A	Three-state	**Flag Pins.** Each FLAG pin is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals. These pins can be used as an SPI interface slave select output during SPI mastering. These pins are also multiplexed with the $\overline{\text{IRQx}}$ and the TIMEXP signals. In SPI master boot mode, FLAG0 is the slave select pin that must be connected to an SPI EPROM. FLAG0 is configured as a slave select during SPI master boot. When Bit 16 is set (= 1) in the SYSCTL register, FLAG0 is configured as $\overline{\text{IRQ0}}$. When Bit 17 is set (= 1) in the SYSCTL register, FLAG1 is configured as $\overline{\text{IRQ1}}$. When Bit 18 is set (= 1) in the SYSCTL register, FLAG2 is configured as $\overline{\text{IRQ2}}$. When Bit 19 is set (= 1) in the SYSCTL register, FLAG3 is configured as TIMEXP, which indicates that the system timer has expired.
DAI_P20–1	I/O/T	Three-state with programmable pull-up	**Digital Application Interface Pins**. These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the SRU can be routed to any of these pins. The SRU provides the connection from the serial ports, input data port, precision clock generators, and timers to the DAI_P20–1 pins. These pins have internal 22.5 kΩ pull-up resistors which are enabled on reset. These pull-ups can be disabled in the DAI_PIN_PULLUP register.

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
CLK_CFG1–0	I	Input only	**Core/CLKIN Ratio Control**. These pins set the start up clock frequency. See Table 9 for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
$\overline{\text{RESETOUT}}$	O	Output only	**Reset Out**. Drives out the core reset signal to an external device.
$\overline{\text{RESET}}$	I/A	Input only	**Processor Reset**. Resets the ADSP-2126x to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Input only[3]	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2126x.
TMS	I/S	Three-state with pull-up enabled	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TDI	I/S	Three-state with pull-up enabled	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 22.5 kΩ internal pull-up resistor.
TDO	O	Three-state[4]	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Three-state with pull-up enabled	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2126x. $\overline{\text{TRST}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	Three-state with pull-up enabled	**Emulation Status**. Must be connected to the ADSP-2126x Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 kΩ internal pull-up resistor.
V_{DDINT}	P		**Core Power Supply**. Nominally +1.2 V dc and supplies the DSP's core processor (13 pins on the BGA package, 32 pins on the LQFP package).
V_{DDEXT}	P		**I/O Power Supply**. Nominally +3.3 V dc (6 pins on the BGA package, 10 pins on the LQFP package).
A_{VDD}	P		**Analog Power Supply**. Nominally +1.2 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 7.
A_{VSS}	G		**Analog Power Supply Return**.
GND	G		**Power Supply Return**. (54 pins on the BGA package, 39 pins on the LQFP package).

[1] $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE are continuously driven by the DSP and will not be three-stated.
[2] Output only is a three-state driver with its output path always enabled.
[3] Input only is a three-state driver, with both output path and pull-up disabled.
[4] Three-state is a three-state driver, with pull-up disabled.

PRODUCT SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Min	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.14	1.26	V
A_{VDD}	Analog (PLL) Supply Voltage	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
V_{IH}	High Level Input Voltage[2] @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	V
V_{IL}	Low Level Input Voltage[2] @ V_{DDEXT} = Min	–0.5	+0.8	V
V_{IH_CLKIN}	High Level Input Voltage[3] @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.19	V
T_{AMB} K Grade	Ambient Operating Temperature[4, 5]	0	+70	°C
T_{AMB} B Grade	Ambient Operating Temperature[4, 5]	–40	+85	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: AD15–0, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.
[4] See Thermal Characteristics on Page 38 for information on thermal specifications.
[5] See Engineer-to-Engineer Note (No. EE-216) for further information.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[2]	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[3]	2.4		V
V_{OL}	Low Level Output Voltage[2]	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[3]		0.4	V
I_{IH}	High Level Input Current[4, 5]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}	Low Level Input Current[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU}	Low Level Input Current Pull-Up[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
I_{OZH}	Three-State Leakage Current [6, 7, 8]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}	Three-State Leakage Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU}	Three-State Leakage Current Pull-Up[7]	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$	Supply Current (Internal)[9, 10, 11]	t_{CCLK} = 5.0 ns, V_{DDINT} = 1.2 V, T_{AMB} = +25°C		500	mA
I_{AVDD}	Supply Current (Analog)[11]	A_{VDD} = Max		10	mA
C_{IN}	Input Capacitance[12, 13]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.2 V		4.7	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AD15–0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{EMU}$, TDO, CLKOUT, XTAL.
[3] See Output Drive Currents on Page 37 for typical drive current capabilities.
[4] Applies to input pins: $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pins: FLAG3–0.
[7] Applies to three-statable pins with 22.5 kΩ pull-ups: AD15–0, DAI_Px, SPICLK, MISO, MOSI.
[8] Applies to open-drain output pins: $\overline{EMU}$, MISO, MOSI.
[9] Typical internal current data reflects nominal operating conditions.
[10] See Engineer-to-Engineer Note (EE-216) for further information.
[11] Characterized, but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

Clock Input

See Table 16 and Figure 6.

Table 16. Clock Input

Parameter		150 MHz[1] Min	150 MHz[1] Max	200 MHz[2] Min	200 MHz[2] Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	20[3]	160[4]	15[3]	160[4]	ns
t_{CKL}	CLKIN Width Low	7.5[3]	80[4]	6[3]	80[4]	ns
t_{CKH}	CLKIN Width High	7.5[3]	80[4]	6[3]	80[4]	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3	ns
f_{VCO}[5]	VCO Frequency	200	800	200	800	MHz
t_{CCLK}	CCLK Period[6]	6.66	10	5	10	ns

[1] Applies to all 150 MHz models. See Ordering Guide on Page 45.
[2] Applies to all 200 MHz models. See Ordering Guide on Page 45.
[3] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[4] Applies only for CLK_CFG1–0 = 01 and default values for PLL control bits in PMCTL.
[5] See Figure 4 on Page 16 for VCO diagram.
[6] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

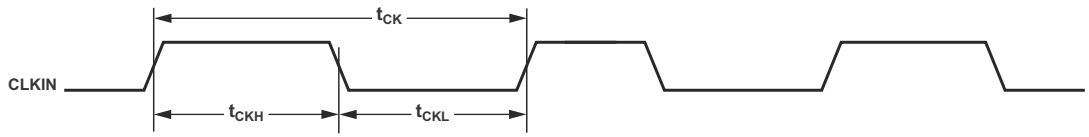
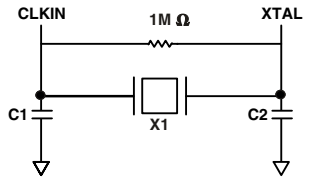


Figure 6. Clock Input

Clock Signals

The ADSP-2126x can use an external clock or a crystal. See CLKIN pin description. The programmer can configure the ADSP-2126x to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode. Note that the 200 MHz clock rate is achieved using a 12.5 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN).



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. CRYSTAL SELECTION MUST COMPLY WITH CLKCFG1-0 = 10 OR = 01.

Figure 7. 150 MHz or 200 MHz Operation with a 12.5 MHz Fundamental Mode Crystal

Reset

See Table 17 and Figure 8.

Table 17. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable VDD and CLKIN (not including start-up time of external clock oscillator).

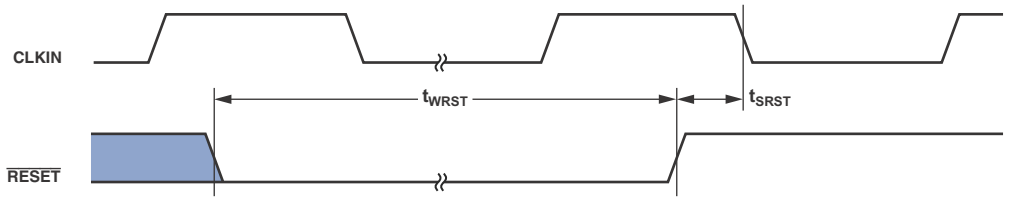


Figure 8. Reset

Interrupts

The timing specification in Table 18 and Figure 9 applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts. Also applies to DAI_P20–1 pins when configured as interrupts.

Table 18. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2\ t_{CCLK} + 2$		ns

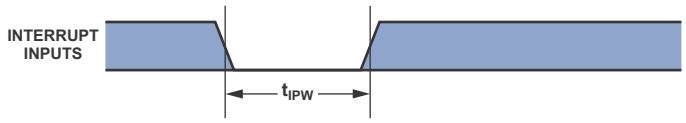


Figure 9. Interrupts

Core Timer

The timing specification in Table 19 and Figure 10 applies to FLAG3 when it is configured as the core timer (CTIMER).

Table 19. Core Timer

Parameter		Min	Max	Unit
Switching Characteristics				
t_{WCTIM}	CTIMER Pulse Width	$4 \times t_{CCLK} - 1$		ns

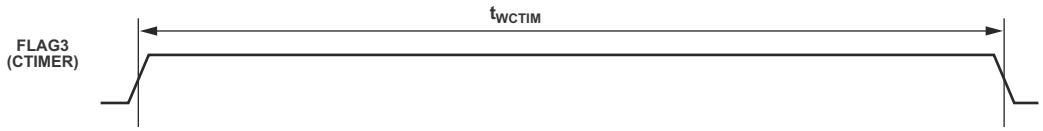


Figure 10. Core Timer

Timer PWM_OUT Cycle Timing

The timing specification in Table 20 and Figure 11 applies to Timer in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 20. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{CCLK} - 1$	$2(2^{31} - 1) \times t_{CCLK}$	ns

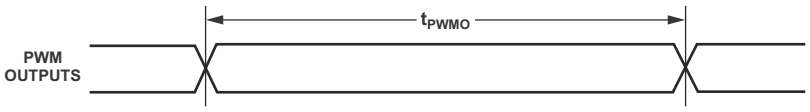


Figure 11. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The timing specification in Table 21 and Figure 12 applies to Timer in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DAI_P20–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 21. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PWI}	Timer Pulse Width	$2 \times t_{CCLK}$	$2(2^{31} - 1) \times t_{CCLK}$	ns

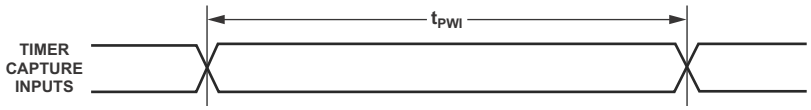


Figure 12. Timer Width Capture Timing

DAI Pin-to-Pin Direct Routing

See Table 22 and Figure 13 for direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 22. DAI Pin-to-Pin Routing

Parameter		Min	Max	Unit
Timing Requirements				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	10	ns

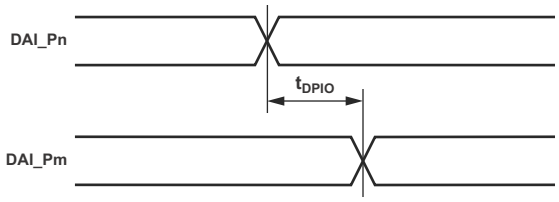


Figure 13. DAI Pin-to-Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

The timing in Table 23 and Figure 14 is valid only when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P07–DAI_P20).

Table 23. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Pulse Width	20		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	2		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	2		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock Falling Edge	2.5	10	ns
t_{DTRIG}	PCG Output Clock and Frame Sync Delay After PCG Trigger	$2.5 + 2.5 \times t_{PCGOW}$	$10 + 2.5 \times t_{PCGOW}$	ns
t_{PCGOW}	Output Clock Pulse Width	40		ns

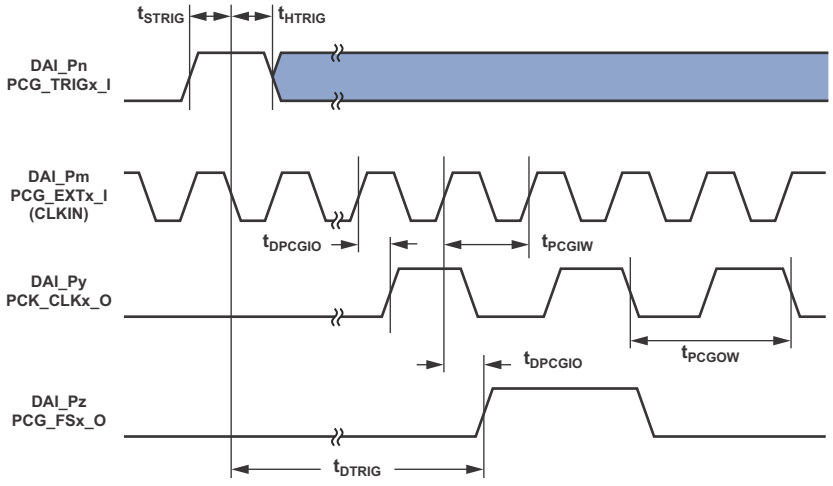


Figure 14. Precision Clock Generator (Direct Pin Routing)

Memory Read—Parallel Port

The specifications in Table 25, Table 26, Figure 16, and Figure 17 are for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-2126x is accessing external memory space.

Table 25. 8-Bit Memory Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{DRS}	Address/Data 7–0 Setup Before $\overline{RD}$ High	3.3		ns
t_{DRH}	Address/Data 7–0 Hold After $\overline{RD}$ High	0		ns
t_{DAD}	Address 15–8 to Data Valid		$D + 0.5 \times t_{CCLK} - 3.5$	ns
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{CCLK} - 2$		ns
t_{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 0.5$		ns
t_{ADAS}[1]	Address/Data 15–0 Setup Before ALE Deasserted	$2.5 \times t_{CCLK} - 2.0$		ns
t_{ADAH}1	Address/Data 15–0 Hold After ALE Deasserted	$0.5 \times t_{CCLK} - 0.8$		ns
t_{ALEHZ}[1]	ALE Deasserted to Address/Data7–0 in High-Z	$0.5 \times t_{CCLK} - 0.8$	$0.5 \times t_{CCLK} + 2.0$	ns
t_{RW}	$\overline{RD}$ Pulse Width	D – 2		ns
t_{ADRH}	Address/Data 15–8 Hold After $\overline{RD}$ High	$0.5 \times t_{CCLK} - 1 + H$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{CCLK}
H = t_{CCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be reconfigured by software to be active low.

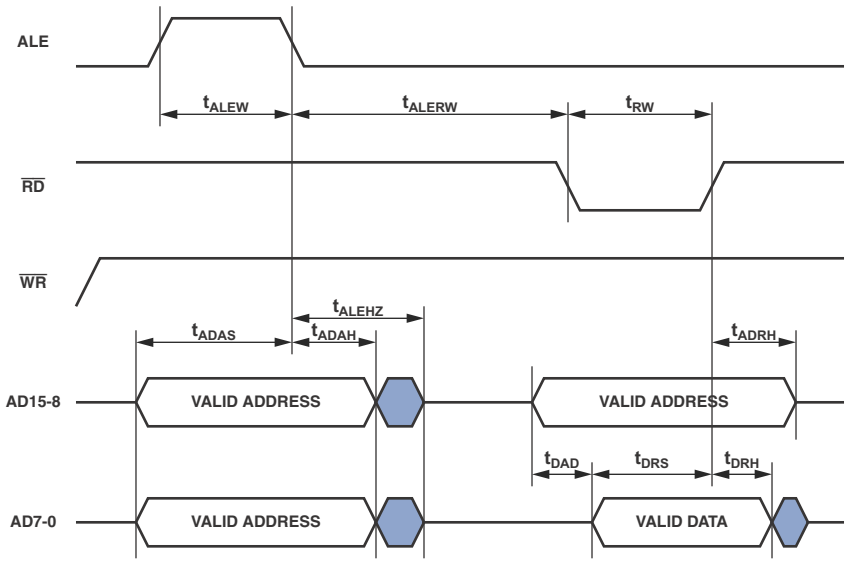


Figure 16. 8-Bit Memory Read Cycle

Memory Write—Parallel Port

Use the specifications in Table 27, Table 28, Figure 18, and Figure 19 for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-2126x is accessing external memory space.

Table 27. 8-Bit Memory Write Cycle

Parameter		Min	Max	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{CCLK} - 2$		ns
t_{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 0.5$		ns
t_{ADAS}[1]	Address/Data 15–0 Setup Before ALE Deasserted	$2.5 \times t_{CCLK} - 2.0$		ns
t_{ADAH}[1]	Address/Data 15–0 Hold After ALE Deasserted	$0.5 \times t_{CCLK} - 0.8$		ns
t_{WW}	$\overline{WR}$ Pulse Width	D – 2		ns
t_{ADWL}	Address/Data 15–8 to $\overline{WR}$ Low	$0.5 \times t_{CCLK} - 1.5$		ns
t_{ADWH}	Address/Data 15–8 Hold After $\overline{WR}$ High	$0.5 \times t_{CCLK} - 1 + H$		ns
t_{ALEHZ}	ALE Deasserted to Address/Data 15–0 in High-Z	$0.5 \times t_{CCLK} - 0.8$	$0.5 \times t_{CCLK} + 2.0$	ns
t_{DWS}	Address/Data 7–0 Setup Before $\overline{WR}$ High	D		ns
t_{DWH}	Address/Data 7–0 Hold After $\overline{WR}$ High	$0.5 \times t_{CCLK} - 1.5 + H$		ns
t_{DAWH}	Address/Data to $\overline{WR}$ High	D		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{CCLK}
H = t_{CCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be reconfigured by software to be active low.

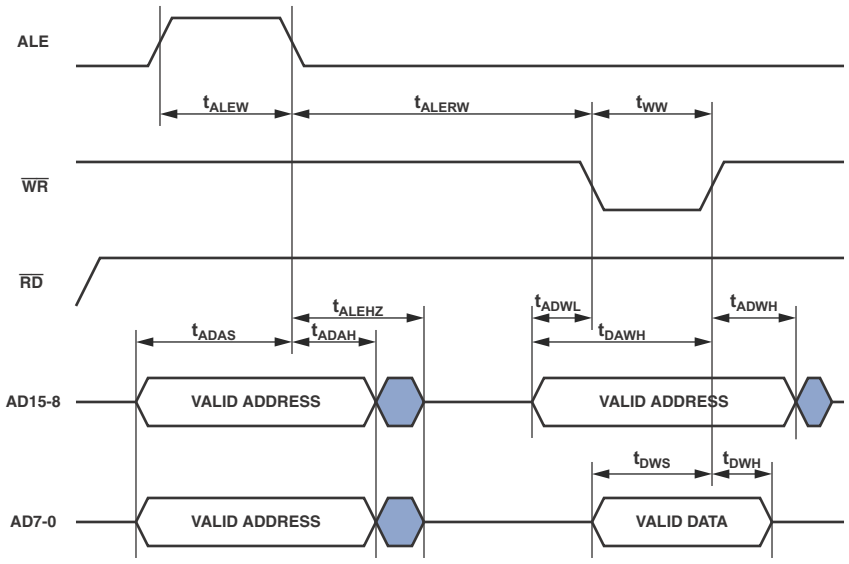


Figure 18. 8-Bit Memory Write Cycle

Table 31. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SCLK[1]	2		ns
t_{DDTTE}	Data Disable from External Transmit SCLK[1]		7	ns
t_{DDTIN}	Data Enable from Internal Transmit SCLK[1]	–1		ns

[1] Referenced to drive edge.

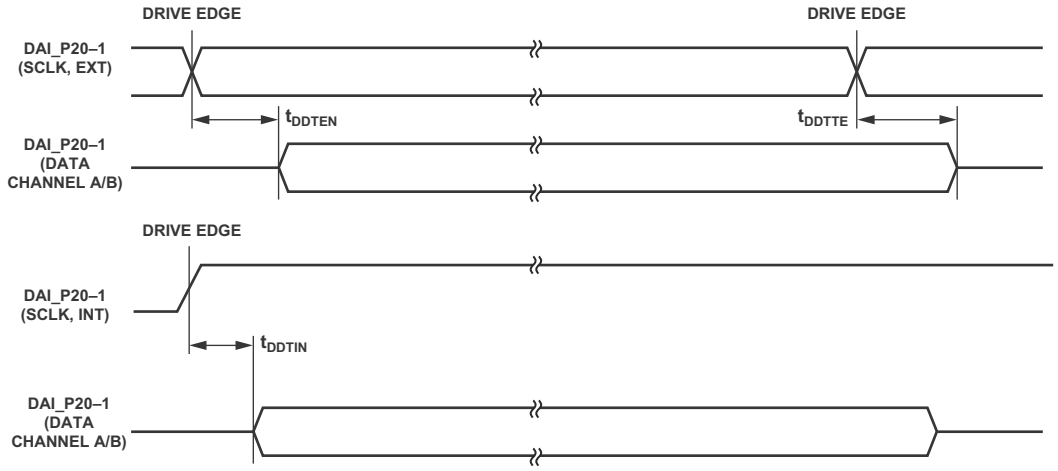


Figure 21. Enable and Three-State

Table 32. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		7	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair mode as well as DSP serial mode, and MCE = 1, MFD = 0.

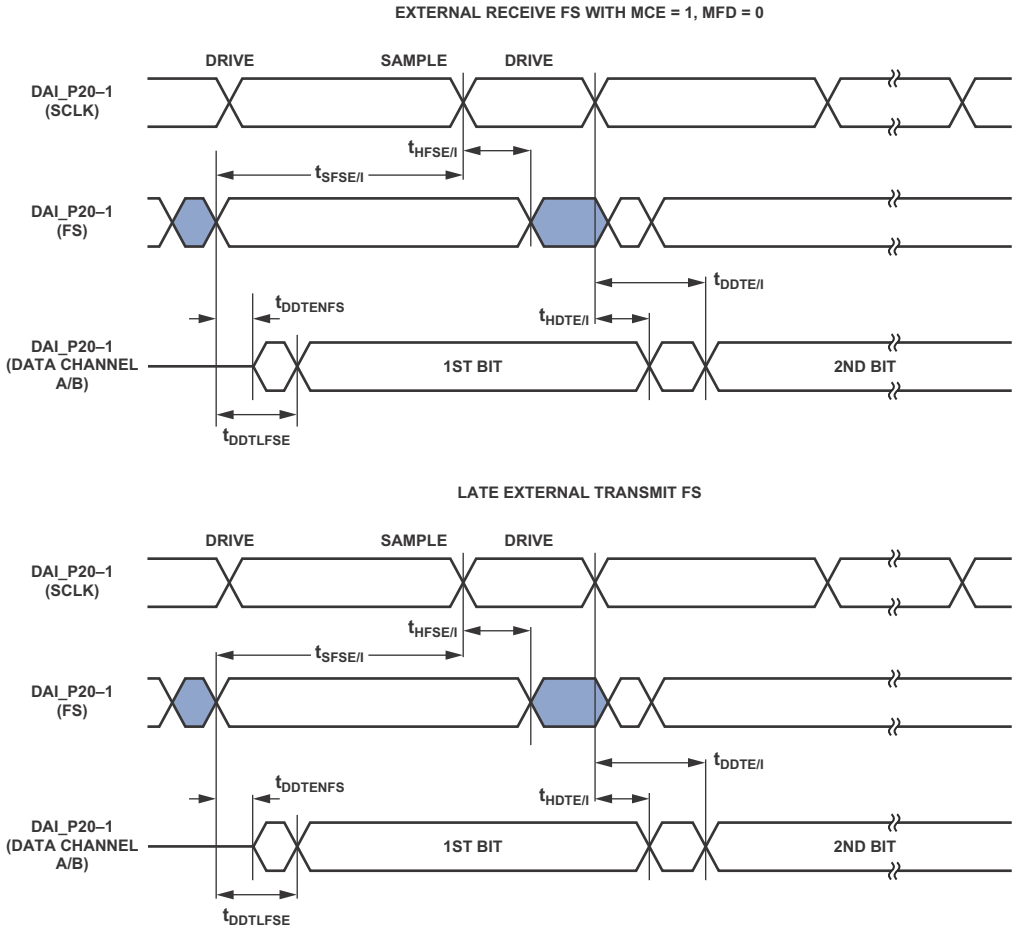


Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

OUTPUT DRIVE CURRENTS

Figure 28 shows typical I-V characteristics for the output drivers of the ADSP-2126x. The curves represent the current drive capability of the output drivers as a function of output voltage.

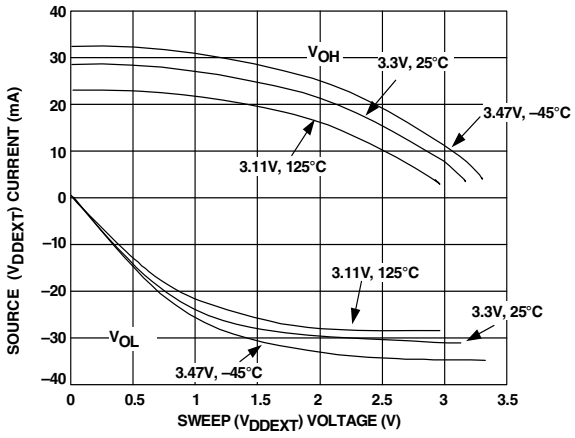


Figure 28. Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 16 on Page 18 through Table 37 on Page 36. These include output disable time, output enable time, and capacitive loading.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 30. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

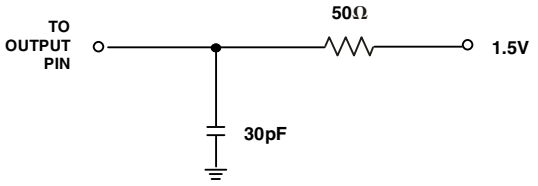


Figure 29. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

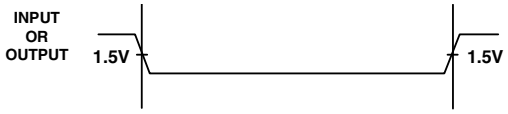


Figure 30. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 29). Figure 32 shows graphically how output delays and holds vary with load capacitance (note that this graph or derating does not apply to output disable delays). The graphs of Figure 31, Figure 32, and Figure 33 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

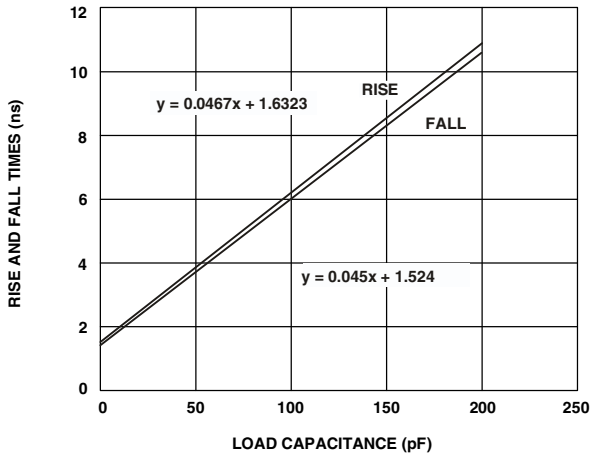


Figure 31. Typical Output Rise Time (20% to 80%, V_{DDEXT} = Max)

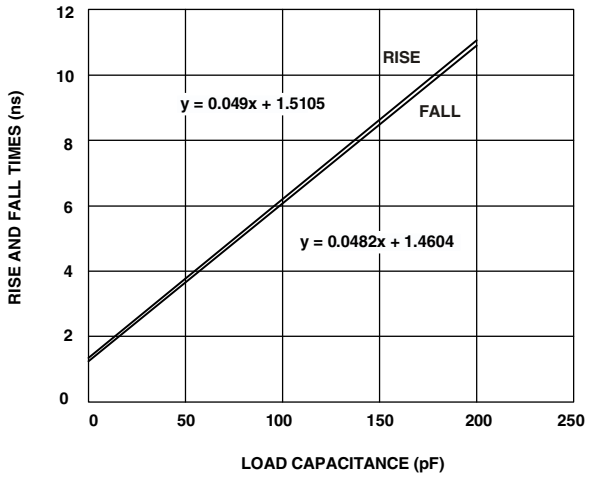


Figure 32. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

136-BALL BGA PIN CONFIGURATIONS

Table 41 shows the ADSP-2126x's pin names and their default function after reset (in parentheses). Figure 34 on Page 42 shows the BGA package pin assignments.

Table 41. 136-Ball BGA Pin Assignments

Pin Name	BGA Pin No.	Pin Name	BGA Pin No.	Pin Name	BGA Pin No.	Pin Name	BGA Pin No.
CLK_CFG0	A01	CLK_CFG1	B01	BOOT_CFG1	C01	V_{DDINT}	D01
XTAL	A02	GND	B02	BOOT_CFG0	C02	GND	D02
TMS	A03	V_{DDEXT}	B03	GND	C03	GND	D04
TCK	A04	CLKIN	B04	GND	C12	GND	D05
TDI	A05	$\overline{TRST}$	B05	GND	C13	GND	D06
$\overline{RESETOUT}$	A06	A_{VSS}	B06	V_{DDINT}	C14	GND	D09
TDO	A07	A_{VDD}	B07			GND	D10
$\overline{EMU}$	A08	V_{DDEXT}	B08			GND	D11
MOSI	A09	SPICLK	B09			GND	D13
MISO	A10	$\overline{RESET}$	B10			V_{DDINT}	D14
$\overline{SPIDS}$	A11	V_{DDINT}	B11				
V_{DDINT}	A12	GND	B12				
GND	A13	GND	B13				
GND	A14	GND	B14				
V_{DDINT}	E01	FLAG1	F01	AD7	G01	AD6	H01
GND	E02	FLAG0	F02	V_{DDINT}	G02	V_{DDEXT}	H02
GND	E04	GND	F04	V_{DDEXT}	G13	DAI_P18 (SD5B)	H13
GND	E05	GND	F05	DAI_P19 (SCLK45)	G14	DAI_P17 (SD5A)	H14
GND	E06	GND	F06				
GND	E09	GND	F09				
GND	E10	GND	F10				
GND	E11	GND	F11				
GND	E13	FLAG2	F13				
FLAG3	E14	DAI_P20 (SFS45)	F14				

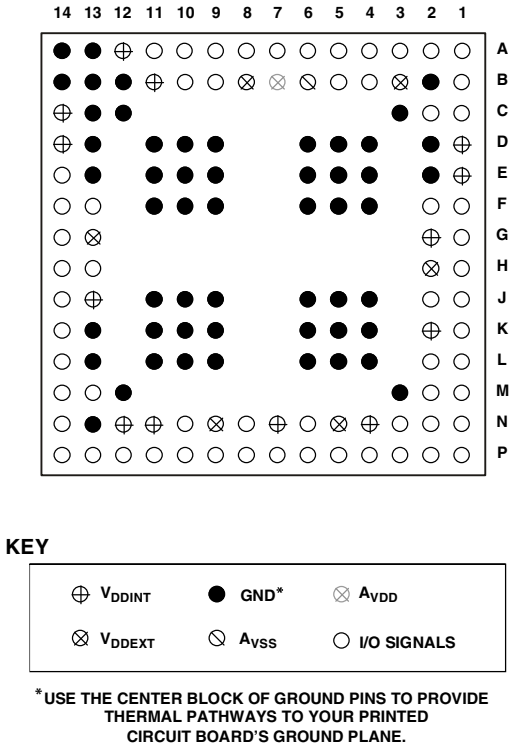
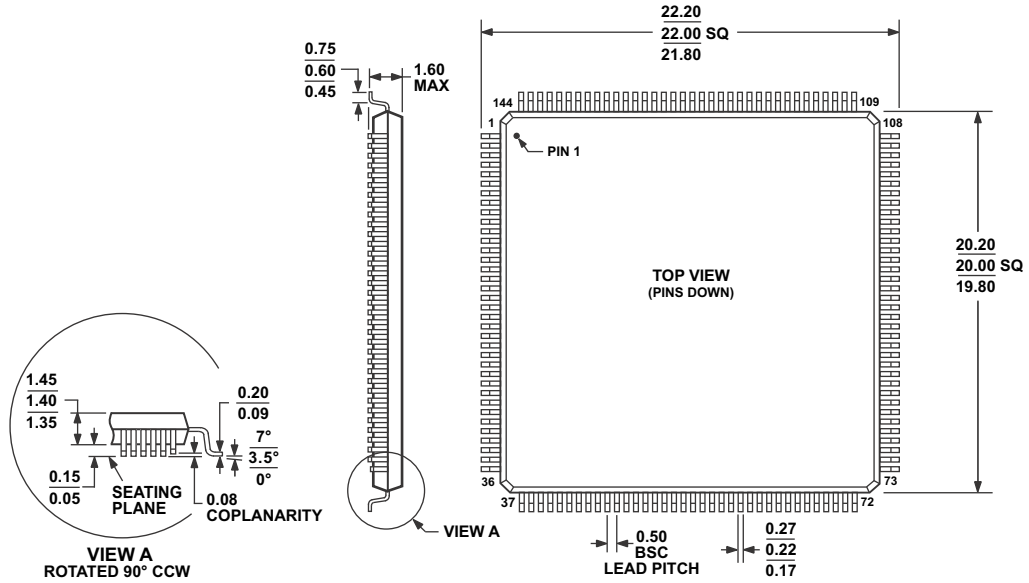


Figure 34. 136-Ball BGA Pin Assignments (Bottom View, Summary)

OUTLINE DIMENSIONS

The ADSP-2126x is available in a 144-lead LQFP package and a 136-ball BGA package shown in Figure 35 and Figure 36.



COMPLIANT TO JEDEC STANDARDS MS-026-BFB

Figure 35. 144-Lead Low Profile Flat Package [LQFP]
(ST-144)
Dimensions shown in millimeters

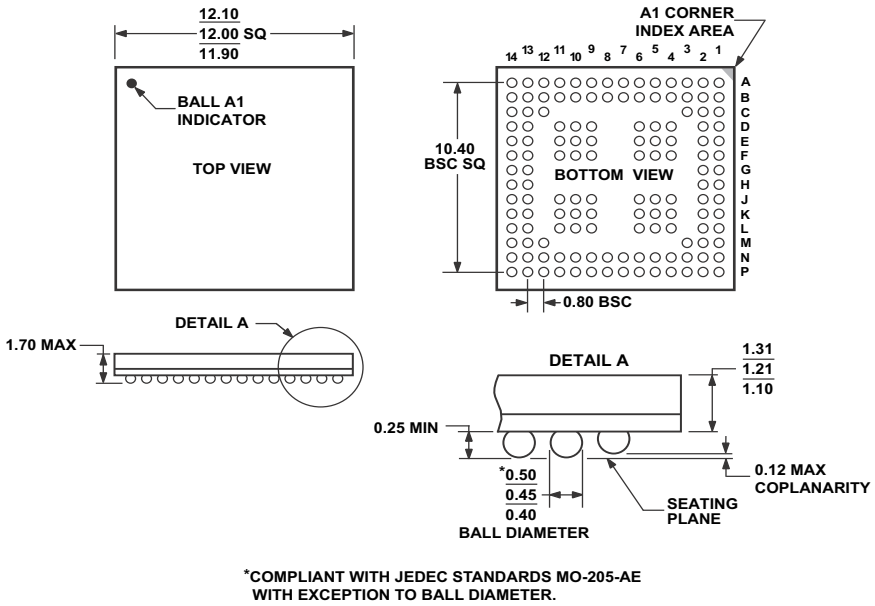


Figure 36. 136-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-136-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 42 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 42. BGA_ED Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
136-Ball CSP_BGA (BC-136-1)	Solder Mask Defined (SMD)	0.4 mm	0.53 mm