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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, SPI
Clock Rate	150MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21266skstz-1d

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REVISION HISTORY

12/12—Rev. F to Rev. G

Corrected Long Word Memory Space in Table 4 in Memory and I/O Interface Features 4

Updated Development Tools 8

Added section, Related Signal Chains 9

Changed the package designator in Figure 36 from BC-136 to BC-136-1. This change in no way affects form, fit, or function. See Outline Dimensions 43

Updated Ordering Guide 45

GENERAL DESCRIPTION

The ADSP-21261/ADSP-21262/ADSP-21266 SHARC® DSPs are members of the SIMD SHARC family of DSPs featuring Analog Devices, Inc., Super Harvard Architecture. The ADSP-2126x is source code compatible with the ADSP-21160 and ADSP-21161 DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. Like other SHARC DSPs, the ADSP-2126x are 32-bit/40-bit floating-point processors optimized for high performance audio applications with dual-ported on-chip SRAM, mask-programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital application interface.

Table 1 shows performance benchmarks for the processors running at 200 MHz. Table 2 shows the features of the individual product offerings.

Table 1. Processor Benchmarks (at 200 MHz)

Benchmark Algorithm	Speed (at 200 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	61.3 µs
FIR Filter (per tap)[1]	3.3 ns
IIR Filter (per biquad)[1]	13.3 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	30 ns
[4×4] × [4×1]	53.3 ns
Divide (y/x)	20 ns
Inverse Square Root	30 ns

[1] Assumes two files in multichannel SIMD mode.

As shown in the functional block diagram in Figure 1 on Page 1, the ADSP-2126x uses two computational units to deliver a 5 to 10 times performance increase over previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-2126x DSPs achieve an instruction cycle time of 5 ns at 200 MHz or 6.6 ns at 150 MHz. With its SIMD computational hardware, the ADSP-2126x can perform 1200 MFLOPS running at 200 MHz, or 900 MFLOPS running at 150 MHz.

Table 2. ADSP-2126x SHARC Processor Features

Feature	ADSP-21261	ADSP-21262	ADSP-21266
RAM	1M bit	2M bit	2M bit
ROM	3M bit	4M bit	4M bit
Audio Decoders in ROM[1]	No	No	Yes
DMA Channels	18	22	22
SPORTs	4	6	6
Package	136-ball BGA 144-lead LQFP	136-ball BGA 144-lead LQFP	136-ball BGA 144-lead LQFP

[1] For information on available audio decoding algorithms, see Table 3 on Page 4.

The ADSP-2126x continues the SHARC family's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include 2M bit dual-ported SRAM memory, 4M bit dual-ported ROM, an I/O processor that supports 22 DMA channels, six serial ports, an SPI interface, external parallel bus, and digital application interface.

The block diagram of the ADSP-2126x on Page 1 illustrates the following architectural features:

- Two processing elements, each containing an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Three programmable interval timers with PWM generation, PWM capture/pulse width measurement, and external event counter capabilities
- On-chip dual-ported SRAM (up to 2M bit)
- On-chip dual-ported, mask-programmable ROM (up to 4M bit)
- JTAG test access port
- 8- or 16-bit parallel port that supports interfaces to off-chip memory peripherals
- DMA controller
- Six full-duplex serial ports (four on the ADSP-21261)
- SPI-compatible interface
- Digital application interface that includes two precision clock generators (PCG), an input data port (IDP), six serial ports, eight serial interfaces, a 20-bit synchronous parallel input port, 10 interrupts, six flag outputs, six flag inputs, three programmable timers, and a flexible signal routing unit (SRU)

FAMILY CORE ARCHITECTURE

The ADSP-2126x is code compatible at the assembly level with the ADSP-2136x and ADSP-2116x, and with the first generation ADSP-2106x SHARC DSPs. The ADSP-2126x shares architectural features with the ADSP-2136x and ADSP-2116x SIMD SHARC family of DSPs, as detailed in the following sections.

SIMD Computational Engine

The ADSP-2126x contain two computational processing elements that operate as a single-instruction multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY can be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing

The ADSP-2126x's SRAM can be configured as a maximum of 64K words of 32-bit data, 128K words of 16-bit data, 42K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

DMA Controller

The ADSP-2126x's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-2126x's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) port, the IDP (input data port), parallel data acquisition port (PDAP), or the parallel port. Up to 22 channels of DMA are available on the ADSP-2126x—one for the SPI interface, 12 via the serial ports, eight via the input data port, and one via the processor's parallel port. Programs can be downloaded to the ADSP-2126x using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Table 4. Internal Memory Space (ADSP-21261)

IOP Registers 0x0000 0000–0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 SRAM 0x0004 0000–0x0004 1FFF	Block 0 SRAM 0x0008 0000–0x0008 2AAA	Block 0 SRAM 0x0008 0000–0x0008 3FFF	Block 0 SRAM 0x0010 0000–0x0010 7FFF
Reserved 0x0004 2000–0x0005 7FFF	Reserved	Reserved 0x0008 4000–0x000A FFFF	Reserved 0x0010 8000–0x0015 FFFF
Block 0 ROM 0x0005 8000–0x0005 DFFF	Block 0 ROM 0x000A 0000–0x000A 7FFF	Block 0 ROM 0x000B 0000–0x000B BFFF	Block 0 ROM 0x0016 0000–0x0017 7FFF
Reserved 0x0005 E000–0x0005 FFFF	Reserved	Reserved 0x000B C000–0x000B FFFF	Reserved 0x0017 8FFF–0x0017 FFFF
Block 1 SRAM 0x0006 0000–0x0006 1FFF	Block 1 SRAM 0x000C 0000–0x000C 2AAA	Block 1 SRAM 0x000C 0000–0x000C 3FFF	Block 1 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000–0x0007 7FFF	Reserved	Reserved 0x000C 4000–0x000E FFFF	Reserved 0x0018 8000–0x001D FFFF
Block 1 ROM 0x0007 8000–0x0007 DFFF	Block 1 ROM 0x000E 0000–0x000E 7FFF	Block 1 ROM 0x000F 0000–0x000F BFFF	Block 1 ROM 0x001E 0000–0x001F 7FFF
Reserved 0x0007 E000–0x0007 FFFF	Reserved	Reserved 0x000F C000–0x000F FFFF	Reserved 0x0000

Table 5. Internal Memory Space (ADSP-21262/ADSP-21266)

IOP Registers 0x0000 0000–0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 SRAM 0x0004 0000–0x0004 3FFF	Block 0 SRAM 0x0008 0000–0x0008 5555	Block 0 SRAM 0x0008 0000–0x0008 7FFF	Block 0 SRAM 0x0010 0000–0x0010 FFFF
Reserved 0x0004 4000–0x0005 7FFF	Reserved	Reserved 0x0008 8000–0x000A FFFF	Reserved 0x0011 0000–0x0015 FFFF
Block 0 ROM 0x0005 8000–0x0005 FFFF	Block 0 ROM 0x000A 0000–0x000A AAAA	Block 0 ROM 0x000B 0000–0x000B FFFF	Block 0 ROM 0x0016 0000–0x0017 FFFF
Block 1 SRAM 0x0006 0000–0x0006 3FFF	Block 1 SRAM 0x000C 0000–0x000C 5555	Block 1 SRAM 0x000C 0000–0x000C 7FFF	Block 1 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0007 7FFF	Reserved	Reserved 0x000C 8000–0x000E FFFF	Reserved 0x0019 0000–0x001D FFFF
Block 1 ROM 0x0007 8000–0x0007 FFFF	Block 1 ROM 0x000E 0000–0x000E AAAA	Block 1 ROM 0x000F 0000–0x000F FFFF	Block 1 ROM 0x001E 0000–0x001F FFFF

Digital Application Interface (DAI)

The Digital application interface provides the ability to connect various peripherals to any of the SHARC DSP's DAI pins (DAI_P20–1).

Connections are made using the signal routing unit (SRU, shown in the block diagram on Page 1).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes six serial ports, two precision clock generators (PCGs), an input data port (IDP), six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2126x core, configurable as either eight channels of I^2S or serial data, or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the ADSP-2126x's serial ports.

For complete information on using the DAI, see the *ADSP-2126x SHARC DSP Peripherals Manual*.

Serial Ports

The ADSP-2126x features six full duplex synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as the Analog Devices AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has its own dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

The serial ports operate at up to one-quarter of the DSP core clock rate, providing each with a maximum data rate of 50M bits/sec for a 200 MHz core and 37.5M bits/sec for a 150 MHz core. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle, two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample-pair and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs) with two data pins, allowing four left-justified sample-pair or I^2S channels (using two stereo devices) per serial port with a maximum of up to 24 audio channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

Serial Peripheral (Compatible) Interface

The serial peripheral interface is an industry-standard synchronous serial link, enabling the ADSP-2126x SPI-compatible port to communicate with other SPI-compatible devices. SPI is an interface consisting of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-2126x SPI-compatible peripheral implementation also features programmable baud rates at up to 50 MHz for a core clock of 200 MHz and up to 37.5 MHz for a core clock of 150 MHz, clock phases, and polarities. The ADSP-2126x SPI-compatible port uses open-drain drivers to support a multimaster configuration and to avoid data contention.

Parallel Port

The parallel port provides interfaces to SRAM and peripheral devices. The multiplexed address and data pins (AD15–0) can access 8-bit devices with up to 24 bits of address, or 16-bit devices with up to 16 bits of address. In either mode, 8- or 16-bit, the maximum data transfer rate is one-third the core clock speed. As an example, a clock rate of 200 MHz is equivalent to 66M byte/sec, and a clock rate of 150 MHz is equivalent to 50M byte/sec.

DMA transfers are used to move data to and from internal memory. Access to the core is also facilitated through the parallel port register read/write functions. The $\overline{RD}$, $\overline{WR}$, and ALE (address latch enable) pins are the control pins for the parallel port.

Timers

The ADSP-2126x has a total of four timers: a core timer able to generate periodic software interrupts, and three general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired output signal, and each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general-purpose timers independently.

ROM-Based Security

The ADSP-2126x has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the DSP does not boot-load any external code, executing exclusively from internal SRAM/ROM. Additionally, the DSP is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or test access port, will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

Program Booting

The internal memory of the ADSP-2126x boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave, or an internal boot. Booting is determined by the boot configuration (BOOT_CFG1–0) pins.

Phase-Locked Loop

The ADSP-2126x uses an on-chip phase-locked loop (PLL) to generate the internal clock for the core. On power-up, the CLK_CFG1–0 pins are used to select ratios of 16:1, 8:1, and 3:1. After booting, numerous other ratios can be selected via software control. The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 2, 4, 8, and 16.

Power Supplies

The ADSP-2126x has separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (A_{VDD}) powers the ADSP-2126x's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the A_{VDD} pin. Place the filter components as close as possible to the A_{VDD}/A_{VSS} pins. For an example circuit, see Figure 2. (A recommended ferrite chip is the muRata BLM18AG102SN1D). To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DDINT} and GND. Use wide traces to connect the bypass capacitors to the analog power (A_{VDD}) and ground (A_{VSS}) pins. Note that the A_{VDD} and A_{VSS} pins specified in Figure 2 are inputs to the processor and not the analog ground plane on the board—the A_{VSS} pin should connect directly to digital ground (GND) at the chip.

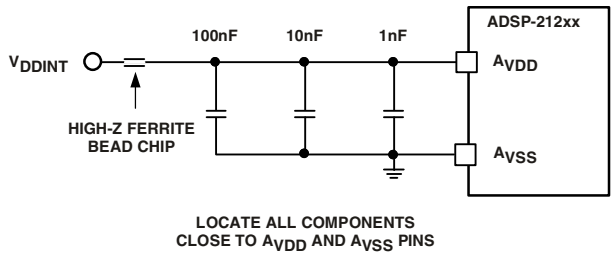


Figure 2. Analog Power Filter Circuit

PIN FUNCTION DESCRIPTIONS

The ADSP-2126x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

DAI_Px, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS,$\overline{\text{TRST}}$, TDI and AD15–0 (NOTE: These pins have internal pull-up resistors.)

The following symbols appear in the Type column of Table 6: A = asynchronous, G = ground, I = input, O = output, P = power supply, S = synchronous, (A/D) = active drive, (O/D) = open-drain, and T = three-state.

Table 6. Pin Descriptions

Pin	Type	State During and After Reset	Function
AD15–0	I/O/T	Rev. 0.1 silicon—AD15–0 pins are driven low both during and after reset. Rev. 0.2 silicon—AD15–0 pins are three-stated and pulled high both during and after reset.	**Parallel Port Address/Data.** The parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 kΩ internal pull-up resistor. See Address Data Modes on Page 13 for details of the AD pin operation. For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, A23–8; ALE is used in conjunction with an external latch to retain the values of the A23–8. For 16-bit mode: ALE is automatically asserted whenever a change occurs in the address bits, A15–0; ALE is used in conjunction with an external latch to retain the values of the A15–0. To use these pins as flags (FLAG15–0), set (= 1) Bit 20 of the SYSCTL register and disable the parallel port. See Table 7 on Page 13 for a list of how the AD15–0 pins map to the flag pins. When configured in the IDP_PDAP_CTL register, the IDP Channel 0 can use these pins for parallel input data.
$\overline{\text{RD}}$	O	Output only, driven high[1]	**Parallel Port Read Enable.** $\overline{\text{RD}}$ is asserted low whenever the DSP reads 8-bit or 16-bit data from an external memory device. When AD15–0 are flags, this pin remains deasserted.
$\overline{\text{WR}}$	O	Output only, driven high[1]	**Parallel Port Write Enable.** $\overline{\text{WR}}$ is asserted low whenever the DSP writes 8-bit or 16-bit data to an external memory device. When AD15–0 are flags, this pin remains deasserted.
ALE	O	Output only, driven low[1]	**Parallel Port Address Latch Enable.** ALE is asserted whenever the DSP drives a new address on the parallel port address pin. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15–0 are flags, this pin remains deasserted.
FLAG3–0	I/O/A	Three-state	**Flag Pins.** Each FLAG pin is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals. These pins can be used as an SPI interface slave select output during SPI mastering. These pins are also multiplexed with the $\overline{\text{IRQx}}$ and the TIMEXP signals. In SPI master boot mode, FLAG0 is the slave select pin that must be connected to an SPI EPROM. FLAG0 is configured as a slave select during SPI master boot. When Bit 16 is set (= 1) in the SYSCTL register, FLAG0 is configured as $\overline{\text{IRQ0}}$. When Bit 17 is set (= 1) in the SYSCTL register, FLAG1 is configured as $\overline{\text{IRQ1}}$. When Bit 18 is set (= 1) in the SYSCTL register, FLAG2 is configured as $\overline{\text{IRQ2}}$. When Bit 19 is set (= 1) in the SYSCTL register, FLAG3 is configured as TIMEXP, which indicates that the system timer has expired.
DAI_P20–1	I/O/T	Three-state with programmable pull-up	**Digital Application Interface Pins**. These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the SRU can be routed to any of these pins. The SRU provides the connection from the serial ports, input data port, precision clock generators, and timers to the DAI_P20–1 pins. These pins have internal 22.5 kΩ pull-up resistors which are enabled on reset. These pull-ups can be disabled in the DAI_PIN_PULLUP register.

PRODUCT SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Min	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.14	1.26	V
A_{VDD}	Analog (PLL) Supply Voltage	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
V_{IH}	High Level Input Voltage[2] @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	V
V_{IL}	Low Level Input Voltage[2] @ V_{DDEXT} = Min	–0.5	+0.8	V
V_{IH_CLKIN}	High Level Input Voltage[3] @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.19	V
T_{AMB} K Grade	Ambient Operating Temperature[4, 5]	0	+70	°C
T_{AMB} B Grade	Ambient Operating Temperature[4, 5]	–40	+85	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: AD15–0, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.
[4] See Thermal Characteristics on Page 38 for information on thermal specifications.
[5] See Engineer-to-Engineer Note (No. EE-216) for further information.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[2]	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[3]	2.4		V
V_{OL}	Low Level Output Voltage[2]	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[3]		0.4	V
I_{IH}	High Level Input Current[4, 5]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}	Low Level Input Current[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU}	Low Level Input Current Pull-Up[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
I_{OZH}	Three-State Leakage Current [6, 7, 8]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}	Three-State Leakage Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU}	Three-State Leakage Current Pull-Up[7]	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$	Supply Current (Internal)[9, 10, 11]	t_{CCLK} = 5.0 ns, V_{DDINT} = 1.2 V, T_{AMB} = +25°C		500	mA
I_{AVDD}	Supply Current (Analog)[11]	A_{VDD} = Max		10	mA
C_{IN}	Input Capacitance[12, 13]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.2 V		4.7	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AD15–0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{EMU}$, TDO, CLKOUT, XTAL.
[3] See Output Drive Currents on Page 37 for typical drive current capabilities.
[4] Applies to input pins: $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pins: FLAG3–0.
[7] Applies to three-statable pins with 22.5 kΩ pull-ups: AD15–0, DAI_Px, SPICLK, MISO, MOSI.
[8] Applies to open-drain output pins: $\overline{EMU}$, MISO, MOSI.
[9] Typical internal current data reflects nominal operating conditions.
[10] See Engineer-to-Engineer Note (EE-216) for further information.
[11] Characterized, but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 16.

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in Table 16 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 16 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLD)$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 2, 4, 8, 16 based on the PLLD value programmed on the PMCTL register. During reset this value is 1.

f_{INPUT} = is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of various clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 13 and Table 14.

Table 13. CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CCLK	Core Clock	Variable, see equation

Table 14. Clock Periods

Timing Requirements	Description[1]
t_{CK}	CLKIN Clock Period
t_{CCLK}	(Processor) Core Clock Period
t_{MCLK}	Internal memory clock = 1/2 t_{CCLK}
t_{SCLK}	Serial Port Clock Period = (t_{CCLK}) × SR
t_{SPICLK}	SPI Clock Period = (t_{CCLK}) × SPIR

[1] where:
SR = serial port-to-core clock ratio (wide range, determined by SPORT CLKDIV)
SPIR = SPI-to-core clock ratio (wide range, determined by SPIBAUD register)
SCLK = serial port clock
SPICLK = SPI clock

Figure 4 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-2126x SHARC Processor Peripherals Reference* and *Managing the Core PLL on Third-Generation SHARC Processors (EE-290).*

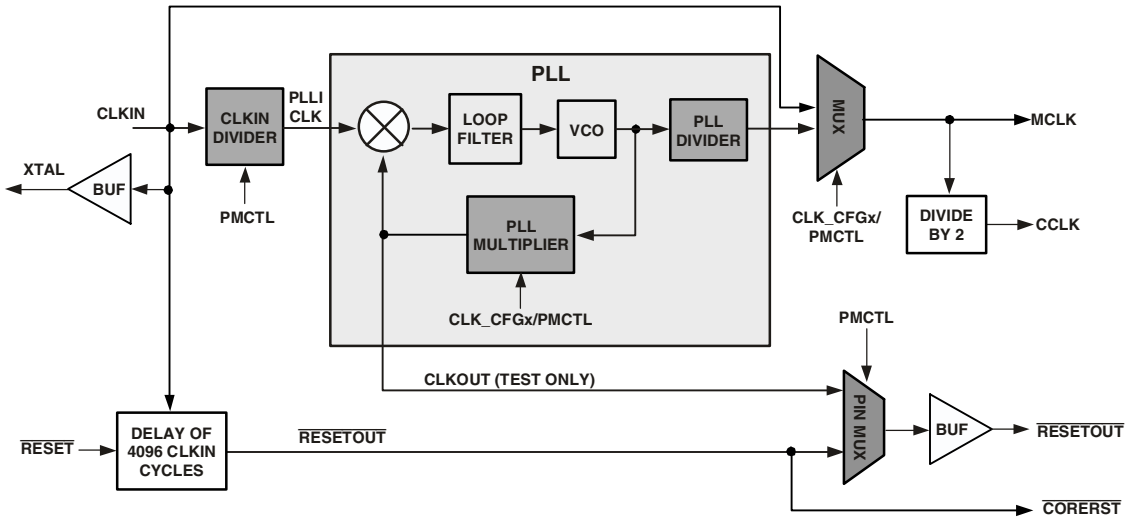


Figure 4. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for DSP startup are given in Table 15 and Figure 5. Note that during power-up, a leakage current of approximately 200 µA may be observed on the $\overline{\text{RESET}}$ pin. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 15. Power-Up Sequencing (DSP Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid[1]	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
Switching Characteristics				
$t_{CORERST}$	DSP Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK}$[4, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to the crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 17. If setup time is not met, one additional CLKIN cycle can be added to the core reset time, resulting in 4097 cycles maximum.

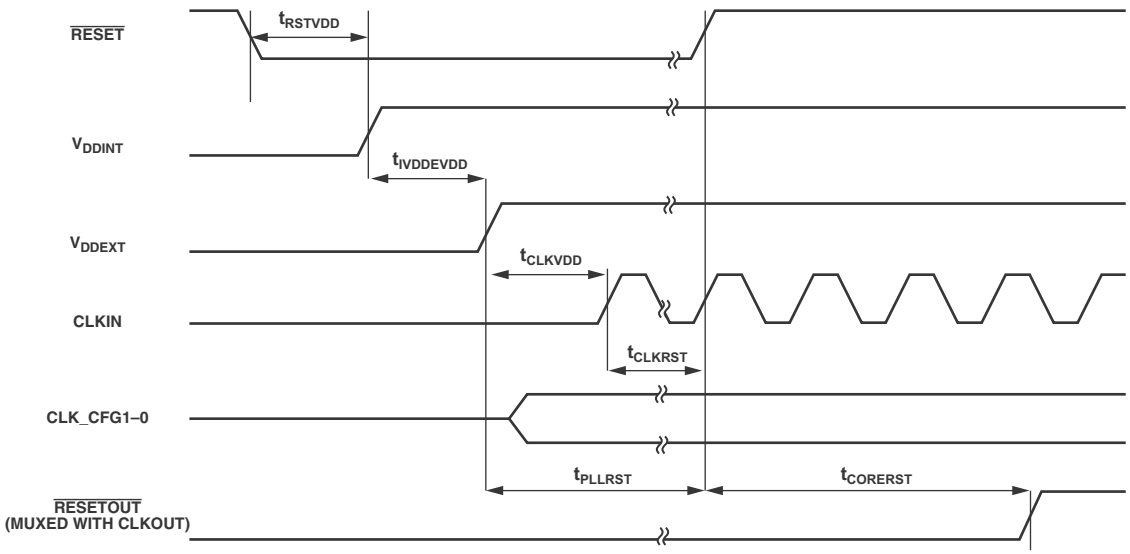


Figure 5. Power-Up Sequencing

Reset

See Table 17 and Figure 8.

Table 17. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable VDD and CLKIN (not including start-up time of external clock oscillator).

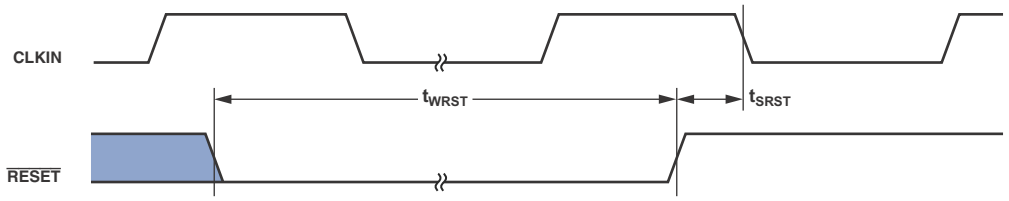


Figure 8. Reset

Interrupts

The timing specification in Table 18 and Figure 9 applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts. Also applies to DAI_P20–1 pins when configured as interrupts.

Table 18. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2\ t_{CCLK} + 2$		ns

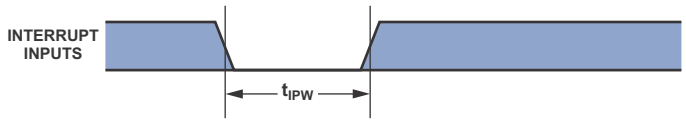


Figure 9. Interrupts

Flags

The timing specifications in Table 24 and Figure 15 apply to the FLAG3–0 and DAI_P20–1 pins, the parallel port, and the serial peripheral interface. See Table 6 on Page 10 for more information on flag use.

Table 24. Flags

Parameter		Min	Max	Unit
Timing Requirements				
t_{FIPW}	FLAG3–0 IN Pulse Width	$2 \times t_{CCLK} + 3$		ns
Switching Characteristics				
t_{FOPW}	FLAG3–0 OUT Pulse Width	$2 \times t_{CCLK} - 1$		ns

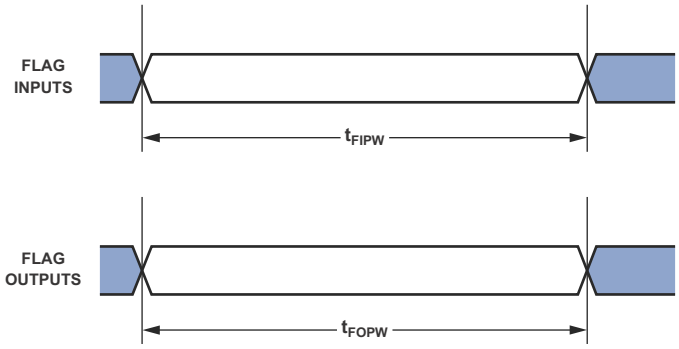


Figure 15. Flags

Memory Read—Parallel Port

The specifications in Table 25, Table 26, Figure 16, and Figure 17 are for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-2126x is accessing external memory space.

Table 25. 8-Bit Memory Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{DRS}	Address/Data 7–0 Setup Before $\overline{RD}$ High	3.3		ns
t_{DRH}	Address/Data 7–0 Hold After $\overline{RD}$ High	0		ns
t_{DAD}	Address 15–8 to Data Valid		$D + 0.5 \times t_{CCLK} - 3.5$	ns
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{CCLK} - 2$		ns
t_{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 0.5$		ns
t_{ADAS}[1]	Address/Data 15–0 Setup Before ALE Deasserted	$2.5 \times t_{CCLK} - 2.0$		ns
t_{ADAH}1	Address/Data 15–0 Hold After ALE Deasserted	$0.5 \times t_{CCLK} - 0.8$		ns
t_{ALEHZ}[1]	ALE Deasserted to Address/Data7–0 in High-Z	$0.5 \times t_{CCLK} - 0.8$	$0.5 \times t_{CCLK} + 2.0$	ns
t_{RW}	$\overline{RD}$ Pulse Width	D – 2		ns
t_{ADRH}	Address/Data 15–8 Hold After $\overline{RD}$ High	$0.5 \times t_{CCLK} - 1 + H$		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{CCLK}
H = t_{CCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be reconfigured by software to be active low.

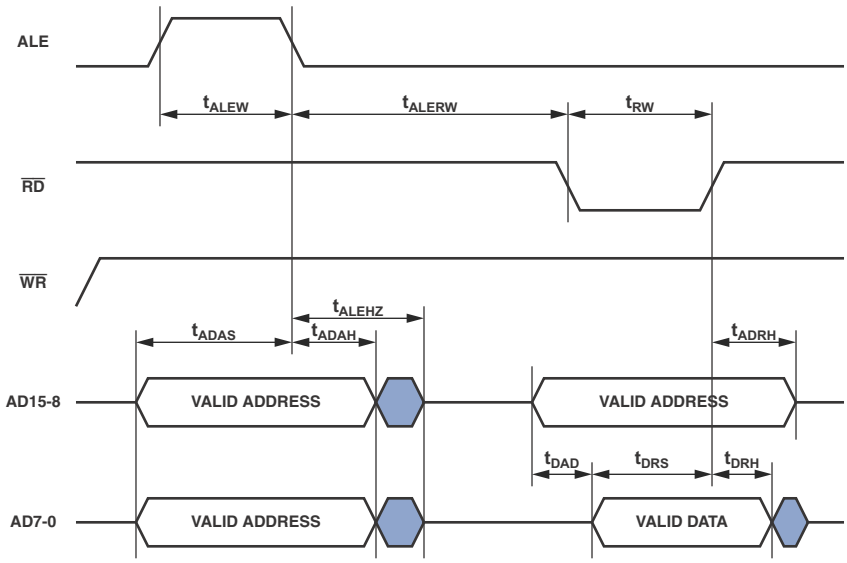


Figure 16. 8-Bit Memory Read Cycle

Serial Ports

To determine whether communication is possible between two devices at a given clock speed, the specifications in Table 29, Table 30, Table 31, Table 32, Figure 20, Figure 21, and Figure 22 must be confirmed: 1) frame sync delay and frame sync setup and hold; 2) data delay and data setup and hold; and 3) SCLK width.

Serial port signals (SCLK, FS, DxA,/DxB) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 29. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)[1]	2.5		ns
t_{HFSE}	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)[1]	2.5		ns
t_{SDRE}	Receive Data Setup Before Receive SCLK[1]	2.5		ns
t_{HDRE}	Receive Data Hold After SCLK[1]	2.5		ns
t_{SCLKW}	SCLK Width	7		ns
t_{SCLK}	SCLK Period	20		ns
Switching Characteristics				
t_{DFSE}	FS Delay After SCLK (Internally Generated FS in Either Transmit or Receive Mode)[2]		7	ns
t_{HOFSE}	FS Hold After SCLK (Internally Generated FS in Either Transmit or Receive Mode)[2]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SCLK[2]		7	ns
t_{HDTE}	Transmit Data Hold After Transmit SCLK[2]	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 30. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	FS Setup Before SCLK (Externally Generated FS in Either Transmit or Receive Mode)[1]	6		ns
t_{HFSI}	FS Hold After SCLK (Externally Generated FS in Either Transmit or Receive Mode)[1]	1.5		ns
t_{SDRI}	Receive Data Setup Before SCLK[1]	6		ns
t_{HDRI}	Receive Data Hold After SCLK[1]	1.5		ns
Switching Characteristics				
t_{DFSI}	FS Delay After SCLK (Internally Generated FS in Transmit Mode)[2]		3	ns
t_{HOFSI}	FS Hold After SCLK (Internally Generated FS in Transmit Mode)[2]	–1.0		ns
t_{DFSI}	FS Delay After SCLK (Internally Generated FS in Receive Mode)[2]		3	ns
t_{HOFSI}	FS Hold After SCLK (Internally Generated FS in Receive Mode)[2]	–1.0		ns
t_{DDTI}	Transmit Data Delay After SCLK[2]		3	ns
t_{HDTI}	Transmit Data Hold After SCLK[2]	–1.0		ns
t_{SCLKIW}	Transmit or Receive SCLK Width	$0.5t_{SCLK} - 2$	$0.5t_{SCLK} + 2$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 32. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		7	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair mode as well as DSP serial mode, and MCE = 1, MFD = 0.

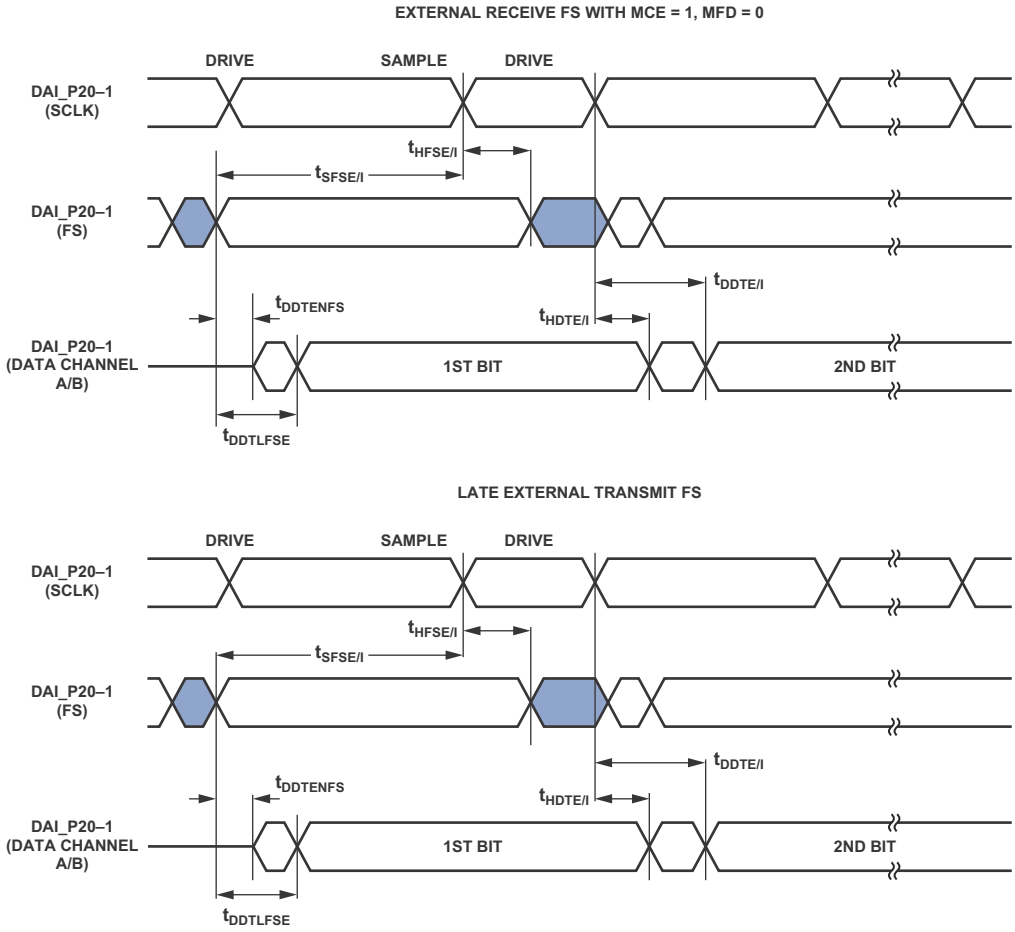


Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

JTAG Test Access Port and Emulation

Table 37. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	8		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		10	ns

[1] System Inputs = AD15–0, $\overline{\text{SPIDS}}$, CLK_CFG1–0, $\overline{\text{RESET}}$, $\overline{\text{BOOT\_CFG1–0}}$, MISO, MOSI, SPICLK, DAI_Px, FLAG3–0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, AD15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, CLKOUT, $\overline{\text{EMU}}$, ALE.

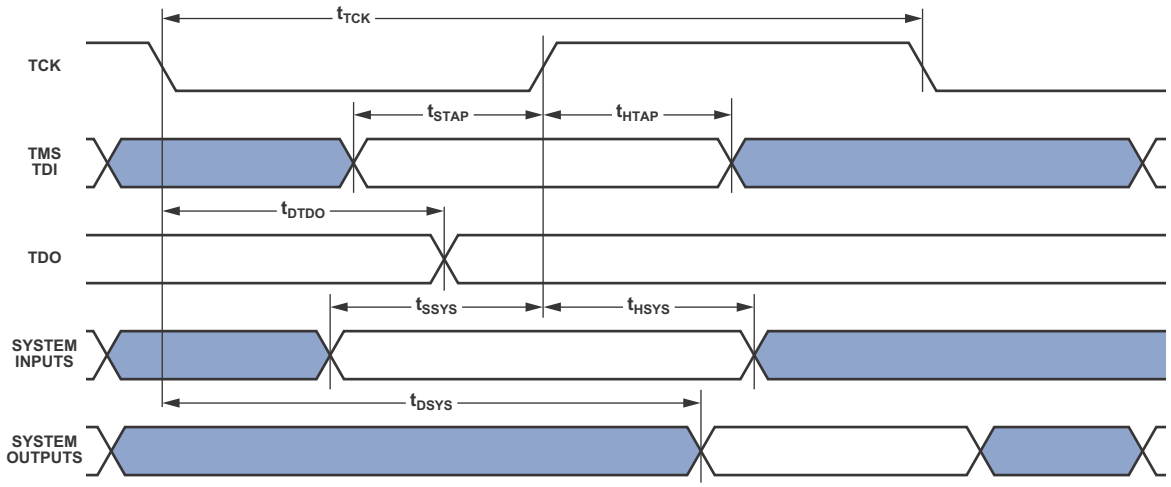


Figure 27. JTAG Test Access Port and Emulation

OUTPUT DRIVE CURRENTS

Figure 28 shows typical I-V characteristics for the output drivers of the ADSP-2126x. The curves represent the current drive capability of the output drivers as a function of output voltage.

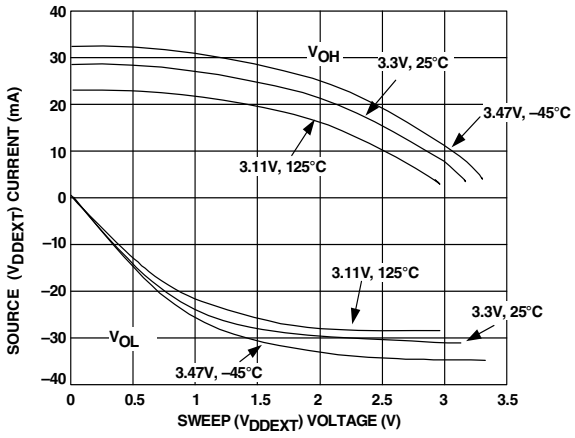


Figure 28. Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 16 on Page 18 through Table 37 on Page 36. These include output disable time, output enable time, and capacitive loading.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 30. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

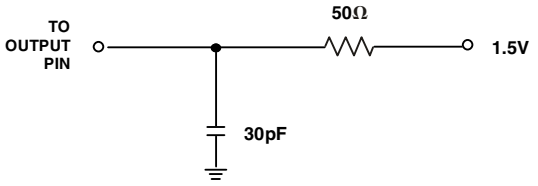


Figure 29. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

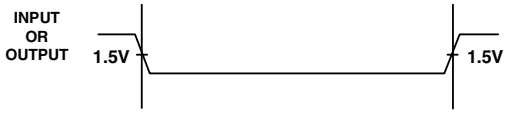


Figure 30. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 29). Figure 32 shows graphically how output delays and holds vary with load capacitance (note that this graph or derating does not apply to output disable delays). The graphs of Figure 31, Figure 32, and Figure 33 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

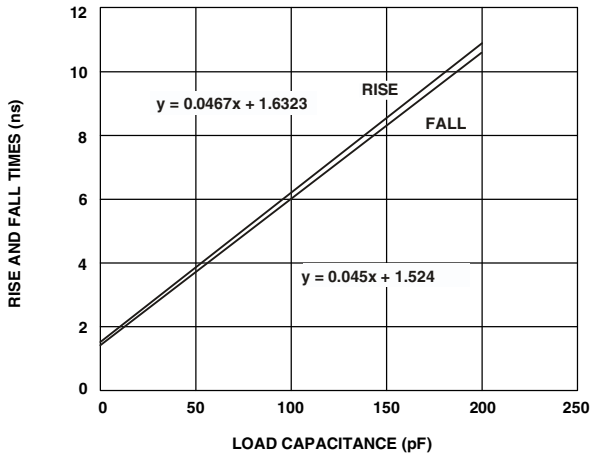


Figure 31. Typical Output Rise Time (20% to 80%, V_{DDEXT} = Max)

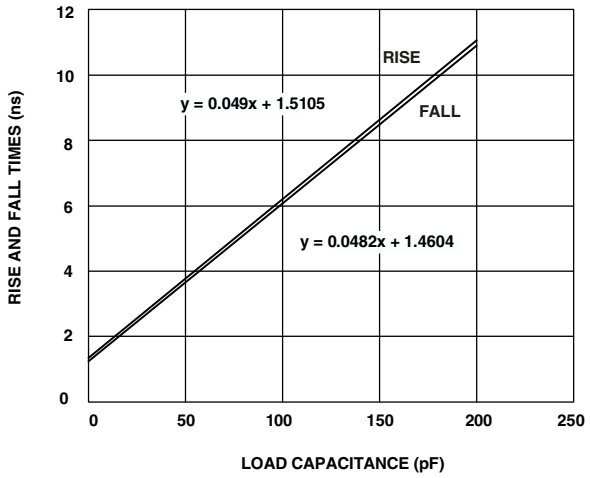


Figure 32. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

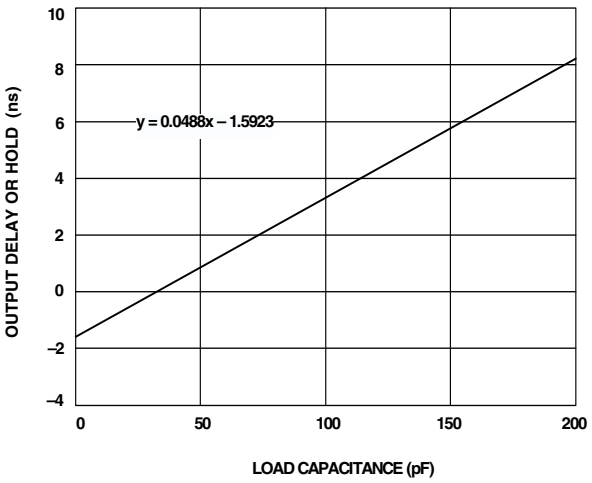


Figure 33. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

ENVIRONMENTAL CONDITIONS

The ADSP-2126x processor is rated for performance under T_{AMB} environmental conditions specified in the Operating Conditions on Page 14.

THERMAL CHARACTERISTICS

Table 38 and Table 39 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 38 and Table 39 (Ψ_{JMT} indicates moving air).

P_D = power dissipation. See *Estimating Power Dissipation for ADSP-21262 SHARC DSPs (EE-216)* for more information.

Values of θ_{JA} are provided for package comparison and PCB design considerations (θ_{JMA} indicates moving air). θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Table 38. Thermal Characteristics for 136-Ball BGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	31.0	°C/W
θ_{JMA}	Airflow = 1 m/s	27.3	°C/W
θ_{JMA}	Airflow = 2 m/s	26.0	°C/W
θ_{JC}		6.99	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.16	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.30	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.35	°C/W

Table 39. Thermal Characteristics for 144-Lead LQFP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	32.5	°C/W
θ_{JMA}	Airflow = 1 m/s	28.9	°C/W
θ_{JMA}	Airflow = 2 m/s	27.8	°C/W
θ_{JC}		7.8	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.5	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.8	°C/W
Ψ_{JMT}	Airflow = 2 m/s	1.0	°C/W

144-LEAD LQFP PIN CONFIGURATIONS

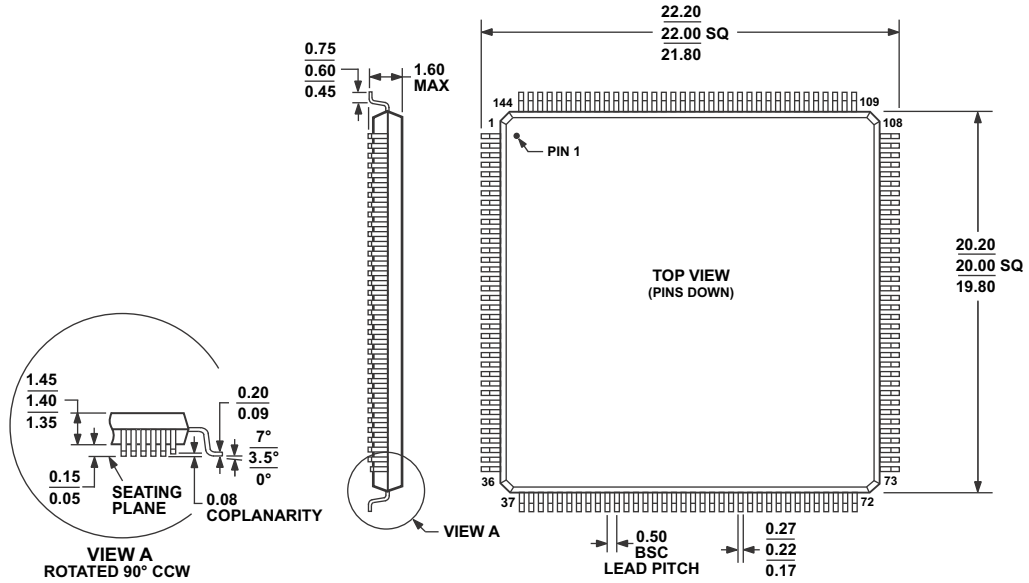
Table 40 shows the ADSP-2126x's pin names and their default function after reset (in parentheses).

Table 40. 144-Lead LQFP Pin Assignments

Pin Name	LQFP Pin No.	Pin Name	LQFP Pin No.	Pin Name	LQFP Pin No.	Pin Name	LQFP Pin No.
V_{DDINT}	1	V_{DDINT}	37	V_{DDEXT}	73	GND	109
CLK_CFG0	2	GND	38	GND	74	V_{DDINT}	110
CLK_CFG1	3	$\overline{RD}$	39	V_{DDINT}	75	GND	111
BOOT_CFG0	4	ALE	40	GND	76	V_{DDINT}	112
BOOT_CFG1	5	AD15	41	DAI_P10 (SD2B)	77	GND	113
GND	6	AD14	42	DAI_P11 (SD3A)	78	V_{DDINT}	114
V_{DDEXT}	7	AD13	43	DAI_P12 (SD3B)	79	GND	115
GND	8	GND	44	DAI_P13 (SCLK23)	80	V_{DDEXT}	116
V_{DDINT}	9	V_{DDEXT}	45	DAI_P14 (SFS23)	81	GND	117
GND	10	AD12	46	DAI_P15 (SD4A)	82	V_{DDINT}	118
V_{DDINT}	11	V_{DDINT}	47	V_{DDINT}	83	GND	119
GND	12	GND	48	GND	84	V_{DDINT}	120
V_{DDINT}	13	AD11	49	GND	85	$\overline{RESET}$	121
GND	14	AD10	50	DAI_P16 (SD4B)	86	$\overline{SPIDS}$	122
FLAG0	15	AD9	51	DAI_P17 (SD5A)	87	GND	123
FLAG1	16	AD8	52	DAI_P18 (SD5B)	88	V_{DDINT}	124
AD7	17	DAI_P1 (SD0A)	53	DAI_P19 (SCLK45)	89	SPICLK	125
GND	18	V_{DDINT}	54	V_{DDINT}	90	MISO	126
V_{DDINT}	19	GND	55	GND	91	MOSI	127
GND	20	DAI_P2 (SD0B)	56	GND	92	GND	128
V_{DDEXT}	21	DAI_P3 (SCLK0)	57	V_{DDEXT}	93	V_{DDINT}	129
GND	22	GND	58	DAI_P20 (SFS45)	94	V_{DDEXT}	130
V_{DDINT}	23	V_{DDEXT}	59	GND	95	A_{VDD}	131
AD6	24	V_{DDINT}	60	V_{DDINT}	96	A_{VSS}	132
AD5	25	GND	61	FLAG2	97	GND	133
AD4	26	DAI_P4 (SFS0)	62	FLAG3	98	$\overline{RESETOUT}$	134
V_{DDINT}	27	DAI_P5 (SD1A)	63	V_{DDINT}	99	$\overline{EMU}$	135
GND	28	DAI_P6 (SD1B)	64	GND	100	TDO	136
AD3	29	DAI_P7 (SCLK1)	65	V_{DDINT}	101	TDI	137
AD2	30	V_{DDINT}	66	GND	102	$\overline{TRST}$	138
V_{DDEXT}	31	GND	67	V_{DDINT}	103	TCK	139
GND	32	V_{DDINT}	68	GND	104	TMS	140
AD1	33	GND	69	V_{DDINT}	105	GND	141
AD0	34	DAI_P8 (SFS1)	70	GND	106	CLKIN	142
$\overline{WR}$	35	DAI_P9 (SD2A)	71	V_{DDINT}	107	XTAL	143
V_{DDINT}	36	V_{DDINT}	72	V_{DDINT}	108	V_{DDEXT}	144

OUTLINE DIMENSIONS

The ADSP-2126x is available in a 144-lead LQFP package and a 136-ball BGA package shown in Figure 35 and Figure 36.



COMPLIANT TO JEDEC STANDARDS MS-026-BFB

Figure 35. 144-Lead Low Profile Flat Package [LQFP]
(ST-144)
Dimensions shown in millimeters

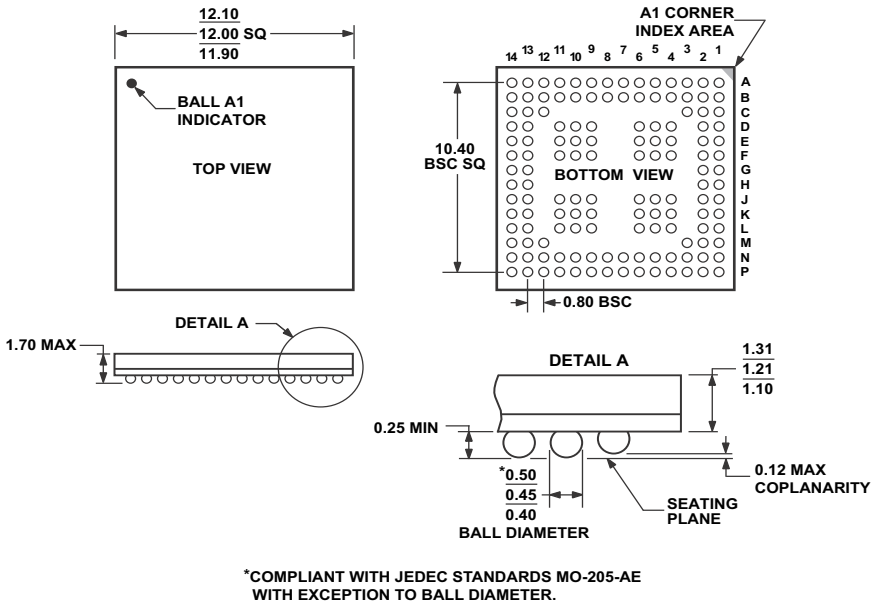


Figure 36. 136-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-136-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 42 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 42. BGA_ED Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
136-Ball CSP_BGA (BC-136-1)	Solder Mask Defined (SMD)	0.4 mm	0.53 mm