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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	DAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	256kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21266skstz-2d

elements, but each processing element operates on different data. This architecture is efficient at executing math intensive audio algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2126x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2126x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on Page 1). With the ADSP-2126x's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2126x includes an on-chip instruction cache that enables three-bus operation to fetch an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The ADSP-2126x's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-2126x contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the ADSP-2126x can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-2126x adds the following architectural features to the SIMD SHARC family core:

Dual-Ported On-Chip Memory

The ADSP-21262 and ADSP-21266 contain two megabits of internal SRAM and four megabits of internal mask-programmable ROM. The ADSP-21261 contain one megabit of internal SRAM and three megabits of internal mask-programmable ROM. Each block can be configured for different combinations of code and data storage (see memory maps, Table 4 and Table 5). Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory, in combination with three separate on-chip buses, allows two data transfers from the core and one from the I/O processor, in a single cycle.

The ADSP-2126x is available with a variety of multichannel surround sound decoders, preprogrammed in ROM memory. Table 3 shows the configuration of decoder algorithms.

Table 3. Multichannel Surround Sound Decoder Algorithms in On-Chip ROM

Algorithms	B ROM	C ROM	D ROM
PCM	Yes	Yes	Yes
AC-3	Yes	Yes	Yes
DTS 96/24	v2.2	v2.3	v2.3
AAC (LC)	Yes	Yes	Coefficients only
WMAPRO 7.1 96 KHz	No	No	Yes
MPEG2 BC 2ch	Yes	Yes	No
Noise	Yes	Yes	Yes
DPL2x/EX	DPL2	Yes	Yes
Neo:6/ES (v2.5046)	Yes	Yes	Yes

Table 5. Internal Memory Space (ADSP-21262/ADSP-21266)

IOP Registers 0x0000 0000–0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 SRAM 0x0004 0000–0x0004 3FFF	Block 0 SRAM 0x0008 0000–0x0008 5555	Block 0 SRAM 0x0008 0000–0x0008 7FFF	Block 0 SRAM 0x0010 0000–0x0010 FFFF
Reserved 0x0004 4000–0x0005 7FFF	Reserved	Reserved 0x0008 8000–0x000A FFFF	Reserved 0x0011 0000–0x0015 FFFF
Block 0 ROM 0x0005 8000–0x0005 FFFF	Block 0 ROM 0x000A 0000–0x000A AAAA	Block 0 ROM 0x000B 0000–0x000B FFFF	Block 0 ROM 0x0016 0000–0x0017 FFFF
Block 1 SRAM 0x0006 0000–0x0006 3FFF	Block 1 SRAM 0x000C 0000–0x000C 5555	Block 1 SRAM 0x000C 0000–0x000C 7FFF	Block 1 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0007 7FFF	Reserved	Reserved 0x000C 8000–0x000E FFFF	Reserved 0x0019 0000–0x001D FFFF
Block 1 ROM 0x0007 8000–0x0007 FFFF	Block 1 ROM 0x000E 0000–0x000E AAAA	Block 1 ROM 0x000F 0000–0x000F FFFF	Block 1 ROM 0x001E 0000–0x001F FFFF

Digital Application Interface (DAI)

The Digital application interface provides the ability to connect various peripherals to any of the SHARC DSP's DAI pins (DAI_P20–1).

Connections are made using the signal routing unit (SRU, shown in the block diagram on Page 1).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes six serial ports, two precision clock generators (PCGs), an input data port (IDP), six flag outputs and six flag inputs, and three timers. The IDP provides an additional input path to the ADSP-2126x core, configurable as either eight channels of I^2S or serial data, or as seven channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the ADSP-2126x's serial ports.

For complete information on using the DAI, see the *ADSP-2126x SHARC DSP Peripherals Manual*.

Serial Ports

The ADSP-2126x features six full duplex synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as the Analog Devices AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has its own dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTs are enabled, or six full duplex TDM streams of 128 channels per frame.

The serial ports operate at up to one-quarter of the DSP core clock rate, providing each with a maximum data rate of 50M bits/sec for a 200 MHz core and 37.5M bits/sec for a 150 MHz core. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle, two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample-pair and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs) with two data pins, allowing four left-justified sample-pair or I^2S channels (using two stereo devices) per serial port with a maximum of up to 24 audio channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

TARGET BOARD JTAG EMULATOR CONNECTOR

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2126x processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply.

The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set

breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2126x architecture and functionality. For detailed information on the ADSP-2126x family core architecture and instruction set, refer to the *ADSP-2126x SHARC DSP Core Manual* and the *ADSP-21160 SHARC DSP Instruction Set Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 6. Pin Descriptions (Continued)

Pin	Type	State During and After Reset	Function
SPICLK	I/O	Three-state with pull-up enabled, driven high in SPI-master boot mode	**Serial Peripheral Interface Clock Signal**. Driven by the master, this signal controls the rate at which data is transferred. The master can transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (HIGH). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 22.5 kΩ internal pull-up resistor. If SPI master boot mode is selected, MOSI and SPICLK pins are driven during reset. These pins are not three-stated during reset in SPI master boot mode.
$\overline{\text{SPIDS}}$	I	Input only	**Serial Peripheral Interface Slave Device Select**. An active low signal used to select the DSP as an SPI slave device. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode, the DSP's $\overline{\text{SPIDS}}$ signal can be driven by a slave device to signal to the DSP (as SPI master) that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single master, multiple-slave configuration where flag pins are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For ADSP-2126x to ADSP-2126x SPI interaction, any of the master ADSP-2126x's flag pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the ADSP-2126x SPI slave device.
MOSI	I/O (O/D)	Three-state with pull-up enabled, driven low in SPI-master boot mode	**SPI Master Out Slave In**. If the ADSP-2126x is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the ADSP-2126x is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an ADSP-2126x SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has a 22.5 kΩ internal pull-up resistor. If SPI master boot mode is selected, MOSI and SPICLK pins are driven during reset. These pins are not three-stated during reset in SPI master boot mode.
MISO	I/O (O/D)	Three-state with pull-up enabled	**SPI Master In Slave Out**. If the ADSP-2126x is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the ADSP-2126x is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an ADSP-2126x SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has a 22.5 kΩ internal pull-up resistor. MISO can be configured as O/D by setting the OPD bit in the SPICTL register. **Note:** *Only one slave is allowed to transmit data at any given time.* To enable broadcast transmission to multiple SPI slaves, the DSP's MISO pin can be disabled by setting (= 1) Bit 5 (DMISO) of the SPICTL register.
BOOT_CFG1–0	I	Input only	**Boot Configuration Select**. Selects the boot mode for the DSP. The BOOT_CFG pins must be valid before reset is asserted. See Table 8 on Page 13 for a description of the boot modes.
CLKIN	I	Input only	**Local Clock In**. Used in conjunction with XTAL. CLKIN is the ADSP-2126x clock input. It configures the ADSP-2126x to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-2126x to use the external clock source such as an external clock oscillator. The core is clocked either by the PLL output or this clock input depending on the CLK_CFG1–0 pin settings. CLKIN should not be halted, changed, or operated below the specified frequency.
XTAL	O	Output only[2]	**Crystal Oscillator Terminal**. Used in conjunction with CLKIN to drive an external crystal.

ADDRESS DATA PINS AS FLAGS

To use these pins as flags (FLAG15–0), set (= 1) Bit 20 of the SYSCTL register and disable the parallel port.

Table 7. AD15–0 to FLAG Pin Mapping

AD Pin	Flag Pin	AD Pin	Flag Pin
AD0	FLAG8	AD8	FLAG0
AD1	FLAG9	AD9	FLAG1
AD2	FLAG10	AD10	FLAG2
AD3	FLAG11	AD11	FLAG3
AD4	FLAG12	AD12	FLAG4
AD5	FLAG13	AD13	FLAG5
AD6	FLAG14	AD14	FLAG6
AD7	FLAG15	AD15	FLAG7

Boot Modes

Table 8. Boot Mode Selection

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port Boot via EPROM
11	Reserved

CORE INSTRUCTION RATE TO CLKIN RATIO MODES

Table 9. Core Instruction Rate/CLKIN Ratio Selection

CLK_CFG1–0	Core to CLKIN Ratio
00	3:1
01	16:1
10	8:1
11	Reserved

ADDRESS DATA MODES

Table 10 shows the functionality of the AD pins for 8-bit and 16-bit transfers to the parallel port. For 8-bit data transfers, ALE latches address bits A23–A8 when asserted, followed by address bits A7–A0 and data bits D7–D0 when deasserted. For 16-bit data transfers, ALE latches address bits A15–A0 when asserted, followed by data bits D15–D0 when deasserted.

Table 10. Address/Data Mode Selection

EP Data Mode	ALE	AD7–0 Function	AD15–8 Function
8-bit	Asserted	A15–8	A23–16
8-bit	Deasserted	D7–0	A7–0
16-bit	Asserted	A7–0	A15–8
16-bit	Deasserted	D7–0	D15–8

PRODUCT SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Min	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.14	1.26	V
A_{VDD}	Analog (PLL) Supply Voltage	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
V_{IH}	High Level Input Voltage[2] @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	V
V_{IL}	Low Level Input Voltage[2] @ V_{DDEXT} = Min	–0.5	+0.8	V
V_{IH_CLKIN}	High Level Input Voltage[3] @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.19	V
T_{AMB} K Grade	Ambient Operating Temperature[4, 5]	0	+70	°C
T_{AMB} B Grade	Ambient Operating Temperature[4, 5]	–40	+85	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: AD15–0, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.
[4] See Thermal Characteristics on Page 38 for information on thermal specifications.
[5] See Engineer-to-Engineer Note (No. EE-216) for further information.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[2]	@ V_{DDEXT} = Min, I_{OH} = –1.0 mA[3]	2.4		V
V_{OL}	Low Level Output Voltage[2]	@ V_{DDEXT} = Min, I_{OL} = 1.0 mA[3]		0.4	V
I_{IH}	High Level Input Current[4, 5]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}	Low Level Input Current[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{ILPU}	Low Level Input Current Pull-Up[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
I_{OZH}	Three-State Leakage Current [6, 7, 8]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}	Three-State Leakage Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU}	Three-State Leakage Current Pull-Up[7]	@ V_{DDEXT} = Max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$	Supply Current (Internal)[9, 10, 11]	t_{CCLK} = 5.0 ns, V_{DDINT} = 1.2 V, T_{AMB} = +25°C		500	mA
I_{AVDD}	Supply Current (Analog)[11]	A_{VDD} = Max		10	mA
C_{IN}	Input Capacitance[12, 13]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.2 V		4.7	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AD15–0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3–0, DAI_Px, SPICLK, MOSI, MISO, $\overline{EMU}$, TDO, CLKOUT, XTAL.
[3] See Output Drive Currents on Page 37 for typical drive current capabilities.
[4] Applies to input pins: $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pins: FLAG3–0.
[7] Applies to three-statable pins with 22.5 kΩ pull-ups: AD15–0, DAI_Px, SPICLK, MISO, MOSI.
[8] Applies to open-drain output pins: $\overline{EMU}$, MISO, MOSI.
[9] Typical internal current data reflects nominal operating conditions.
[10] See Engineer-to-Engineer Note (EE-216) for further information.
[11] Characterized, but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 3 provides details about the package branding for the ADSP-21266 processors. For a complete listing of product availability, see Ordering Guide on Page 45.

Figure 3. Typical Package Brand

Table 11. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option (optional)
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See *Estimating Power for the ADSP-21262 SHARC Processors (EE-216)* for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 38.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 12 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.4 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +1.4 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage –0.5 V to V_{DDEXT}	+0.5 V
Output Voltage Swing –0.5 V to V_{DDEXT}	+0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	125°C

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, serial ports, and parallel port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins. To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the parallel port logic and I/O pads).

Power-Up Sequencing

The timing requirements for DSP startup are given in Table 15 and Figure 5. Note that during power-up, a leakage current of approximately 200 µA may be observed on the $\overline{\text{RESET}}$ pin. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 15. Power-Up Sequencing (DSP Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid[1]	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
Switching Characteristics				
$t_{CORERST}$	DSP Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK}$[4, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 V and 3.3 V rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to the crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 17. If setup time is not met, one additional CLKIN cycle can be added to the core reset time, resulting in 4097 cycles maximum.

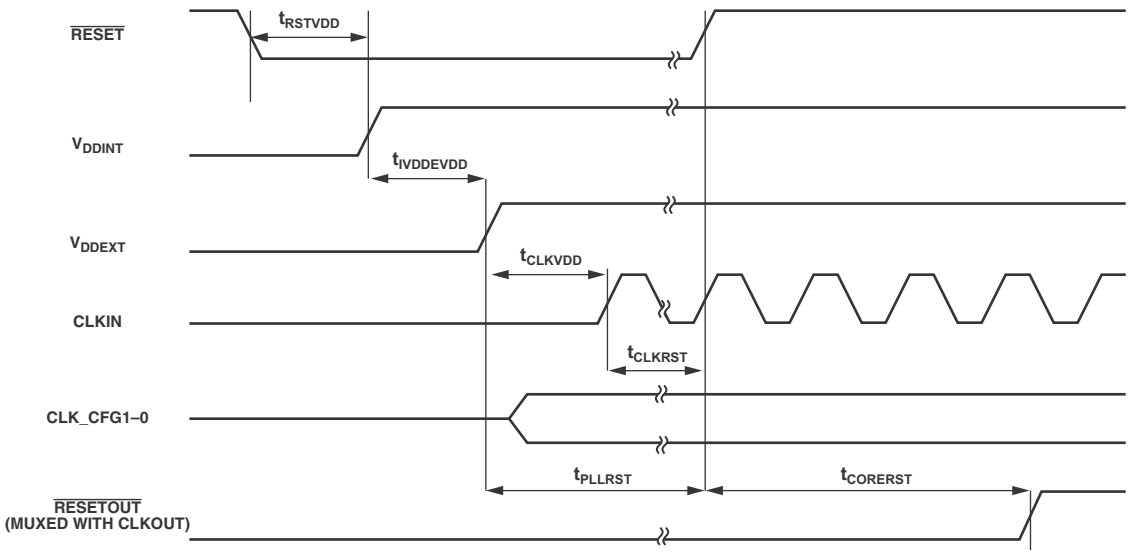

Figure 5. Power-Up Sequencing

Reset

See Table 17 and Figure 8.

Table 17. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable VDD and CLKIN (not including start-up time of external clock oscillator).

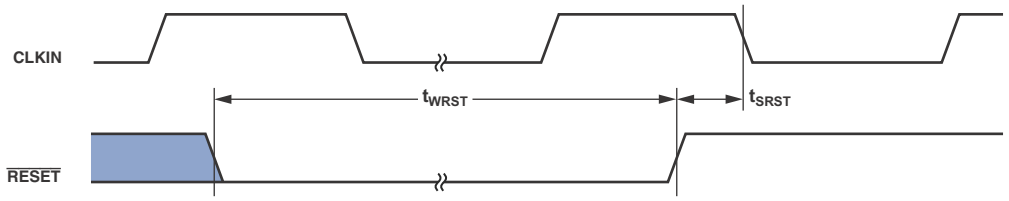

Figure 8. Reset

Interrupts

The timing specification in Table 18 and Figure 9 applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts. Also applies to DAI_P20–1 pins when configured as interrupts.

Table 18. Interrupts

Parameter		Min	Max	Unit
Timing Requirements				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2\ t_{CCLK} + 2$		ns

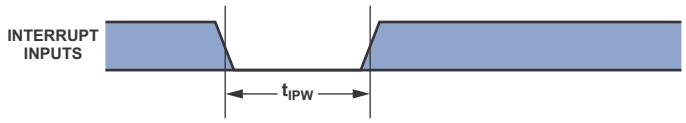

Figure 9. Interrupts

Precision Clock Generator (Direct Pin Routing)

The timing in Table 23 and Figure 14 is valid only when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P07–DAI_P20).

Table 23. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Pulse Width	20		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	2		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	2		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock Falling Edge	2.5	10	ns
t_{DTRIG}	PCG Output Clock and Frame Sync Delay After PCG Trigger	$2.5 + 2.5 \times t_{PCGOW}$	$10 + 2.5 \times t_{PCGOW}$	ns
t_{PCGOW}	Output Clock Pulse Width	40		ns

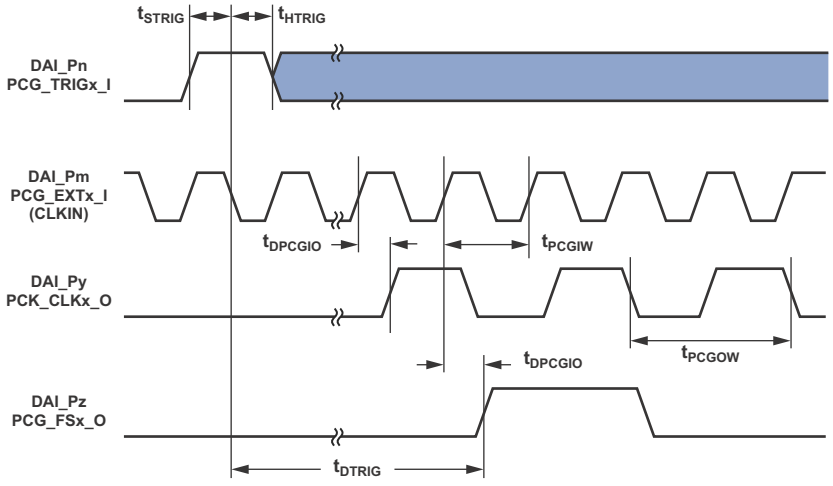

Figure 14. Precision Clock Generator (Direct Pin Routing)

Memory Write—Parallel Port

Use the specifications in Table 27, Table 28, Figure 18, and Figure 19 for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-2126x is accessing external memory space.

Table 27. 8-Bit Memory Write Cycle

Parameter		Min	Max	Unit
Switching Characteristics				
t_{ALEW}	ALE Pulse Width	$2 \times t_{CCLK} - 2$		ns
t_{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 0.5$		ns
t_{ADAS}[1]	Address/Data 15–0 Setup Before ALE Deasserted	$2.5 \times t_{CCLK} - 2.0$		ns
t_{ADAH}[1]	Address/Data 15–0 Hold After ALE Deasserted	$0.5 \times t_{CCLK} - 0.8$		ns
t_{WW}	$\overline{WR}$ Pulse Width	D – 2		ns
t_{ADWL}	Address/Data 15–8 to $\overline{WR}$ Low	$0.5 \times t_{CCLK} - 1.5$		ns
t_{ADWH}	Address/Data 15–8 Hold After $\overline{WR}$ High	$0.5 \times t_{CCLK} - 1 + H$		ns
t_{ALEHZ}	ALE Deasserted to Address/Data 15–0 in High-Z	$0.5 \times t_{CCLK} - 0.8$	$0.5 \times t_{CCLK} + 2.0$	ns
t_{DWS}	Address/Data 7–0 Setup Before $\overline{WR}$ High	D		ns
t_{DWH}	Address/Data 7–0 Hold After $\overline{WR}$ High	$0.5 \times t_{CCLK} - 1.5 + H$		ns
t_{DAWH}	Address/Data to $\overline{WR}$ High	D		ns

D = (The value set by the PPDUR Bits (5–1) in the PPCTL register) × t_{CCLK}
H = t_{CCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be reconfigured by software to be active low.

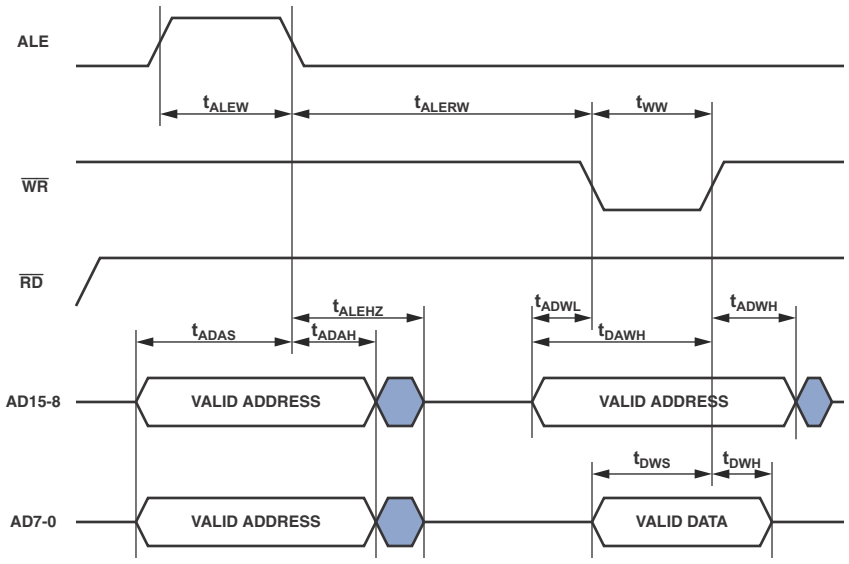

Figure 18. 8-Bit Memory Write Cycle

Table 31. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SCLK[1]	2		ns
t_{DDTTE}	Data Disable from External Transmit SCLK[1]		7	ns
t_{DDTIN}	Data Enable from Internal Transmit SCLK[1]	–1		ns

[1] Referenced to drive edge.

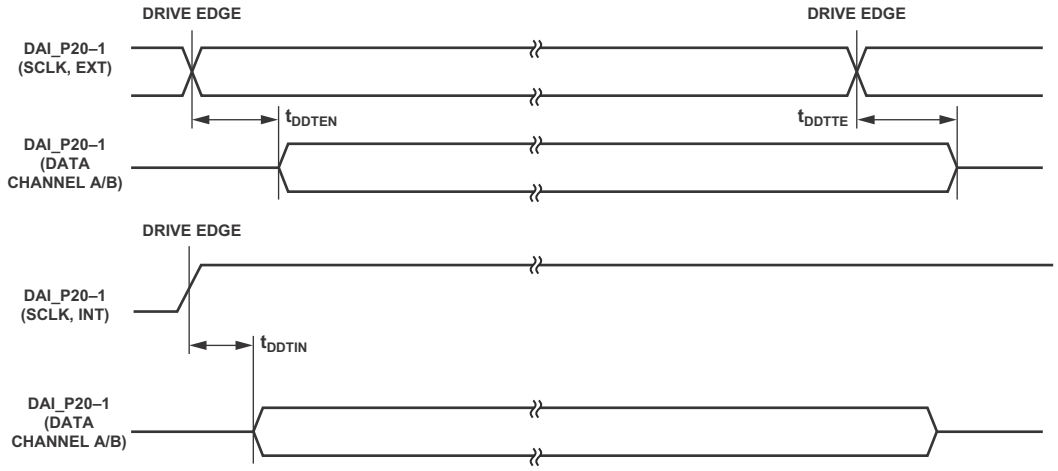

Figure 21. Enable and Three-State

Table 32. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		7	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair mode as well as DSP serial mode, and MCE = 1, MFD = 0.

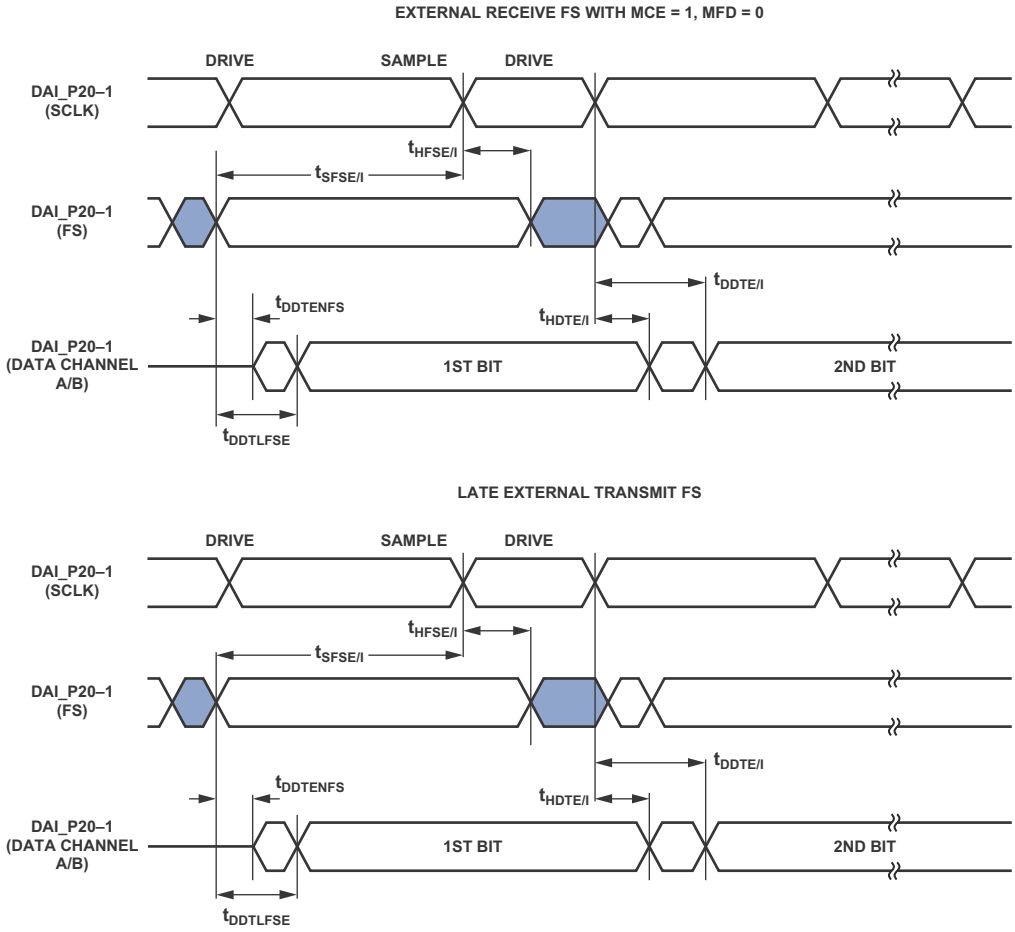

Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 33 and Figure 23. IDP Signals (SCLK, FS, SDATA) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 33. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}	FS Setup Before SCLK Rising Edge[1]	2.5		ns
t_{SIHFS}	FS Hold After SCLK Rising Edge[1]	2.5		ns
t_{SISD}	SDATA Setup Before SCLK Rising Edge[1]	2.5		ns
t_{SIHD}	SDATA Hold After SCLK Rising Edge[1]	2.5		ns
$t_{IDPCLKW}$	Clock Width	7		ns
t_{IDPCLK}	Clock Period	20		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via the precision clock generators (PCG) or SPORTs. PCG input can be either CLKIN or any of the DAI pins.

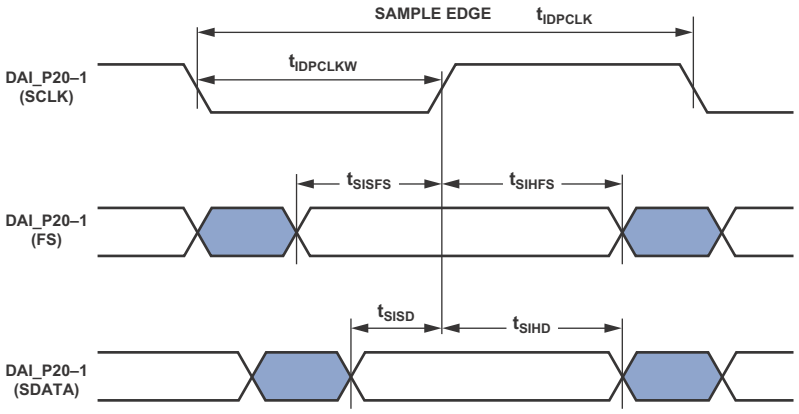

Figure 23. Input Data Port (IDP)

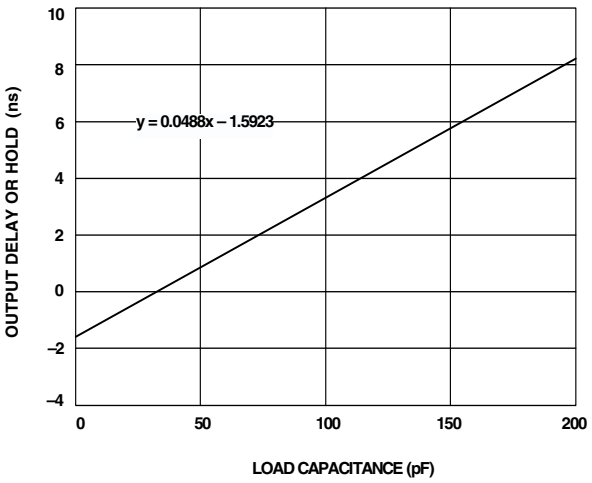

Figure 33. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

ENVIRONMENTAL CONDITIONS

The ADSP-2126x processor is rated for performance under T_{AMB} environmental conditions specified in the Operating Conditions on Page 14.

THERMAL CHARACTERISTICS

Table 38 and Table 39 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 38 and Table 39 (Ψ_{JMT} indicates moving air).

P_D = power dissipation. See *Estimating Power Dissipation for ADSP-21262 SHARC DSPs (EE-216)* for more information.

Values of θ_{JA} are provided for package comparison and PCB design considerations (θ_{JMA} indicates moving air). θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Table 38. Thermal Characteristics for 136-Ball BGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	31.0	°C/W
θ_{JMA}	Airflow = 1 m/s	27.3	°C/W
θ_{JMA}	Airflow = 2 m/s	26.0	°C/W
θ_{JC}		6.99	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.16	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.30	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.35	°C/W

Table 39. Thermal Characteristics for 144-Lead LQFP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	32.5	°C/W
θ_{JMA}	Airflow = 1 m/s	28.9	°C/W
θ_{JMA}	Airflow = 2 m/s	27.8	°C/W
θ_{JC}		7.8	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.5	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.8	°C/W
Ψ_{JMT}	Airflow = 2 m/s	1.0	°C/W

144-LEAD LQFP PIN CONFIGURATIONS

Table 40 shows the ADSP-2126x's pin names and their default function after reset (in parentheses).

Table 40. 144-Lead LQFP Pin Assignments

Pin Name	LQFP Pin No.	Pin Name	LQFP Pin No.	Pin Name	LQFP Pin No.	Pin Name	LQFP Pin No.
V_{DDINT}	1	V_{DDINT}	37	V_{DDEXT}	73	GND	109
CLK_CFG0	2	GND	38	GND	74	V_{DDINT}	110
CLK_CFG1	3	$\overline{RD}$	39	V_{DDINT}	75	GND	111
BOOT_CFG0	4	ALE	40	GND	76	V_{DDINT}	112
BOOT_CFG1	5	AD15	41	DAI_P10 (SD2B)	77	GND	113
GND	6	AD14	42	DAI_P11 (SD3A)	78	V_{DDINT}	114
V_{DDEXT}	7	AD13	43	DAI_P12 (SD3B)	79	GND	115
GND	8	GND	44	DAI_P13 (SCLK23)	80	V_{DDEXT}	116
V_{DDINT}	9	V_{DDEXT}	45	DAI_P14 (SFS23)	81	GND	117
GND	10	AD12	46	DAI_P15 (SD4A)	82	V_{DDINT}	118
V_{DDINT}	11	V_{DDINT}	47	V_{DDINT}	83	GND	119
GND	12	GND	48	GND	84	V_{DDINT}	120
V_{DDINT}	13	AD11	49	GND	85	$\overline{RESET}$	121
GND	14	AD10	50	DAI_P16 (SD4B)	86	$\overline{SPIDS}$	122
FLAG0	15	AD9	51	DAI_P17 (SD5A)	87	GND	123
FLAG1	16	AD8	52	DAI_P18 (SD5B)	88	V_{DDINT}	124
AD7	17	DAI_P1 (SD0A)	53	DAI_P19 (SCLK45)	89	SPICLK	125
GND	18	V_{DDINT}	54	V_{DDINT}	90	MISO	126
V_{DDINT}	19	GND	55	GND	91	MOSI	127
GND	20	DAI_P2 (SD0B)	56	GND	92	GND	128
V_{DDEXT}	21	DAI_P3 (SCLK0)	57	V_{DDEXT}	93	V_{DDINT}	129
GND	22	GND	58	DAI_P20 (SFS45)	94	V_{DDEXT}	130
V_{DDINT}	23	V_{DDEXT}	59	GND	95	A_{VDD}	131
AD6	24	V_{DDINT}	60	V_{DDINT}	96	A_{VSS}	132
AD5	25	GND	61	FLAG2	97	GND	133
AD4	26	DAI_P4 (SFS0)	62	FLAG3	98	$\overline{RESETOUT}$	134
V_{DDINT}	27	DAI_P5 (SD1A)	63	V_{DDINT}	99	$\overline{EMU}$	135
GND	28	DAI_P6 (SD1B)	64	GND	100	TDO	136
AD3	29	DAI_P7 (SCLK1)	65	V_{DDINT}	101	TDI	137
AD2	30	V_{DDINT}	66	GND	102	$\overline{TRST}$	138
V_{DDEXT}	31	GND	67	V_{DDINT}	103	TCK	139
GND	32	V_{DDINT}	68	GND	104	TMS	140
AD1	33	GND	69	V_{DDINT}	105	GND	141
AD0	34	DAI_P8 (SFS1)	70	GND	106	CLKIN	142
$\overline{WR}$	35	DAI_P9 (SD2A)	71	V_{DDINT}	107	XTAL	143
V_{DDINT}	36	V_{DDINT}	72	V_{DDINT}	108	V_{DDEXT}	144

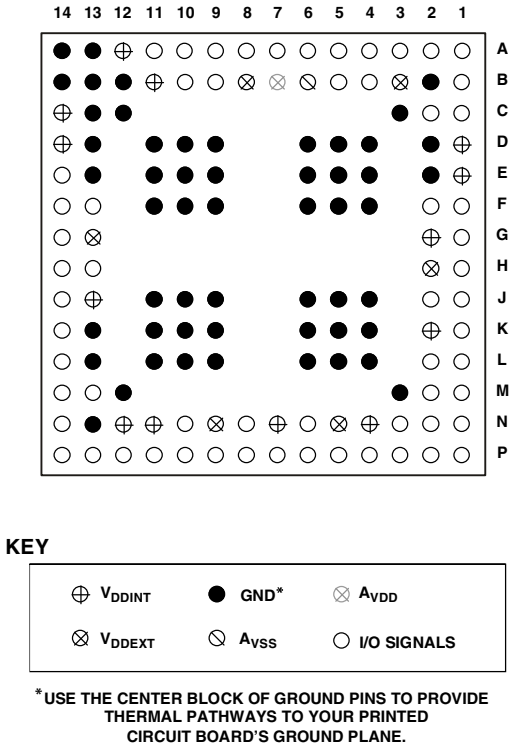

Figure 34. 136-Ball BGA Pin Assignments (Bottom View, Summary)

AUTOMOTIVE PRODUCTS

The ADSP-21261W and ADSP-21262W are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

ORDERING GUIDE

Analog Devices offers a wide variety of audio algorithms and combinations to run on the ADSP-21266 DSP. For a complete list, visit our website at www.analog.com/SHARC.

Model	Notes	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21261SKBCZ150	[2]	0°C to +70°C	150 MHz	1M bit	3M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21261SKSTZ150	[2]	0°C to +70°C	150 MHz	1M bit	3M bit	144-Lead LQFP	ST-144
ADSP-21262SBBC-150		–40°C to +85°C	150 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21262SBBCZ150	[2]	–40°C to +85°C	150 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21262SKBC-200		0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21262SKBCZ200	[2]	0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21262SKSTZ200	[2]	0°C to +70°C	200 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKSTZ-1B	[2, 3]	0°C to +70°C	150 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKSTZ-2B	[2, 3]	0°C to +70°C	200 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKBCZ-2B	[2, 3]	0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21266SKSTZ-1C	[2, 4]	0°C to +70°C	150 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKSTZ-2C	[2, 4]	0°C to +70°C	200 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKBCZ-2C	[2, 4]	0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1
ADSP-21266SKSTZ-1D	[2, 4]	0°C to +70°C	150 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKSTZ-2D	[2, 4]	0°C to +70°C	200 MHz	2M bit	4M bit	144-Lead LQFP	ST-144
ADSP-21266SKBCZ-2D	[2, 4]	0°C to +70°C	200 MHz	2M bit	4M bit	136-Ball CSP_BGA	BC-136-1

[1] Referenced temperature is ambient temperature.
[2] Z = RoHS Compliant Part.
[3] B at end of part number indicates Rev. 0.1 silicon. See Table 3 on Page 4 for multichannel surround sound decoder algorithms in on-chip B ROM.
[4] C and D at end of part number indicate Rev. 0.2 silicon. See Table 3 on Page 4 for multichannel surround sound decoder algorithms in on-chip C and D ROM.