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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643lf2mlq1r

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- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processing channel.

1.5.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow block for test, censorship device and user option bits
- Wait states:
  - 3 wait states for frequencies =< 120 MHz
  - 2 wait states for frequencies =< 80 MHz
  - 1 wait state for frequencies =< 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-chip SRAM with ECC

The MPC5643L SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 128 KB
- ECC on 32-bit word (syndrome of 7 bits)
  - ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection
- Wait states:
  - 1 wait state for frequencies =< 120 MHz
  - 0 wait states for frequencies =< 80 MHz

1.5.7 Platform flash memory controller

The following list summarizes the key features of the flash memory controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.

The BAM provides the following features:

- Enables booting via serial mode (FlexCAN or LINFlex-UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either Power Architecture code (default) or Freescale VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.5.25 System Status and Configuration Module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as Freescale VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features

  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1 Rev. A
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit or receive
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO
- Message buffer header, status, and payload data stored in system memory (SRAM)
- Internal FlexRay memories have error detection and correction

1.5.28 Serial communication interface module (LINFlexD)

The LINFlexD module (LINFlex with DMA support) on this device features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 50-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, 16-bit, or 17-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
122	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
123	JCOMP	—	—	JCOMP
124	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
125	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
126	$V_{DD\_HV\_IO}$	—		
127	$V_{SS\_HV\_IO}$	—		
128	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
129	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
130	$V_{DD\_HV\_REG\_2}$	—		
131	$V_{DD\_LV\_COR}$	—		
132	$V_{SS\_LV\_COR}$	—		
133	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD\_LV\_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS\_LV\_COR}$	—		
138	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
139	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—
140	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
141	FCCU_F[1]	FCCU	F[1]	F[1]
142	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
143	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]

Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
144	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1 V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 4. 257 MAPBGA pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
A1	$V_{SS\_HV\_IO\_RING}$	—		
A2	$V_{SS\_HV\_IO\_RING}$	—		
A3	$V_{DD\_HV\_IO\_RING}$	—		
A4	H[2]	SIUL	GPIO[114]	GPIO[114]
		NPC	MDO[5]	—
A5	H[0]	SIUL	GPIO[112]	GPIO[112]
		NPC	MDO[7]	—
A6	G[14]	SIUL	GPIO[110]	GPIO[110]
		NPC	MDO[9]	—
A7	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
A8	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
A9	$V_{DD\_HV\_IO\_RING}$	—		
A10	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
G1	H[3]	SIUL	GPIO[115]	GPIO[115]
		NPC	MDO[4]	—
G2	$V_{DD\_HV\_IO\_RING}$	—		
G3	C[5]	SIUL	GPIO[37]	GPIO[37]
		DSPI_0	SCK	SCK
		SSCM	DEBUG[5]	—
		FlexPWM_0	—	FAULT[3]
		SIUL	—	EIRQ[23]
G4	A[6]	SIUL	GPIO[6]	GPIO[6]
		DSPI_1	SCK	SCK
		SIUL	—	EIRQ[6]
G6	$V_{DD\_LV\_CORE\_RING}$	—		
G7	$V_{SS\_LV\_CORE\_RING}$	—		
G8	$V_{SS\_LV\_CORE\_RING}$	—		
G9	$V_{SS\_LV\_CORE\_RING}$	—		
G10	$V_{SS\_LV\_CORE\_RING}$	—		
G11	$V_{SS\_LV\_CORE\_RING}$	—		
G12	$V_{DD\_LV\_CORE\_RING}$	—		
G14	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
G15	H[13]	SIUL	GPIO[125]	GPIO[125]
		FlexPWM_1	X[3]	X[3]
		eTimer_2	ETC[3]	ETC[3]
G16	H[9]	SIUL	GPIO[121]	GPIO[121]
		FlexPWM_1	B[1]	B[1]
		DSPI_0	CS7	—
G17	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
H1	G[13]	SIUL	GPIO[109]	GPIO[109]
		NPC	MDO[10]	—
H2	$V_{SS\_HV\_IO\_RING}$	—		

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	—	M	S		118	A13
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1						
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0						
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0						
		SIUL	—	—	EIRQ[9]	—						
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	—	M	S		120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	—	M	S		122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
B[1]	PCR[17]	SIUL	GPIO[17]	ALT0	GPIO[17]	—	—	M	S		110	C14
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=0						
		SSCM	DEBUG[1]	ALT3	—	—						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=1						
		SIUL	—	—	EIRQ[16]	—						
B[2]	PCR[18]	SIUL	GPIO[18]	ALT0	GPIO[18]	—	—	M	S		114	A14
		LINFlexD_0	TXD	ALT1	—	—						
		SSCM	DEBUG[2]	ALT3	—	—						
		SIUL	—	—	EIRQ[17]	—						
B[3]	PCR[19]	SIUL	GPIO[19]	ALT0	GPIO[19]	—	—	M	S		116	B13
		SSCM	DEBUG[3]	ALT3	—	—						
		LINFlexD_0	—	—	RXD	PSMI[31]; PADSEL=0						
B[4][2]	PCR[20]	SIUL	GPIO[20]	ALT0	GPIO[20]	—	—	F	S		89	L17
		JTAGC	TDO	ALT1	—	—						
B[5]	PCR[21]	SIUL	GPIO[21]	ALT0	GPIO[21]	—	Pull up	M	S		86	M15
		JTAGC	—	—	TDI	—						
B[6]	PCR[22]	SIUL	GPIO[22]	ALT0	GPIO[22]	—	—	F	S		138	B3
		MC_CGM	clk_out	ALT1	—	—						
		DSPI_2	CS2	ALT2	—	—						
		SIUL	—		EIRQ[18]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
G[9]	PCR[105]	SIUL	GPIO[105]	ALT0	GPIO[105]	—	—	M	S		79	R17
		FlexRay	DBG1	ALT1	—	—						
		DSPI_1	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=2						
		SIUL	—	—	EIRQ[29]	—						
G[10]	PCR[106]	SIUL	GPIO[106]	ALT0	GPIO[106]	—	—	M	S		77	P15
		FlexRay	DBG2	ALT1	—	—						
		DSPI_2	CS3	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=1						
G[11]	PCR[107]	SIUL	GPIO[107]	ALT0	GPIO[107]	—	—	M	S		75	U15
		FlexRay	DBG3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=2						
G[12]	PCR[108]	SIUL	GPIO[108]	ALT0	GPIO[108]	—	—	F	S		—	F2
		NPC	MDO[11]	ALT2	—	—						
G[13]	PCR[109]	SIUL	GPIO[109]	ALT0	GPIO[109]	—	—	F	S		—	H1
		NPC	MDO[10]	ALT2	—	—						
G[14]	PCR[110]	SIUL	GPIO[110]	ALT0	GPIO[110]	—	—	F	S		—	A6
		NPC	MDO[9]	ALT2	—	—						
G[15]	PCR[111]	SIUL	GPIO[111]	ALT0	GPIO[111]	—	—	F	S		—	J2
		NPC	MDO[8]	ALT2	—	—						
Port H												
H[0]	PCR[112]	SIUL	GPIO[112]	ALT0	GPIO[112]	—	—	F	S		—	A5
		NPC	MDO[7]	ALT2	—	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	—	M	S		—	C12
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1						
		DSPI_0	CS5	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[1]	—						
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	—	M	S		—	F16
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1						
		DSPI_0	CS6	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[2]	—						
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	—	M	S		—	E17
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1						
		DSPI_0	CS7	ALT2	—	—						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexPWM_1	—	—	FAULT[3]	—						
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	—	F	S		—	K3
		NPC	$\overline{\text{RDY}}$	ALT2	—	—						

1 Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay)

2 The default function of this pin out of reset is ALT1 (TDO).

3 Analog

NOTE

Open Drain can be configured by the PCRn for all pins used as output (except FCCU_F[0] and FCCU_F[1]).

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 120 MHz. The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “CC” identifies controller characteristics—indicating the characteristics and timing of the signals that the chip provides.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 8. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	3.63[2, 3]	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADR0}$[3,4] $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADR0}$ $V_{SS\_HV\_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	3.63[2, 3]	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V

Table 11. Thermal characteristics for 144 LQFP package[1]

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection[2]	Single layer board – 1s	44	°C/W
			Four layer board – 2s2p	36	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	35	°C/W
			Four layer board – 2s2p	30	
$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	24	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case[4]	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 12. Thermal characteristics for 257 MAPBGA package[1]

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient natural convection[2]	Single layer board – 1s	46	°C/W
			Four layer board – 2s2p	26	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	37	°C/W
			Four layer board – 2s2p	22	
$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	13	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case[4]	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 22. Main oscillator electrical characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
$g_{mXOSCHS}$	P	Oscillator transconductance	V_{DD} = 3.3 V ±10%	4.5	—	13.25	mA/V
V_{XOSCHS}	D	Oscillation amplitude	f_{OSC} = 4, 8, 10, 12, 16 MHz	1.3	—	—	V
			f_{OSC} = 40 MHz	1.1	—	—	
$V_{XOSCHSOP}$	D	Oscillation operating point	—	—	0.82	—	V
$T_{XOSCHSSU}$	T	Oscillator start-up time	f_{OSC} = 4, 8, 10, 12 MHz[2]	—	—	6	ms
			f_{OSC} = 16, 40 MHz[2]	—	—	2	
V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

1 V_{DD} = 3.3 V ±10%, T_J = –40 to +150 °C, unless otherwise specified.

2 The recommended configuration for maximizing the oscillator margin are:
XOSC_MARGIN = 0 for 4 MHz quartz
XOSC_MARGIN = 1 for 8/16/40 MHz quartz

3.13 FMPLL electrical characteristics

Table 23. FMPLL electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{REF\_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range[1]	Crystal reference	4	—	40	MHz
f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	4	—	120[2]	MHz
f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	20	—	150	MHz
f_{sys}	D	On-chip FMPLL frequency[2]	—	16	—	120	MHz
t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window[3]	Lower limit	1.6	—	3.7	MHz
			Upper limit	24	—	56	
f_{SCM}	D	Self-clocked mode frequency[4,5]	—	20	—	150	MHz
t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{p2} being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_{p2} + CS equal to 7.5 pF, a resistance of 133 kΩ is obtained (R_{EQ} = 1 / (fS*(C_{p2}+C_S)), where fS represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_s) and the sum of R_S + R_F, the external circuit must be designed to respect the Equation 4:

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 4}$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

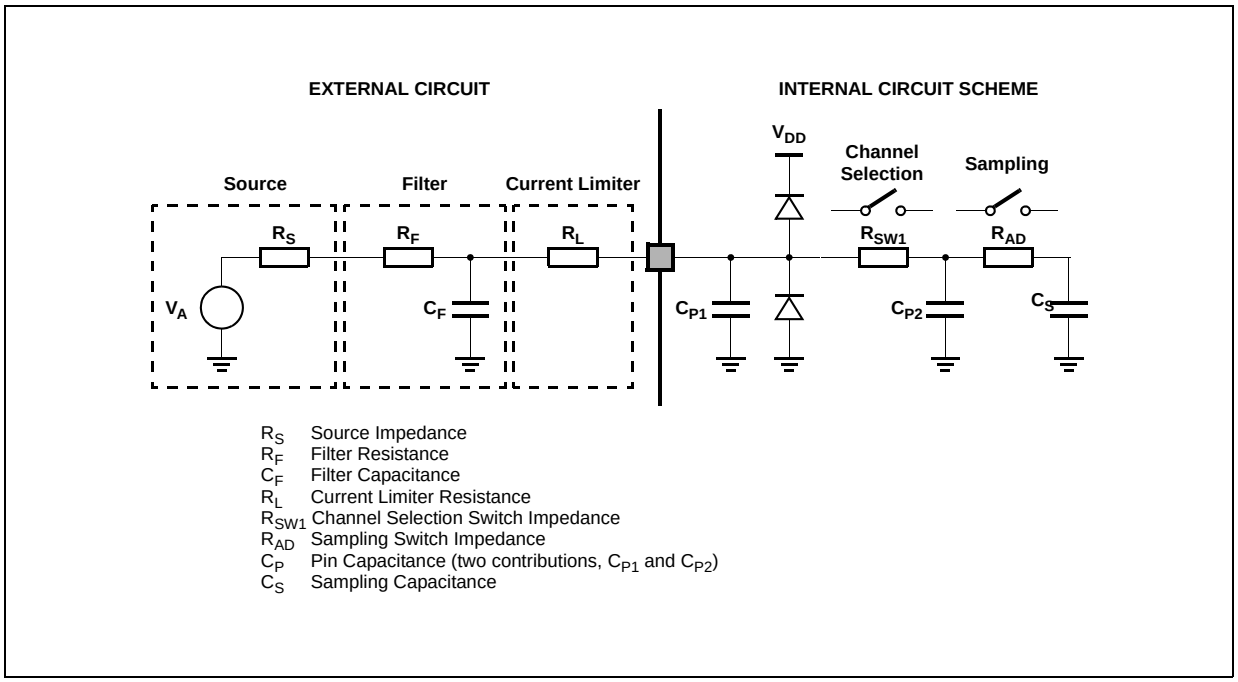

Figure 8. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 8): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

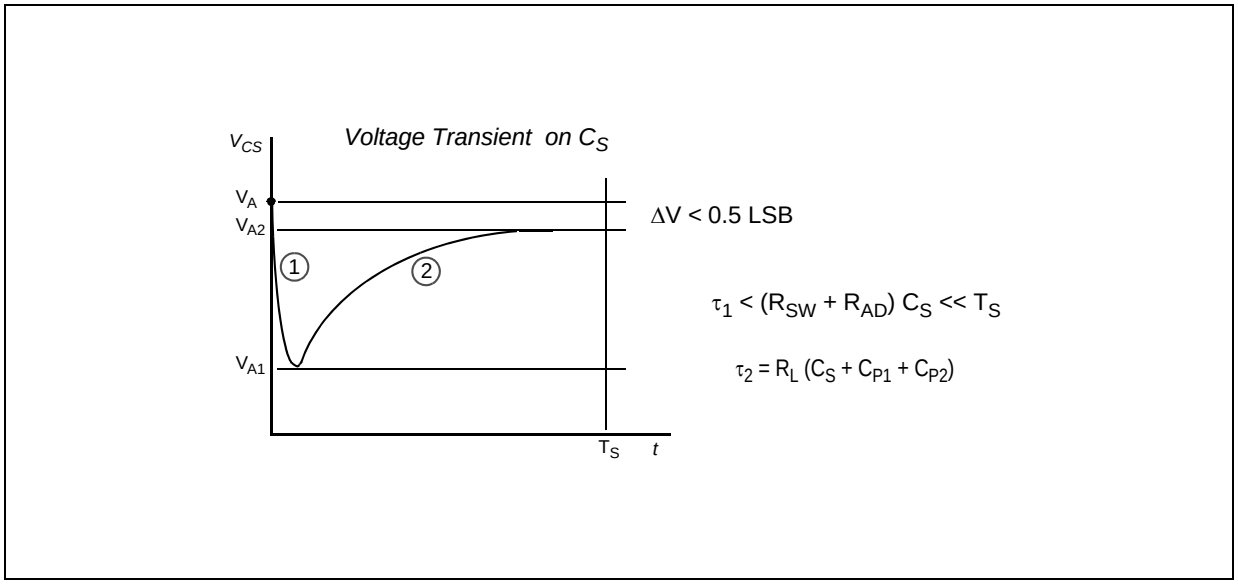

Figure 9. Transient Behavior during Sampling Phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S} \qquad \textit{Eqn. 5}$$

  Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S \qquad \textit{Eqn. 6}$$

  The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2}) \qquad \textit{Eqn. 7}$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2}) \qquad \textit{Eqn. 8}$$

  In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S \qquad \textit{Eqn. 9}$$

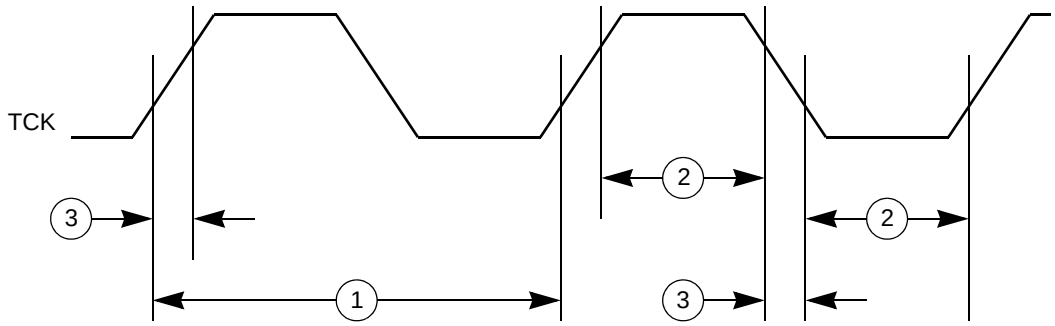

Figure 22. JTAG test clock input timing

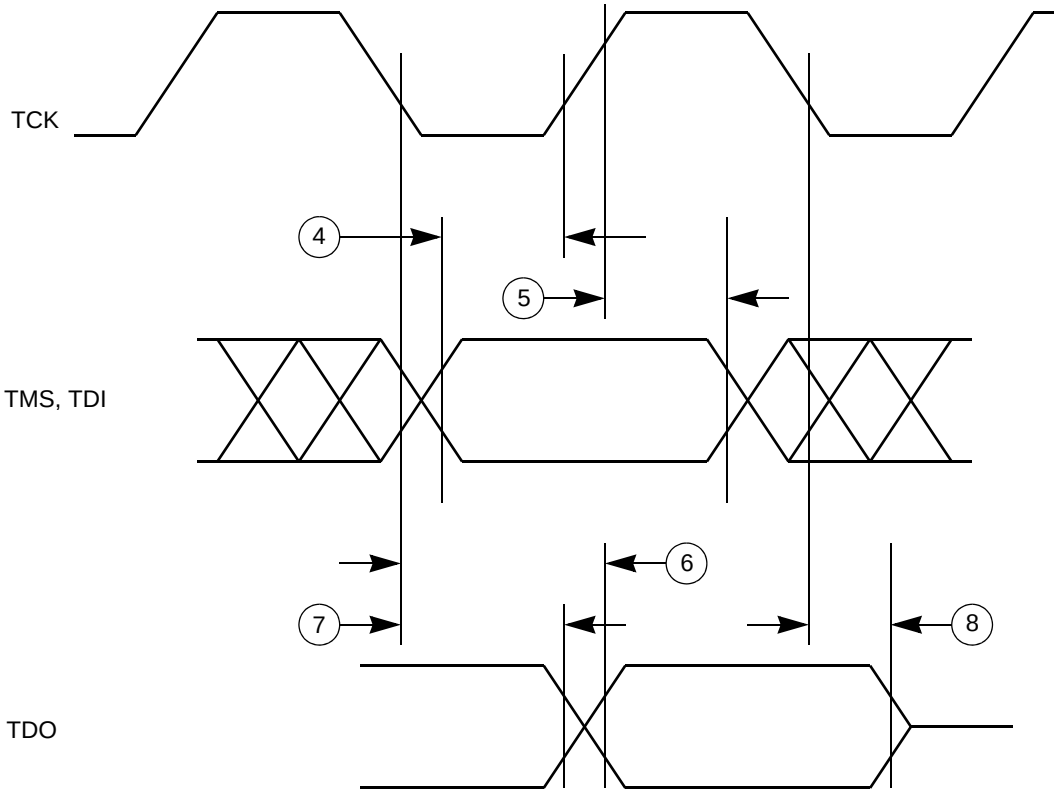

Figure 23. JTAG test access port timing

Table 41. Revision history (continued)

Revision	Date	Description of changes
4	2 Mar 2010	Editorial changes and improvements. Revised the 257-pin package pin pitch (was 1.4 mm, is 0.8 mm). In the Overview section: • Renamed the peripheral bridge to “PBRIDGE”. • Revised the information for FlexRay. • Revised the “Clock, reset, power, mode and test control module” section. • Revised the “Platform memory access time summary” table and replaced TBDs by meaningful values. Extensive revisions to signal descriptions and pin muxing information. In the “ conditions (3.3 V)” table, changed the specification for $V_{DD\_HV\_ADR0}$ and $V_{DD\_HV\_ADR1}$ (was “...3.3 V”, is “...3.6 V”). Revised the “EMI testing specifications” table. In the “HPREG1, HPREG2, Main LVDs, Digital HVD, and Digital LVD electrical specifications” table, added a specification for the digital low voltage detector upper threshold. Revised the “FMPLL electrical characteristics” table. In the “Main oscillator electrical characteristics” table, changed the maximum specification for $g_{mXOSCHS}$ (was 11 mA/V, is 11.8 mA/V). Revised the “ADC electrical characteristics” section. In the “ADC conversion characteristics” table: • Changed the t_{ADC_S} specification (was TBD, is minimum of 383 ns). • Added the footnote “No missing codes” to the DNL specification. • Added specifications for SNR, THD, SINAD, and ENOB. Revised the “Ordering information” section.

Table 41. Revision history (continued)

Revision	Date	Description of changes
6 (cont.)	11 Mar 2011 (cont.)	Added “WKUP/NMI Timing” subsection and “WKUP/NMI Glitch Filter” table to the “AC timing characteristics” section. Added “Nexus DDR Mode output timing” table to the “Nexus timing” section. Removed the “CLKOUT” diagram from the “External interrupt timing (IRQ pin)” section as it is not relevant. Corrected an error in the IRQ timing in the “External interrupt timing” figure. Updated the t_{SDC} parameters in the “DSPI timing” table. Renamed the “Electromagnetic Interference (EMI) characteristics” section (is “Electromagnetic Interference (EMI) characteristics (cut1)”) and revised all information in that section. In the “Voltage regulator electrical characteristics” section, added the BCX68 from Infineon to the list of supported transistors. Revised the “Voltage regulator electrical specifications” table to include cut1 and cut2 information. Renamed the “Supply current characteristics” section (is “Supply current characteristics (cut2)”) and revised it to show meaningful data. In the footnotes of the “Main oscillator electrical characteristics” table, changed SELMARGIN to XOSC_MARGIN. In the “ADC conversion characteristics” table: • Changed “LSB” to “Counts”. • Created separate rows for the TUE specifications. Added bullet regarding HALT and STOP in the “Clock, reset, power, mode and test control modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)“ subsection of the “Features“ section. In the “Analog-to-Digital Converter module“ subsection of the “Feature Details” section, changed “Motor control mode“ to “CTU mode“ to be consistent with the nomenclature used in the Reference Manual. Updated the JCOMP entries in the “Pin function summary“ table. Added footnotes regarding pad pull devices to NMI, TMS, TCK, and JCOMP in the “System pins“ table. Added “Time constant of RC filter at LVD input” parameters to the “Main supply LVD (LVD Main) specifications“ table. In the “Supply current characteristics (cut2)“ table: • Changed “$I_{DD\_LV\_MAX}$” to “$I_{DD\_LV\_MAX}$“; • Removed all “40-120 MHz” frequency ranges from the “Conditions” column; • Updated the “Max” values column; • Added parameter “$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$“ with “P” classification and special footnote; • Changed all “25°C“ temperature conditions to “ambient”; • Added “T_J = 150 °C“ condition to parameters $I_{DD\_HV\_ADC}$, $I_{DD\_HV\_AREF}$, $I_{DD\_HV\_OSC}$, and $I_{DD\_HV\_FLASH}$. Changed the timing diagram in the “Main oscillator electrical characteristics” section to reference MTRANS assertion instead of V_{DDMIN}. Updated the jitter specs in the “FMPLL electrical characteristics“ table. In the “ADC conversion characteristics“ table, changed all parameters with units of “counts” to units of “LSB” and updated Min/Max values. Changed $I_{DD\_LV\_BIST}$ + $I_{DD\_LV\_PLL}$ operating current (for both cases) to TBD. In the “Supply current characteristics (cut2)” section, added a footnote that $I_{DD\_HV\_ADC}$ and $I_{DD\_HV\_AREF}$ represent the total current of both ADCs in the “Current consumption characteristics” table.