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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz
Connectivity	CANbus, FlexRay, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643lf2mlq8r

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5643L series of microcontroller units (MCUs). For functional characteristics, see the *MPC5643L Microcontroller Reference Manual*. For use of the MPC5643Lin a fail-safe system according to safety standard ISO26262, see the *Safety Application Guide for MPC5643L*.

1.2 Description

The MPC5643L series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The MPC5643L family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the MPC5643L automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users' implementations.

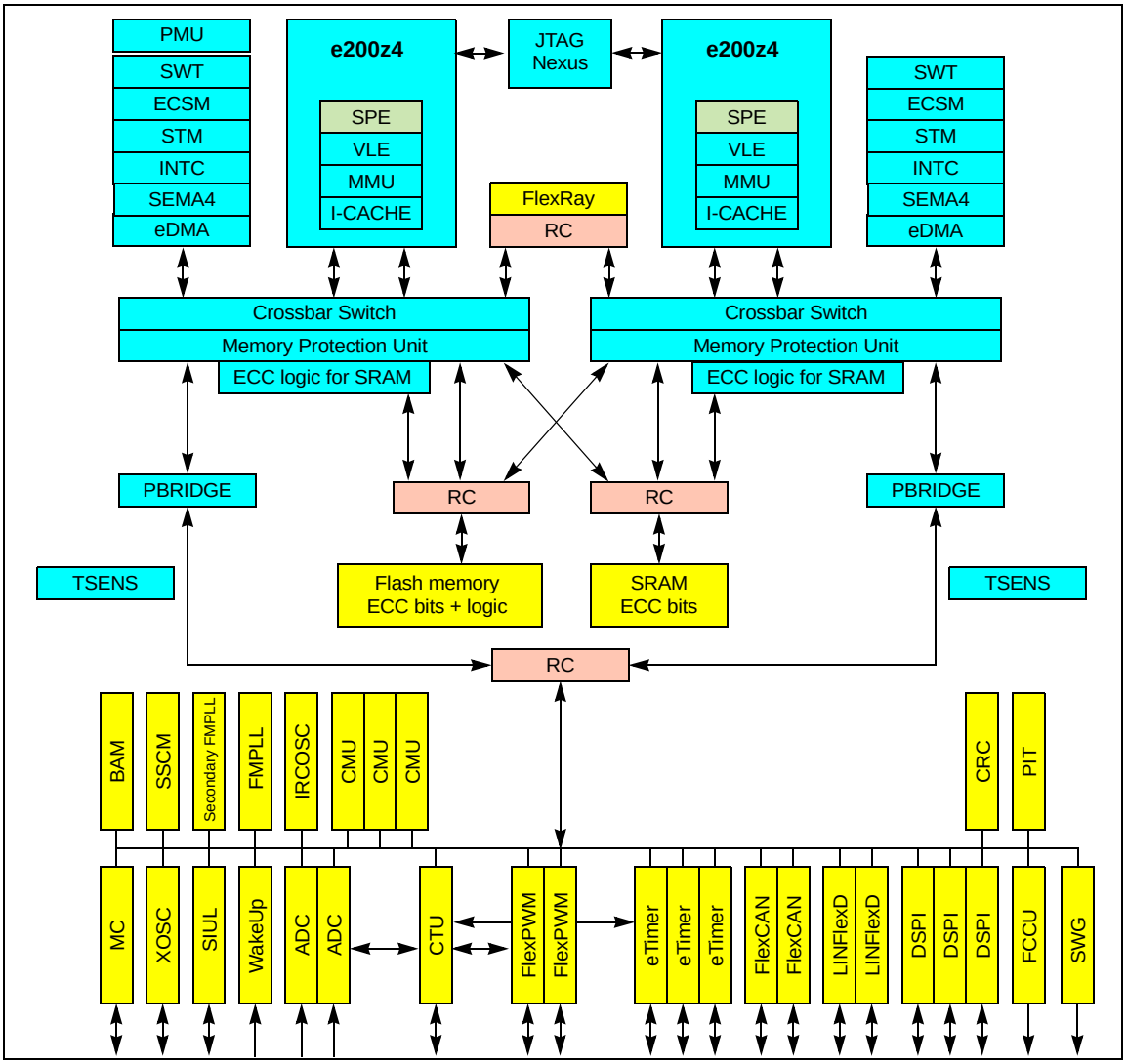
1.3 Device comparison

Table 1. MPC5643L device summary

Feature		MPC5643L
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)
	Architecture	Harvard
	Execution speed	0–120 MHz (+2% FM)
	DMIPS intrinsic performance	>240 MIPS
	SIMD (DSP + FPU)	Yes
	MMU	16 entry
	Instruction set PPC	Yes
	Instruction set VLE	Yes
	Instruction cache	4 KB, EDC
	MPU-16 regions	Yes, replicated module
	Semaphore unit (SEMA4)	Yes
Buses	Core bus	AHB, 32-bit address, 64-bit data
	Internal periphery bus	32-bit address, 32-bit data
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3

Table 1. MPC5643L device summary (continued)

Feature		MPC5643L
Memory	Flash	1 MB, ECC, RWW
	Static RAM (SRAM)	128 KB, ECC
Modules	Interrupt Controller (INTC)	16 interrupt levels, replicated module
	Periodic Interrupt Timer (PIT)	1 × 4 channels
	System Timer Module (STM)	1 × 4 channels, replicated module
	Software Watchdog Timer (SWT)	Yes, replicated module
	eDMA	16 channels, replicated module
	FlexRay	1 × 64 message buffers, dual channel
	FlexCAN	2 × 32 message buffers
	LINFlexD (UART and LIN with DMA support)	2
	Clock out	Yes
	Fault Collection and Control Unit (FCCU)	Yes
	Cross Triggering Unit (CTU)	Yes
	eTimer	3 × 6 channels[1]
	FlexPWM	2 Module 4 × (2 + 1) channels[2]
	Analog-to-Digital Converter (ADC)	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)
	Sine Wave Generator (SWG)	32 point
Modules (cont.)	Deserial Serial Peripheral Interface (DSPI)	3 × DSPI as many as 8 chip selects
	Cyclic Redundancy Checker (CRC) unit	Yes
	Junction temperature sensor (TSENS)	Yes, replicated module
	Digital I/Os	≥ 16
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2
	Internal RC oscillator	16 MHz
	External crystal oscillator	4 – 40 MHz
Debug	Nexus	Level 3+



ADC – Analog-to-Digital Converter
BAM – Boot Assist Module
CMU – Clock Monitoring Unit
CRC – Cyclic Redundancy Check unit
CTU – Cross Triggering Unit
DSPI – Serial Peripherals Interface
ECC – Error Correction Code
ECSM – Error Correction Status Module
eDMA – Enhanced Direct Memory Access controller
FCCU – Fault Collection and Control Unit
FlexCAN – Controller Area Network controller
FMPLL – Frequency Modulated Phase Locked Loop
INTC – Interrupt Controller
IRCOSC – Internal RC Oscillator
JTAG – Joint Test Action Group interface
LINFlexD – LIN controller with DMA support
MC – Mode Entry, Clock, Reset, & Power
PBRIDGE – Peripheral bridge
PIT – Periodic Interrupt Timer
PMU – Power Management Unit
RC – Redundancy Checker
RTC – Real Time Clock
SEMA4 – Semaphore Unit
SIUL – System Integration Unit Lite
SSCM – System Status and Configuration Module
STM – System Timer Module
SWG – Sine Wave Generator
SWT – Software Watchdog Timer
TSENS – Temperature Sensor
XOSC – Crystal Oscillator

Figure 1. MPC5643L block diagram

Table 2. Platform memory access time summary (continued)

AHB transfer	Data phase wait states	Description
e200z4d data write	0	SRAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d data write	0–2	SRAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d flash memory read	0	Flash memory prefetch buffer hit (page hit)
e200z4d flash memory read	3	Flash memory prefetch buffer miss (at 120 MHz; includes 1 cycle of program flash memory controller arbitration)

1.5.10 Error Correction Status Module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory
- ECC error reporting for SRAM
- ECC error injection for SRAM

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
B6	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
B7	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
B8	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
B9	$V_{SS\_HV\_IO\_RING}$	—		
B10	H[12]	SIUL	GPIO[124]	GPIO[124]
		FlexPWM_1	B[2]	B[2]
B11	E[15]	SIUL	GPIO[79]	GPIO[79]
		DSPI_0	CS1	—
		SIUL	—	EIRQ[27]
B12	E[14]	SIUL	GPIO[78]	GPIO[78]
		eTimer_1	ETC[5]	ETC[5]
		SIUL	—	EIRQ[26]
B13	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	—
		LINFlexD_0	—	RXD
B14	F[13]	SIUL	GPIO[93]	GPIO[93]
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[31]
B15	B[0]	SIUL	GPIO[16]	GPIO[16]
		FlexCAN_0	TXD	—
		eTimer_1	ETC[2]	ETC[2]
		SSCM	DEBUG[0]	—
		SIUL	—	EIRQ[15]
B16	$V_{DD\_HV\_IO\_RING}$	—		
B17	$V_{SS\_HV\_IO\_RING}$	—		
C1	$V_{DD\_HV\_IO\_RING}$	—		

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C16	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
C17	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
D1	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
D2	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—
D3	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]
D4	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
D5	$V_{SS\_LV\_CORE\_RING}$	—		
D6	$V_{DD\_LV\_CORE\_RING}$	—		
D7	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
D8	$V_{DD\_HV\_IO\_RING}$	—		
D9	$V_{SS\_HV\_IO\_RING}$	—		
D10	Not connected	—		

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S		84	N16
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0						
		MC_RGM	—	—	ABS[0]	—						
		SIUL	—	—	EIRQ[2]	—						
A[3]	PCR[3]	SIUL	GPIO[3]	ALT0	GPIO[3]	—	Pull down	M	S		92	K17
		eTimer_0	ETC[3]	ALT1	ETC[3]	PSMI[38]; PADSEL=0						
		DSPI_2	CS0	ALT2	CS0	PSMI[3]; PADSEL=0						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=0						
		MC_RGM	—	—	ABS[2]	—						
		SIUL	—	—	EIRQ[3]	—						
A[4]	PCR[4]	SIUL	GPIO[4]	ALT0	GPIO[4]	—	Pull down	M	S		108	C16
		eTimer_1	ETC[0]	ALT1	ETC[0]	PSMI[9]; PADSEL=0						
		DSPI_2	CS1	ALT2	—	—						
		eTimer_0	ETC[4]	ALT3	ETC[4]	PSMI[7]; PADSEL=0						
		MC_RGM	—	—	FAB	—						
		SIUL	—	—	EIRQ[4]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
F[11]	PCR[91]	SIUL	GPIO[91]	ALT0	GPIO[91]	—	—	M	S		25	L2
		NPC	—	ALT2	$\overline{\text{EVTI}}$	—						
F[12]	PCR[92]	SIUL	GPIO[92]	ALT0	GPIO[92]	—	—	M	S		106	C17
		eTimer_1	ETC[3]	ALT1	ETC[3]	PSMI[12]; PADSEL=2						
		SIUL	—	—	EIRQ[30]	—						
F[13]	PCR[93]	SIUL	GPIO[93]	ALT0	GPIO[93]	—	—	M	S		112	B14
		eTimer_1	ETC[4]	ALT1	ETC[4]	PSMI[13]; PADSEL=3						
		SIUL	—	—	EIRQ[31]	—						
F[14]	PCR[94]	SIUL	GPIO[94]	ALT0	GPIO[94]	—	—	M	S		115	C13
		LINFlexD_1	TXD	ALT1	—	—						
F[15]	PCR[95]	SIUL	GPIO[95]	ALT0	GPIO[95]	—	—	M	S		113	D13
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=2						
FCCU												
FCCU_F[0]	—	FCCU	F[0]	ALT0	F[0]	—	—	S	S		38	R2
FCCU_F[1]	—	FCCU	F[1]	ALT0	F[1]	—	—	S	S		141	C4
Port G												
G[2]	PCR[98]	SIUL	GPIO[98]	ALT0	GPIO[98]	—	—	M	S		102	E16
		FlexPWM_0	X[2]	ALT1	X[2]	PSMI[29]; PADSEL=1						
		DSPI_1	CS1	ALT2	—	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
G[3]	PCR[99]	SIUL	GPIO[99]	ALT0	GPIO[99]	—	—	M	S		104	D17
		FlexPWM_0	A[2]	ALT1	A[2]	PSMI[22]; PADSEL=2						
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=3						
G[4]	PCR[100]	SIUL	GPIO[100]	ALT0	GPIO[100]	—	—	M	S		100	F17
		FlexPWM_0	B[2]	ALT1	B[2]	PSMI[26]; PADSEL=2						
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=3						
G[5]	PCR[101]	SIUL	GPIO[101]	ALT0	GPIO[101]	—	—	M	S		85	N17
		FlexPWM_0	X[3]	ALT1	X[3]	PSMI[30]; PADSEL=2						
		DSPI_2	CS3	ALT2	—	—						
G[6]	PCR[102]	SIUL	GPIO[102]	ALT0	GPIO[102]	—	—	M	S		98	G17
		FlexPWM_0	A[3]	ALT1	A[3]	PSMI[23]; PADSEL=3						
G[7]	PCR[103]	SIUL	GPIO[103]	ALT0	GPIO[103]		—	M	S		83	P17
		FlexPWM_0	B[3]	ALT1	B[3]	PSMI[27]; PADSEL=3						
G[8]	PCR[104]	SIUL	GPIO[104]	ALT0	GPIO[104]	—	—	M	S		81	P16
		FlexRay	DBG0	ALT1	—	—						
		DSPI_0	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=2						
		SIUL	—	—	EIRQ[21]	—						

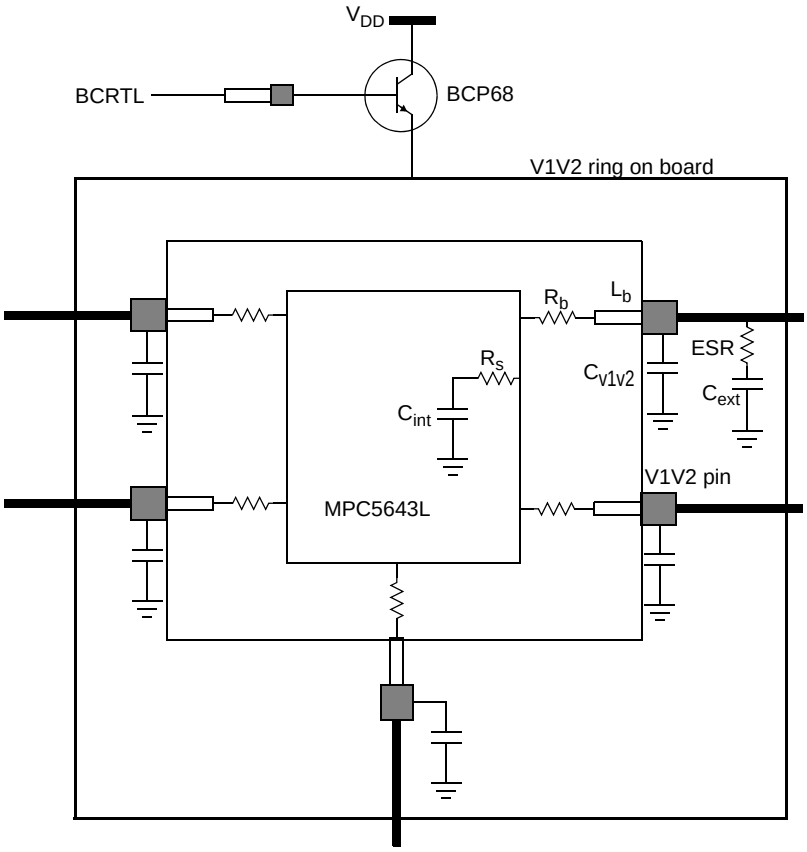


Figure 4. BCP68 board schematic example

NOTE

The minimum value of the ESR is constrained by the resonance caused by the external components, bonding inductance, and internal decoupling. The minimum ESR is required to avoid the resonance and make the regulator stable.

3.9 DC electrical characteristics

Table 19 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IOx}$ < 3.6 V).

Table 19. DC electrical characteristics[1]

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1[2]	—	—	V
V_{IL}	P	Maximum level input voltage	—	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	—	V
V_{IH}	D	Maximum high level input voltage	—	—	—	$V_{DD\_HV\_IOx}$ + 0.1[2,3]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V

Table 20. Current consumption characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$[2]	T	Operating current	1.2V supplies Tj=105°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	189	mA
			1.2V supplies Tj=125°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	214	mA
			1.2V supplies Tj=150°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	235	mA
$I_{DD\_LV\_STOP}$	T	Operating current in V_{DD} STOP mode	T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	20	mA
	T		T_J = 55 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	57	
	P		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	105	
$I_{DD\_LV\_HALT}$	T	Operating current in V_{DD} HALT mode	T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	25	mA
	T		T_J = 55 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	64	
	P		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	115	
$I_{DD\_HV\_ADC}$[3,4]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_ADC}$ = 3.6 V	—	—	10	mA
$I_{DD\_HV\_AREF}$[4]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_REF}$ = 3.6 V	—	—	3	mA
			T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_REF}$ = 5.5 V	—	—	5	

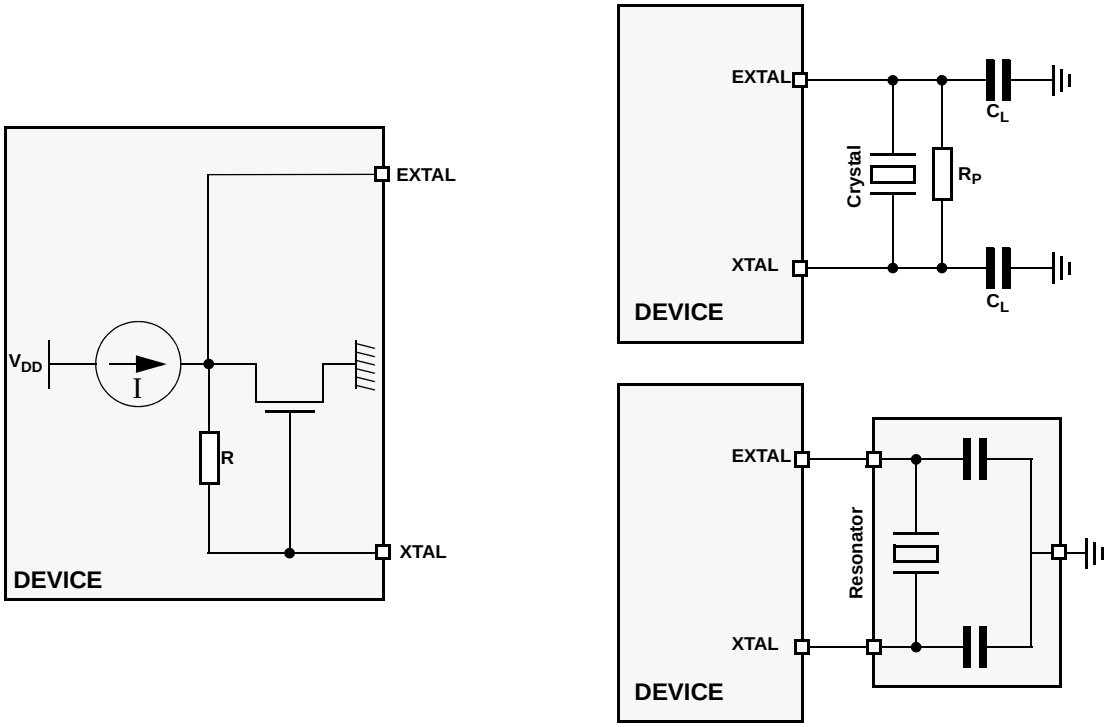


Figure 5. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

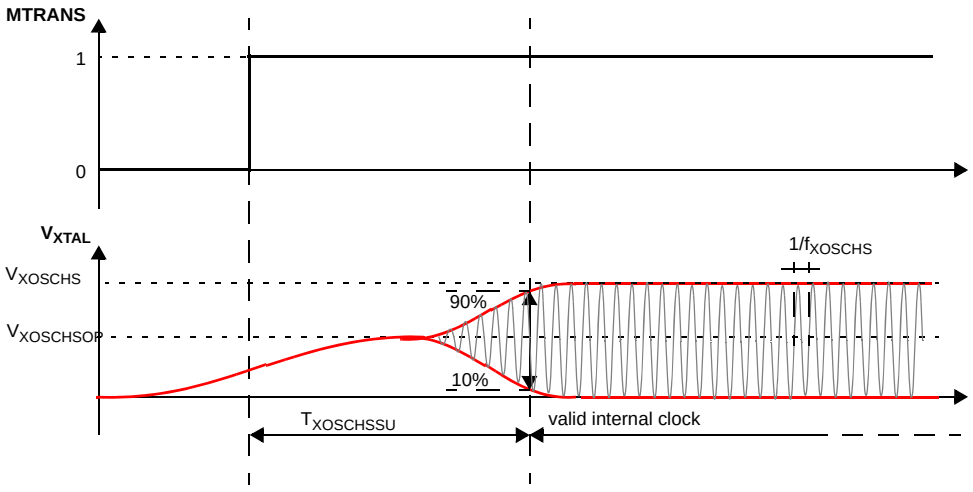


Figure 6. Main oscillator electrical characteristics

conditions as well as the reset trigger mapping to the different reset sequences is specified in Section 3.19.3, Reset sequence trigger mapping.

With the beginning of DRUN mode the first instruction is fetched and executed. At this point application execution starts and the internal reset sequence is finished.

The figures below show the internal states of the chip during the execution of the reset sequence and the possible states of the signal pin $\overline{\text{RESET}}$.

NOTE

$\overline{\text{RESET}}$ is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the chip internal reset circuitry. A high level on this pin can only be generated by an external pull up resistor which is strong enough to overdrive the weak internal pull down resistor. The rising edge on $\overline{\text{RESET}}$ in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in table Table 31 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping $\overline{\text{RESET}}$ asserted low beyond the last PHASE3.

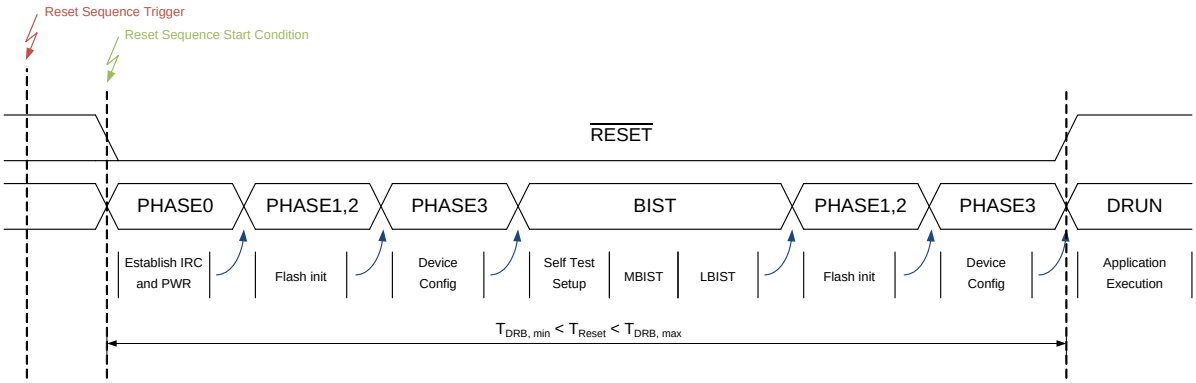


Figure 12. Destructive Reset Sequence, BIST enabled

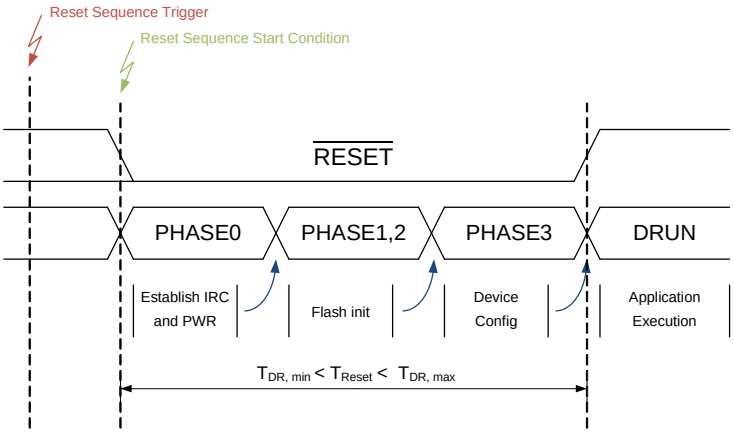


Figure 13. Destructive Reset Sequence, BIST disabled

The reset sequences shown in Figure 15 and Figure 16 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence[1].

3.19.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences. It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in Table 31.

Table 32. Reset sequence trigger — reset sequence

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive Reset Sequence, BIST enabled[1]	*Destructive Reset Sequence, BIST disabled*[1]	*External Reset Sequence Long, BIST enabled*	*Functional Reset Sequence Long*	*Functional Reset Sequence Short*
All internal destructive reset sources (LVDs or internal HVD during power-up and during operation)	Section 3.19.4.1, Destructive reset	Release of $\overline{\text{RESET}}$[2]	triggers		cannot trigger	cannot trigger	cannot trigger
Assertion of $\overline{\text{RESET}}$[3]	Section 3.19.4.2, External reset via RESET		cannot trigger		triggers[4]	triggers[5]	triggers[6]
All internal functional reset sources configured for long reset	Sequence starts with internal reset trigger	Release of $\overline{\text{RESET}}$[7]	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset			cannot trigger		cannot trigger	cannot trigger	triggers

1 Whether BIST is executed or not depends on the chip configuration data stored in the shadow sector of the NVM.

2 End of the internal reset sequence (as specified in Table 31) can only be observed by release of $\overline{\text{RESET}}$ if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 till $\overline{\text{RESET}}$ is released externally.

3 The assertion of $\overline{\text{RESET}}$ can only trigger a reset sequence if the device was running ($\overline{\text{RESET}}$ released) before. $\overline{\text{RESET}}$ does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if $\overline{\text{RESET}}$ is held low externally beyond the end of the internal sequence (beyond PHASE3).

1.See RGM_FBRE register for more details.

Table 34. $\overline{\text{RESET}}$ electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	$\overline{\text{nRESET}}$ input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	$\overline{\text{nRESET}}$ input not filtered pulse	—	500	—	—	ns

1 V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified

2 C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.20.2 WKUP/NMI timing

Table 35. WKUP/NMI glitch filter

No.	Symbol		Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	D	NMI pulse width that is rejected	—	—	45	ns
2	W_{NFNMI}	D	NMI pulse width that is passed	205	—	—	ns

3.20.3 IEEE 1149.1 JTAG interface timing

Table 36. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	62.5	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at V_{DDE}/2)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

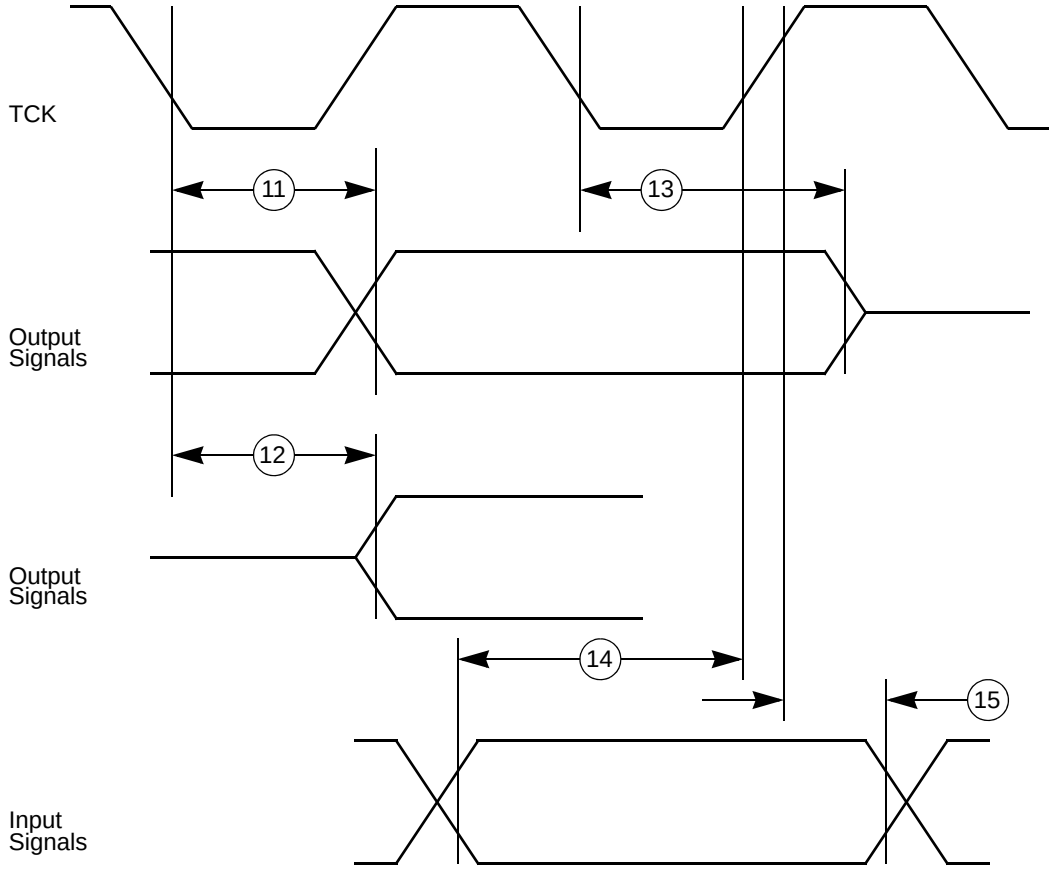


Figure 24. JTAG boundary scan timing

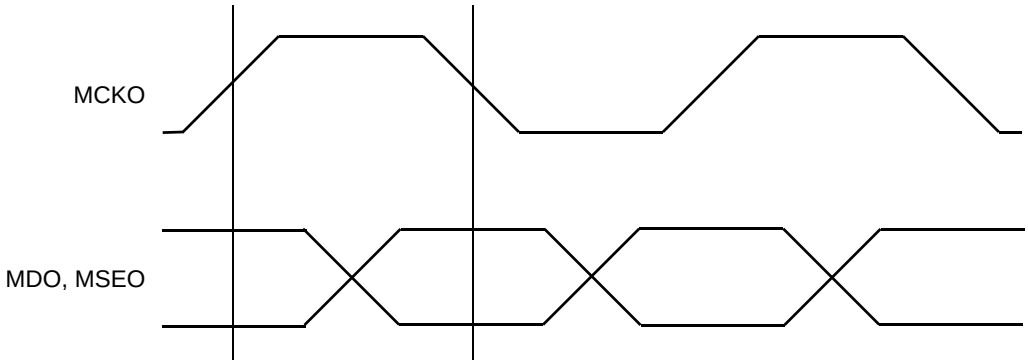
3.20.4 Nexus timing

Table 37. Nexus debug port timing[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	D	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	D	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	D	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	D	$\overline{\text{EVTI}}$ Pulse Width	—	4.0	—	t_{TCYC}
5	t_{EVTOPW}	D	$\overline{\text{EVTO}}$ Pulse Width	—	1		t_{MCYC}
6	t_{TCYC}	D	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	D	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	D	TDI, TMS Data Setup Time	—	8	—	ns
9	t_{NTDIH}, t_{NTMSH}	D	TDI, TMS Data Hold Time		5	—	ns
10	t_{JOV}	D	TCK Low to TDO/RDY Data Valid		0	25	ns

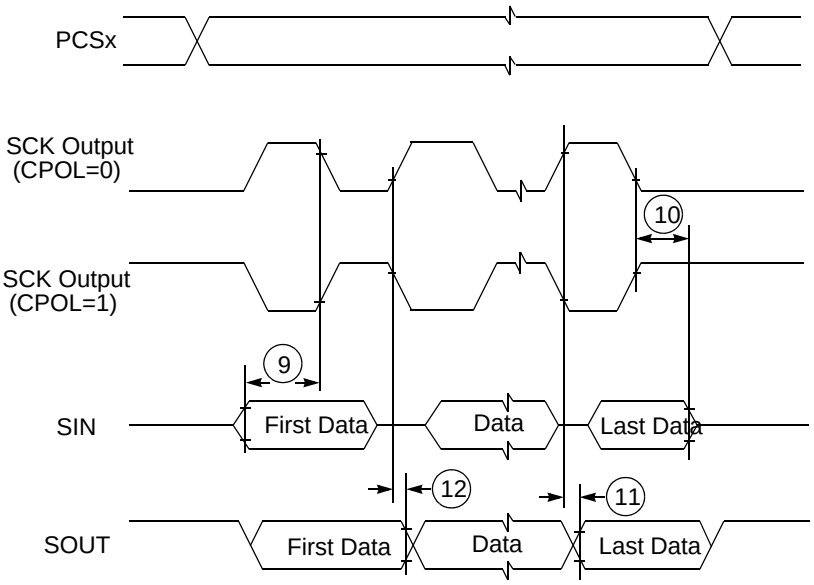
1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

2 For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.



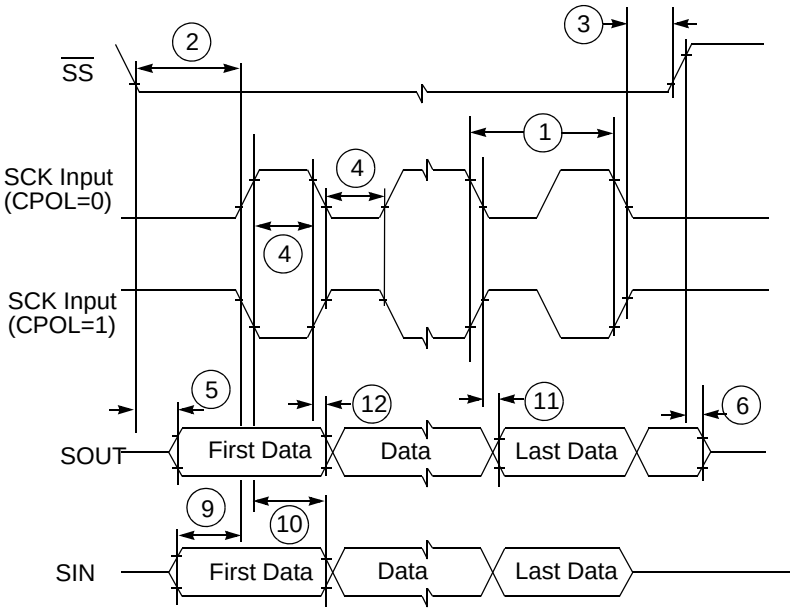
MDO/MSEO data are valid during MCKO rising and falling edge

Figure 27. Nexus Double Data Rate (DDR) Mode output timing



Note: The numbers shown are referenced in Table 39.

Figure 31. DSPI classic SPI timing — master, CPHA = 1



Note: The numbers shown are referenced in Table 39.

Figure 32. DSPI classic SPI timing — slave, CPHA = 0

Table 41. Revision history (continued)

Revision	Date	Description of changes
		• Added Table 29 (MPC5643L SWG Specifications) • In Table 29 (MPC5643L SWG Specifications) Added table footnote for Common Mode. Changed text from “internal device pad resistance” to “internal device routing resistance”. • Added Figure 26 in Section 3.20.4, “Nexus timing”. • In Table 30 (Pad AC specifications (3.3 V , IPP_HVE = 0)), removed the row of pad “Pull Up/Downc(3.6 V max)”. • In Table 40 (Orderable part number summary) and Figure 43, updated part numbers (changed ‘PPC’ to ‘SPC’ and ‘F0’ to ‘F2’). • Replaced Figure 39, Figure 40, Figure 41, Figure 42 with the new versions. • InTable 18 (Voltage regulator electrical specifications),changed the symbol of spec external decoupling capacitor from SR to C_{ext}. In Figure 4, changed the ESR range in note text to 1 mW to 100 mW from 30 mW to 150 mW. • In Section 1.5.32, “Sine Wave Generator (SWG)” removed the following text: Frequency range from 1kHz to 50kHz. Sine wave amplitude from 0.47 V to 2.26 V. • In Table 20 (Current consumption characteristics)”,changed symbol from ‘C’ to ‘T’ , added “operating current” to the parameter and updated the maximum value for five additional RunIDD parameters. • In Table 20 (Current consumption characteristics), changed “Conditions” from ‘1.2 V supplies’ to ‘1.2 V supplies during LBIST (full LBIST configuration)’ for all the parameters. • Removed Table “SWG electrical characteristics”. • In Table 18 (Voltage regulator electrical specifications), changed the “Digital supply high voltage detector upper threshold low limit (After a destructive reset initialization phase completion)” from 1.43V to 1.38V. • Added Table 17 (Recommended operating characteristics). • Updated the IDD values in Table 20 (Current consumption characteristics). Changed conditions text from “1.2 supplies during LBIST (full LBIST configuration)” to “1.2 V supplies” for all the IDD parameters except $I_{DD\_LV\_BIST}$+$I_{DD\_LV\_PLL}$. Added footnote in “Conditions” for the DPM mode. • Removed Cut references from the whole document. • In Table 25 (ADC conversion characteristics), changed the sampling frequency value from ‘1 MHz’ to ‘983.6 KHz’.
8.1	07 May 2012	• Deleted the Footer "Preliminary-Subject to Change Without Notice" label.